CHAPTER 7

CONCLUSION AND FUTURE SCOPE

In future generation wireless communication systems, users are equipped with mobile terminals that can operate in several standards using different physical layers. Reconfigurable architecture is emerging as the platform of choice to design such future high performance wireless communication systems. Reconfigurable architectures meet the performance and flexibility requirements of next generation applications. In this thesis third generation WCDMA standard and OFDM based WiFi standard are considered for the design of reconfigurable architecture. This thesis exploits the use of algorithmic strength reduction transformation technique to reduce the area and power consumption of the proposed architecture by reducing significant amount of multipliers in order to implement radix-2 DIF FFT algorithm and RAKE receiver algorithm. The area and power consumption of the architecture have been estimated at gate level, and implementation results indicated that this architecture is more efficient than the conventional and existing architectures in terms of area. This architecture shares its resources between RAKE receiver processing of WCDMA standard and FFT implementation of OFDM based WiFi standard. A framework has been given to map the applications on this reconfigurable architecture while configuring this hardware dynamically to any one of the standards.

There are several research areas that have to be addressed in the future to extend this research for emerging standards and applications. Some of these areas are outlined briefly as below,

- Emerging architectures are integrating several different architecture paradigms onto the same chip. Conventional microprocessor cores, DSP cores, reconfigurable logic, embedded memory and peripheral controllers are integrated onto the same chip. Developing a model of computation and communication that can be used to map applications and analyze performance is a challenge.

- Algorithmic techniques similar to those in this thesis can be employed to integrate various other advanced wireless standards.

- This design technique can be extended to analyze and optimize the real power dissipation.

- Reconfigurable resource sharing hardware can be used for the realization of the most complex and performance demanding parts of the medium access control layers of the multistandard systems.