CHAPTER 3
LOW-VOLTAGE FGMOS BASED TUNABLE RECIPROCAL CIRCUIT
AND ITS APPLICATIONS

3.1. Introduction

Reciprocal (1/X) circuits are those circuits in which output current (voltage) is inversely proportional to the input current (voltage). These circuits are used as important basic building blocks in analog signal processing applications such as dividers [84-86], current-to-voltage converters [86], filters [87], and logarithmic function generators [88], etc. Several authors have reported reciprocal circuits in literature [84-88].

Laopoulos and Karybakas [84] have suggested a reciprocal circuit based on the voltage-mode divider circuit, which is developed by a voltage controlled oscillator, an integrator and a sample-and-hold circuit. Liu and Liu [86] have proposed voltage-mode CMOS based 1/X circuit operating at the supply voltages of ±1.5V, in which four NMOS transistors, two PMOS transistors and one reference current source are used. In this circuit, the bias current is used to adjust the amplitude of the output. The authors have also suggested a current-to-voltage converter and a current-mode divider as applications of the CMOS based 1/X circuit. Gevel and Kuenen [88] have suggested current-mode MOS based 1/X circuit, in which MOSFETs are biased in the weak inversion region. This circuit is developed by using five PMOS transistors and two reference current sources. The circuit operates at a supply voltage which is slightly more than one threshold voltage of p-type MOSFET. Al-Absi [89] has suggested CMOS current-mode 1/X circuit based on a current-mode divider circuit. The circuit has been developed by using four p-type MOSFETs, which are biased in the weak inversion region.

In this chapter, a low-voltage FGMOS based tunable reciprocal circuit is presented. This circuit is developed by using one of the grounded resistors namely, modified FGVCR suggested in Chapter 2. The proposed circuit uses four n-type FGMOS transistors, four p-type FGMOS transistors and a reference current source. The output amplitude of the reciprocal circuit is controlled by a reference current. This circuit is used as a basic building block to develop FGMOS based current-to-voltage converters (operating at dual and single power supplies) and current-mode dividers (one-quadrant and two-quadrant). All the proposed circuits have been simulated using OrCAD PSPICE and the simulation results are
presented. The performance parameters of the proposed circuits have also been compared with the existing circuits available in literature and the comparison shows that the proposed circuits have improved performance in terms of supply voltage requirement, power dissipation, total harmonic distortion (THD) and input range, which validate the effectiveness of these circuits.

This chapter is organized as follows. Section 3.2 discusses the FGMOS based tunable reciprocal circuit. In Section 3.3, FGMOS based current-to-voltage converters are proposed. Section 3.4 presents the FGMOS based current-mode dividers. The simulation results of the proposed circuits are presented in Section 3.5. The chapter is concluded in Section 3.6.

3.2. FGMOS based tunable reciprocal circuit

The FGMOS based tunable reciprocal circuit is shown in Fig. 3.1. The reciprocal behaviour of this circuit is generated by the transistors M_1 and M_2, whereas M_3, M_4, M_5 and M_6 provide proper biasing. The transistors M_1 and M_2 are biased in the ohmic region and both are perfectly matched i.e. $K_{n1} = K_{n2} = K_n$, $V_{Tn1} = V_{Tn2} = V_{Tn}$, $k_{11} = k_{21} = k_1$ and $k_{12} = k_{22} = k_2$. The transistors M_7 and M_8 are biased in the saturation region and both are perfectly matched i.e. $K_{p7} = K_{p8}$, $V_{Tp7} = V_{Tp8}$, $k_{71} = k_{81}$ and $k_{72} = k_{82}$. These transistors form a current mirror that generates reference current $I_{ref}$. Using eqn. (1.8), the drain currents $I_1$ and $I_2$ are given as

$$I_1 = K_{n1} \left\{ k_1 (V_b - V_{SS}) + k_2 (0 - V_{SS}) - V_{Tn1} \right\} V_{DS1} - \left( \frac{1}{2} \right) V_{DS1}^2$$

$$I_2 = I_{ref} + I_4 = K_{n2} \left\{ k_1 (V_b - V_{SS}) + k_2 (V_{in} - V_{SS}) - V_{Tn2} \right\} V_{DS2} - \left( \frac{1}{2} \right) V_{DS2}^2$$

where $K_{n1}$ & $K_{n2}$ are the transconductance parameters,

$k_1 ( = C_1/\mu_C)$ & $k_2 ( = C_2/\mu_C)$ are the capacitive coupling ratios,

$C_T ( = C_1 + C_2)$ is the total capacitance,

$V_b$ is the bias voltage, $V_{SS}$ is the source voltage,

$V_{Tn1}$ and $V_{Tn2}$ are the threshold voltages,

$V_{DS1}$ and $V_{DS2}$ are the drain-to-source voltages,

$I_{ref}$ is the reference current and

$I_4$ is the drain current of transistor $M_4$. 

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The transistors $M_5$ and $M_6$ are biased in the saturation region and both are perfectly matched i.e. $K_{p5} = K_{p6}$, $V_{tp5} = V_{tp6}$, $k_{s1} = k_{s2}$ and $k_{s2} = k_{s2}$. These transistors form a current mirror that generates current $I_3$, therefore

$$I_3 = I_4 = I_1 \quad (3.3)$$

The transistors $M_3$ and $M_4$ are biased in the saturation region and both are perfectly matched i.e. $K_{n3} = K_{n4}$, $V_{tn3} = V_{tn4}$ and $k_{s1} = k_{s4}$. Using eqn. (1.9), the currents $I_3$ and $I_4$ are given as

$$I_3 = \frac{K_{n3}}{2} (V_{FGS3} - V_{tn3})^2 \quad (3.4)$$

$$I_4 = \frac{K_{n3}}{2} (V_{FGS4} - V_{tn3})^2 \quad (3.5)$$

From eqns. (3.3), (3.4) and (3.5), the voltages $V_{FGS3}$ and $V_{FGS4}$ are obtained as

$$V_{FGS3} = V_{FGS4} = \sqrt{\frac{2I_1}{K_{n3}}} + V_{tn3} \quad (3.6)$$
Since \( V_{FGS3} + V_{DS1} = V_{FGS4} + V_{DS2} \), therefore

\[
V_{DS1} = V_{DS2} \tag{3.7}
\]

Substituting eqns. (3.1), (3.3) and (3.7) in eqn. (3.2), the output voltage \( V_{DS2} \) is obtained as

\[
V_{DS2} = \frac{I_{ref}}{K_n k_2 V_{in}} \tag{3.8}
\]

Equation (3.8) verifies the reciprocal behaviour of the proposed circuit shown in Fig. 3.1. Hence, Fig. 3.1 behaves as a reciprocal circuit and its output amplitude is controlled by the reference current \( I_{ref} \). The simulation results of FGMOS based reciprocal circuit are presented in Section 3.5.1.

3.3. FGMOS based current-to-voltage converters

Current-to-voltage converters play an important role as interface/measurement elements in current-mode mixed signal circuits. Liu and Liu [86] have suggested current-to-voltage converter circuit operating at supply voltage of 2.5V. This circuit is developed by using four NMOS transistors and two PMOS transistors. Srinivasan et al. [90] have proposed current-to-voltage converter circuit, which is developed by using the core converter, the replica biasing scheme and the current multiplication block. In this Section, two current-to-voltage converters operating with dual and single power supplies are presented. These circuits are developed by using four n-type 2-input FGMOSs and two p-type 2-input FGMOSs.

3.3.1. FGMOS based current-to-voltage converter operating with dual power supply

In eqn. (3.8), if the input voltage \( V_{in} \) is replaced by the reference voltage \( V_{ref} \) and the reference current \( I_{ref} \) is replaced by the input current \( I_{IN} \), then eqn. (3.8) is modified as

\[
V_{DS2} = \frac{I_{IN}}{K_n k_2 V_{ref}} \tag{3.9}
\]
From eqn. (3.9), it is observed that the modified form of the reciprocal circuit, shown in Fig. 3.2, can be used as a current-to-voltage converter operating with the dual power supply.

\[
V_{DS2} = V_{out} - V_{b1}
\]

**Eq. 3.10**

Equation (3.10) gives the linear relationship between input current \( I_{IN} \) and output voltage \( V_{D2} \). Hence, Fig. 3.3 behaves as a current-to-voltage converter and its gain is controlled by the difference of the reference voltages \( V_{ref2} - V_{ref1} \). The simulation results of FGMOS based current-to-voltage converters are presented in Section 3.5.2.

3.3.2. FGMOS based current-to-voltage converter operating with a single power supply

Fig. 3.2 is further modified to operate with a single supply as shown in Fig. 3.3 (overleaf). In this circuit, the reference voltages \( V_{ref1} \) and \( V_{ref2} \) are connected to the input gates of transistors \( M_1 \) and \( M_2 \) respectively and the source terminals of transistors \( M_1 \) and \( M_2 \) are connected to the ground. For the circuit shown in Fig. 3.3, eqn. (3.9) is modified as

\[
V_{D2} = \frac{I_{IN}}{K_n k_2 (V_{ref2} - V_{ref1})}
\]

**Eq. 3.10**

Equation (3.10) gives the linear relationship between input current \( I_{IN} \) and output voltage \( V_{D2} \). Hence, Fig. 3.3 behaves as a current-to-voltage converter and its gain is controlled by the difference of the reference voltages \( V_{ref2} - V_{ref1} \). The simulation results of FGMOS based current-to-voltage converters are presented in Section 3.5.2.
3.4. FGMOS based current-mode dividers

The analog dividers are important non-linear building blocks that have found usefulness in the design of signal processing circuits such as analog computation, analog-to-digital (A/D) converters and communication systems, etc. Liu and Liu [86] have suggested current-mode divider operating at supply voltages of ±2.5V. Lopez-martin and Carlosena [91] have proposed current-mode divider operating at supply voltage of 3.3V. In this Section, FGMOS based one-quadrant and two-quadrant current-mode dividers operating at ±0.90V and ±0.75V respectively are presented. In eqn. (3.8), if the reference current $I_{ref}$ is replaced by the input current $I_{IN}$, the eqn. (3.8) is modified as

$$V_{DS2} = \frac{I_{IN}}{K_n k_2 V_{in}}$$  \hspace{1cm} (3.11)

Figure 3.4 shows the circuit in which the reference current $I_{ref}$ is replaced by the input current $I_{IN}$. This circuit is used as a basic building block (BB) to develop FGMOS based one-quadrant and two-quadrant current-mode dividers.
3.4.1. FGMOS based one-quadrant current-mode divider

The FGMOS based one-quadrant current-mode divider is shown in Fig. 3.5. This circuit has been developed by cascading the circuits of Figs. 3.3 and 3.4. In Fig. 3.5, the transistors $M_1$, $M_2$, $M_7$ and $M_8$ are perfectly matched i.e. $K_{n1} = K_{n2} = K_{n7} = K_{n8} = K_n$, $V_{Tn1} = V_{Tn2} = V_{Tn7} = V_{Tn8} = V_{Tn}$, $k_{11} = k_{21} = k_{71} = k_{81} = k_1$ and $k_{12} = k_{22} = k_{72} = k_{82} = k_2$. 

Fig. 3.4 Building block (BB)

C-to-V converter (Fig. 3.3)  BB (Fig. 3.4)

Fig. 3.5 FGMOS based one-quadrant current-mode divider
Using eqn. (3.10), the output voltage of Block-1 (Fig. 3.5) is given as

\[ V_{out1} = \frac{I_{IN2}}{K_n k_2 (V_{ref2} - V_{ref1})} \]  

(3.12)

This output voltage of Block-1 becomes the input voltage of Block-2 (Fig. 3.5), hence

\[ V_{in2} = \frac{I_{IN2}}{K_n k_2 (V_{ref2} - V_{ref1})} \]  

(3.13)

Using eqn. (3.11), the output voltage of Block-2 (Fig. 3.5) is given as

\[ V_{out} = V_{DS2} = \frac{I_{IN1}}{K_n k_2 V_{in2}} \]  

(3.14)

Substituting the value of \( V_{in2} \) from eqn. (3.13) in eqn. (3.14), the output voltage \( V_{out} \) is obtained as

\[ V_{out} = (V_{ref2} - V_{ref1}) \left( \frac{I_{IN1}}{I_{IN2}} \right) \]  

(3.15)

Equation (3.15) verifies the current-division behaviour of the circuit of Fig. 3.5. Hence, Fig. 3.5 behaves as a current-mode divider and the gain of the proposed circuit is controlled by the difference of the reference voltages \( V_{ref2} - V_{ref1} \).

### 3.4.2. FGMOS based two-quadrant current-mode divider

The FGMOS based two-quadrant current-mode divider is shown in Fig. 3.6. The basic building block shown in Fig. 3.4 is used to develop this circuit. In this circuit, the transistors \( M_1, M_2, M_7 \) and \( M_8 \) are perfectly matched i.e. \( K_{n1} = K_{n2} = K_{n7} = K_{n8} = K_n \), \( V_{Tn1} = V_{Tn2} = V_{Tn7} = V_{Tn8} = V_{Tn}, k_{11} = k_{21} = k_{71} = k_{81} = k_1 \) and \( k_{12} = k_{22} = k_{72} = k_{82} = k_2 \).
Using eqn. (3.10), the output voltage of Block-1 (Fig. 3.6) is given as

\[
V_{out1} = \frac{I_{IN2}}{K_n k_4 (V'_{ref2} - V'_{ref1})}
\]  

(3.16)

This output voltage of Block-1 becomes the input voltage of Block-2 (Fig. 3.6), hence

\[
V_{in2} = \frac{I_{IN2}}{K_n k_4 (V'_{ref2} - V'_{ref1})}
\]  

(3.17)

Using eqn. (3.11), the output voltage of Block-2 (Fig. 3.6) is given as

\[
V_{out} = V_{DS2} = \frac{I_{IN1}}{K_n k_4 V_{in2}}
\]  

(3.18)
Substituting the value of $V_{in2}$ from eqn. (3.17) in eqn. (3.18), the output voltage $V_{out}$ is obtained as

$$V_{out} = V_{DS2} = \left( V'_{ref2} - V'_{ref1} \right) \left( \frac{I_{IN1}}{I_{IN2}} \right). \tag{3.19}$$

Equation (3.19) verifies the current-division behaviour of the circuit of Fig. 3.6. Hence, Fig. 3.6 behaves as a current-mode divider and the gain of the proposed circuit is controlled by the difference of the reference voltages $(V'_{ref2} - V'_{ref1})$. Also, from eqn. (3.19), it can be seen that if $V'_{ref1} > V'_{ref2}$, then four quadrant current-mode divider can be developed. The simulation results of FGMOS based current-mode dividers are presented in Section 3.5.3.

3.5. Simulation results

In this Section, the simulation results of FGMOS based reciprocal circuit, current-to-voltage converters (operating with dual and single power supplies) and current-mode dividers (one-quadrant and two-quadrant) are presented. The workability of these circuits have been verified by OrCAD PSPICE using model parameters of 0.5 µm CMOS technology, which are listed in Appendix B.

3.5.1. Simulation results of FGMOS based reciprocal circuit

This Section presents the simulation results of FGMOS based reciprocal circuit shown in Fig. 3.1. Figure 3.7 shows the variation of output voltage $(V_{DS2})$ with respect to input voltage $(V_{in})$ of the reciprocal circuit operating at supply voltages of ±0.75V. The output voltage $V_{DS2}$ is plotted for $I_{ref} = 10 \, \mu A$, $15 \, \mu A$ and $20 \, \mu A$, while $V_{in}$ is varied from 0.06V to 0.75V. The simulation results are consistent with the theoretical results calculated using eqn. (3.8) and the error between theoretical and simulated values is found to be less than ±2%. For the distortion analysis of this circuit, a sinusoidal input voltage $V_{in}$ of 100 KHz with peak-to-peak amplitude ranging from 0.15V to 0.75V is employed. Figure 3.8 shows the THD obtained in the output waveform as a function of the peak-to-peak input voltage. From this figure, it is
observed that for input voltage ranging from 0.15V to 0.75V, distortion is still low (≤ 0.98%). The total power dissipation of this circuit is 137µW.

Fig. 3.7 Simulation results of FGMOS based reciprocal circuit

Fig. 3.8 THD vs. input voltage amplitude of FGMOS based reciprocal circuit
Figure 3.9 shows the frequency response of the reciprocal circuit and it is observed that the response remains constant till 15.8 MHz. The proposed FGMOS based reciprocal circuit is compared with CMOS 1/X circuit reported in [86] and is listed in Table 3.1. From the table, it is observed that the FGMOS based reciprocal circuit has lower supply voltage requirement, lower power dissipation and lower THD than the existing circuit.

Table 3.1 Comparison of FGMOS based reciprocal circuit with the CMOS 1/X circuit reported in [86]

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>1/X circuit [86]</th>
<th>FGMOS based reciprocal circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>$V_{DD}=</td>
<td>V_{SS}</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>0.24 mW</td>
<td>137 µW</td>
</tr>
<tr>
<td>THD</td>
<td>Not available</td>
<td>0.98% for the input signal 0.75V&lt;sub&gt;pp&lt;/sub&gt; at 100 KHz</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>Not available</td>
<td>15.8 MHz</td>
</tr>
</tbody>
</table>
3.5.2. Simulation results of FGMOS based current-to-voltage converters

Section 3.5.2 discusses the simulation results of FGMOS based current-to-voltage converters operating with dual and single power supplies shown in Figs. 3.2 and 3.3 respectively.

3.5.2.1. Simulation results of FGMOS based current-to-voltage converter operating with dual power supply

Figure 3.10 shows the I-V characteristics of the FGMOS based current-to-voltage converter operating at supply voltages of ±0.75V. The output voltage $V_{DS2}$ is plotted for $V_{ref} = 0.40V$, $0.60V$ and $0.80V$, while $I_{IN}$ is varied from 0 to 35 µm. The simulation results are consistent with the theoretical results calculated using eqn. (3.9) and error between theoretical and simulated values is found to be less than 2%.

![I-V characteristics of FGMOS based current-to-voltage converter](image_url)
For the distortion analysis of this circuit, a sinusoidal input current $I_{IN}$ of 100 KHz with peak-to-peak amplitude ranging from 5 µA to 35 µA is employed. Figure 3.11 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ranging from 5 µA to 35 µA, distortion is still low ($\leq 0.68\%$). The total power dissipation of this circuit is 137 µW. Figure 3.12 shows the frequency response of the current-to-voltage converter and it is observed that the response remains constant till 1.1 MHz.

![Fig. 3.11 THD vs. input current amplitude of FGMOS based current-to-voltage converter operating with dual power supply](image1)

![Fig. 3.12 Frequency response of FGMOS based current-to-voltage converter operating with dual power supply](image2)
3.5.2.2. Simulation results of FGMOS based current-to-voltage converter operating with a single power supply

Figure 3.13 shows the I-V characteristics of the FGMOS based current-to-voltage converter operating at a single supply voltage of 0.90V. The output voltage $V_{D2}$ is plotted for $V_{ref2} - V_{ref1} = 0.30V$, 0.35V and 0.40V, while $I_{IN}$ is varied from 0 to 35 $\mu$A. These values of $V_{ref2} - V_{ref1}$ are obtained by choosing the reference voltage $V_{ref1}$ as 0.50V and the reference voltage $V_{ref2}$ as 0.80V, 0.85V and 0.90V. The simulation results are consistent with the theoretical results calculated using eqn. (3.10) and error between theoretical and simulated values is found to be less than 2%.

Fig. 3.13 I-V characteristics of FGMOS based current-to-voltage converter operating with a single power supply
For the distortion analysis of this circuit, a sinusoidal input current $I_{IN}$ of 100 KHz with peak-to-peak amplitude ranging from 5 µA to 35 µA is employed. Figure 3.14 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ranging from 5 µA to 35 µA, distortion is still low ($\leq 0.45\%$). The total power dissipation of this circuit is 12 µW. Figure 3.15 shows the frequency response of the current-to-voltage converter and it is observed that the response remains constant till 1.6 MHz.

Fig. 3.14 THD vs. input current amplitude of FGMOS based current-to-voltage converter operating with a single power supply

Fig. 3.15 Frequency response of FGMOS based current-to-voltage converter operating with a single power supply
A comparison of the FGMOS based current-to-voltage converters operating with dual and single power supplies are listed in Table 3.2. From this table, it is observed that the current-to-voltage converter operating with a single power supply has lower power dissipation, lower THD and wider bandwidth as compared to current-to-voltage converter operating with dual power supply.

Table 3.2 Comparison of FGMOS based current-to-voltage converters operating with dual and single power supplies

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>FGMOS based current-to-voltage converter (Fig. 3.2)</th>
<th>FGMOS based current-to-voltage converter (Fig. 3.3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>$V_{DD}=</td>
<td>V_{SS}</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>137 µW</td>
<td>12 µW</td>
</tr>
<tr>
<td>THD</td>
<td>0.68% for the input signal 35 µA (peak-to-peak) at 100 KHz</td>
<td>0.45% for the input signal 35 µA (peak-to-peak) at 100 KHz</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>1.1 MHz</td>
<td>1.6 MHz</td>
</tr>
</tbody>
</table>

Table 3.3 compares the proposed FGMOS based current-to-voltage converter operating with a single power supply (Fig. 3.3) with current-to-voltage converters reported in [86] and [90]. From this table, it is observed that the FGMOS based current-to-voltage converter presented in this section has lower supply voltage requirement, lower THD, lower power dissipation and wider input current range as compared to the existing circuits.

Table 3.3 Comparison of FGMOS based current-to-voltage converter operating with a single power supply and current-to-voltage converters reported in [86] and [90]

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>Current-to-voltage converter[86]</th>
<th>Current-to-voltage converter [90]</th>
<th>FGMOS based current-to-voltage converter (Fig. 3.3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>$V_{DD} = 2.50 V$</td>
<td>Not available</td>
<td>$V_{DD} = 0.90 V$</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Current range</td>
<td>0 to 35 µA</td>
<td>10 nA to 2.5 µA</td>
<td>0 to 35 µA</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Not available</td>
<td>Not available</td>
<td>12 µW</td>
</tr>
<tr>
<td>THD</td>
<td>Not available</td>
<td>0.82%</td>
<td>0.45%</td>
</tr>
<tr>
<td>3dB frequency</td>
<td>Not available</td>
<td>10 MHz</td>
<td>1.6 MHz</td>
</tr>
</tbody>
</table>
3.5.3. Simulation results of FGMOS based current-mode dividers

Section 3.5.3 discusses the simulation results of FGMOS based one-quadrant and two-quadrant current-mode dividers shown in Figs. 3.5 and 3.6, respectively.

3.5.3.1. Simulation results of FGMOS based one-quadrant current-mode divider

Figure 3.16 shows the I-V characteristics of the FGMOS based one-quadrant current-mode divider operating at supply voltages of ±0.90V. The output voltage $V_{out}$ is plotted for $I_{IN2} = 20 \mu A, 25 \mu A$ and $30 \mu A$, while $I_{IN1}$ is varied from 0 to 30 $\mu m$. From the plots, it is observed that output voltage ($V_{out}$) is directly proportional to the input current ($I_{IN1}$). The simulation results are consistent with the theoretical results calculated using eqn. (3.15) and error between theoretical and simulated values is found to be less than 2%.

![Fig. 3.16 I-V characteristics of FGMOS based one-quadrant current-mode divider](image)

For the distortion analysis of this circuit, the sinusoidal input currents $I_{IN1}$ of 100 KHz with peak-to-peak amplitude ranging from 0.05 $\mu A$ to 0.20 $\mu A$ and $I_{IN2} = 30 \mu A$ are employed. Figure 3.17 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ($I_{IN1}$) ranging from 0.05 $\mu A$ to 0.20 $\mu A$, distortion is still low ($\leq 1.28\%$). The total power dissipation of this
circuit is 635 µW. Figure 3.18 shows the frequency response of this current-mode divider and it is observed that the response remains constant till 604 KHz.

Fig. 3.17 THD vs. input current amplitude of FGMOS based one-quadrant current-mode divider

Fig. 3.18 Frequency response of FGMOS based one-quadrant current-mode divider
3.5.3.2. Simulation results of FGMOS based two-quadrant current-mode divider

Figure 3.19 shows the I-V characteristics of the FGMOS based two-quadrant current-mode divider operating at supply voltages of ±0.75V. The output voltage $V_{out}$ is plotted for $I_{IN2} = 20 \ \mu A$, $25 \ \mu A$ and $30 \ \mu A$, while $I_{IN1}$ is varied from -30 $\mu m$ to 30 $\mu m$. From the plots, it is observed that output voltage ($V_{out}$) is directly proportional to the input current ($I_{IN1}$). The simulation results are consistent with the theoretical results calculated using eqn. (3.19) and error between theoretical and simulated values is found to be less than 2%.

For the distortion analysis of this circuit, the sinusoidal input currents $I_{IN1}$ of 100 KHz with peak-to-peak amplitude ranging from 0.05 $\mu A$ to 0.20 $\mu A$ and $I_{IN2} = 30 \ \mu A$ are employed. Figure 3.20 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ($I_{IN1}$) ranging from 0.05 $\mu A$ to 0.20 $\mu A$, distortion is still low ($\leq 0.93\%$). The total power dissipation of this circuit is 356 $\mu W$. Figure 3.21 shows the frequency response of the current-mode divider and it is observed that the response remains constant till 857 KHz.
Fig. 3.20 THD vs. input current amplitude of FGMOS based two-quadrant current-mode divider

Fig. 3.21 Frequency response of FGMOS based two-quadrant current-mode divider
A comparison of the proposed FGMOS based current-mode dividers (one-quadrant and two-quadrant) are listed in Table 3.4. From this table, it is observed that the two-quadrant current-mode divider has lower supply voltage requirement, lower power dissipation, lower THD and wider bandwidth as compared to one-quadrant current-mode divider.

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>FGMOS based one-quadrant current-mode divider</th>
<th>FGMOS based two-quadrant current-mode divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>$V_{DD} =</td>
<td>V_{SS}</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Current range</td>
<td>0 to 30 µA</td>
<td>-30 to 30 µA</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>635 µW</td>
<td>356 µW</td>
</tr>
<tr>
<td>THD</td>
<td>1.28%</td>
<td>0.93%</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>604 KHz</td>
<td>857 KHz</td>
</tr>
</tbody>
</table>

Table 3.5 compares the proposed FGMOS based two-quadrant current-mode divider with current-mode dividers reported in [86] and [91]. From this table, it is observed that the FGMOS based two-quadrant current-mode divider presented in this section has lower supply voltage requirement, lower THD, lower power dissipation and wider input current range as compared to the existing circuits.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>$V_{DD} =</td>
<td>V_{SS}</td>
<td>= 2.5V$</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>2.4 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Current range</td>
<td>0 to 20 µA</td>
<td>10 nA to 2.5 µA</td>
<td>-30 to 30 µA</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Not available</td>
<td>600 µW</td>
<td>356 µW</td>
</tr>
<tr>
<td>THD</td>
<td>Not available</td>
<td>1.5%</td>
<td>0.93%</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>Not available</td>
<td>3 MHz</td>
<td>857 KHz</td>
</tr>
</tbody>
</table>
3.6. Conclusions

In this chapter, FGMOS based analog building blocks such as reciprocal circuit, current-to-voltage converters and current–mode dividers are proposed. The simulation results of all the circuits have been presented and compared with the existing circuits. The proposed circuits have lower supply voltage requirement, lower power dissipation, lower THD and wider input dynamic range as compared to the existing circuits available in literature.