Annexure

- List of Publications
- Publications Reprint
ANNEXURE - I

List of Publications

1. “89S52 Microcontroller based speed control of vehicle nearby Educational Institutions”  

2. “Design of remote EB metering system with Arm controller”  

3. “FPGA Based SOC for Railway Level crossing Management System”  

4. “Design and implementation of SOC in NIOS-II soft core processor for secured wireless communication”  

5. “Designing of reconfigurable MPNoC on FPGA for processing the wireless sensor networks”  
89S52 Microcontroller based Speed Control of Vehicles nearby Educational Institutions

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Abstract

Nowadays people are driving very fast, accidents are occurred frequently. Hence, the invaluable human life lost, because of the small mistakes while driving. Therefore to avoid such accidents, the project was designed to alert the driver and to control the speed of the vehicle automatically using AT89S52 microcontroller [1], RF transmitter and RF receiver modules. The objective of this project work is to use 89S52 microcontroller to alert the driver about zone to be crossed and control the speed of vehicle automatically, using RF modules. Every zone like school, college, Pedestrians in high ways or hospitals etc may have transmitter tag to transmit the zone information by RF signals. A receiver module placed in the vehicle receives the zone information, which is to be used to alert the driver with buzzer and to vary the speed of the vehicle. A demo module was developed in the lab using DC motor. Practically the actuator may be used to control the throttle of the vehicle.

Keywords: 89S52, RF sensor, speed control.

Introduction

In the modern world, one of the worst scenarios is road fatalities. Road fatalities are a major concern in human life. Recent studies [2] show that a third of the number of fatal or serious accidents is associated with excessive or inappropriate speed of the
vehicles, as well as changes in the road way (like the presence of road work or unexpected obstacles). Reduction of the number of accidents and mitigation of their consequences are big concern of traffic authorities, the automotive industry and transport research groups. Advanced driver assistance system is the solution, which are acoustic or visual signals produced by the vehicle itself to communicate the driver about the possibility of the accident. These advanced systems are somewhat available in almost all commercial vehicles today, and future trends indicate that the higher safety will be achieved by automatic driving signals and a growing number of sensors both on the road, at accident prone zones and inside of the vehicle [3].

Pedestrians especially school children are the most vulnerable traffic participants, because they are often seriously injured in traffic accidents. Pedestrian signal detection is to alert the driver and for automatic speed control in such areas. Generally, to assist the vehicle driver, cruise control (CC) may be used, which has the capability of maintaining a constant user preset speed[4], and its evolution is adaptive cruise control (ACC), which adds to cruise control with the capability of keeping safe distance from preceding vehicle[5]. A drawback of these systems is that they are not independently capable of distinguishing between straight and curved parts of the road, where the speed has to be lowered to avoid accidents. However, curve warning systems (CWS) have been recently developed that use a combination of global positioning system (GPS) and digital maps obtained from a geographical information system (GIS), to assess threat levels for a driver approaching a curve too quickly [6]; likewise intelligent speed assistance (ISA) systems warn the driver when the vehicle’s velocity is inappropriate, using GPS in combination with a digital road map containing information about the speed limits [7].

However, useful of these systems are inoperative where unusual road circumstances such as road work, road diversions, accidents etc. RF modules [8] not only used at educational institutions, may also be placed anywhere where the necessity exist to warn the driver. While artificial vision based recognition of traffic signals might fail if visibility is poor, insufficient light, difficult weather conditions or blocking of the line of sight by preceding vehicles, RF signals might still be transmitted reliable. This work is to focus mainly the application of 89S52 controller. Radio frequency (RF) is a rate of oscillation in the range of about 30 kHz to 300 GHz, which corresponds to the frequency of electrical signals normally used to produce and detect radio waves. RF sensor module is reliable with its high distance coverage and cost effective. Similar kind of work has done by Joshua Perez, where they used RFID tags for the application to control the speed of the vehicle [9].

This paper is organized as follows, a detailed functional description of 433 MHz RF transmitter STT-433, and 433 MHz RF receiver STR-433 [10], HT 12E Encoder, HT12D Decoder, [11] and the features of 89S52 microcontroller features in section 2. In the third section consists of a functional description of the circuit diagram. This paper ends with the conclusion. The figure (1) illustrates block diagram of the transmitter module placed in the pedestrian signal nearby the educational institution.
Components discussion
In this section, we describe the sensors, decoder, encoder, and the features of microcontroller 89S52, which we have been installed at the pedestrian signal before the Educational Institution or any other places of accidental prone zones, where we required automatic speed control.

433 MHz RF Transmitter STT-433
It is low cost RF transmitter [8], and operates from 1.5 to 12V supply. The transmitter employs a SAW- stabilized oscillator, ensuring accurate frequency control for best range performance. Small in size consumes 11mA at 3V. Its minimum data rate 200 BPS and maximum is 3KBPS. It has good temperature adaptability (from -20 °C to +60 °C).

OOK (on off keying) modulation is a binary form of amplitude modulation. When a logical 0 (Data line low) is being sent, the transmitter is off, fully suppressing the
carrier. In this state, the transmitter current is very low, less than 1 mA. When a logical 1 is being sent, the carrier is fully on. In this state, the module current consumption is at its highest, about 11 mA with a 3V power supply. OOK is the modulation method needs no power when it transmits a 0, and requires better power consumption than FSK transmitters for transmitting 1. OOK data rate is limited by the start up time of the oscillator. High Q oscillators which have very stable center frequency take longer to startup than low Q oscillators. The startup time of the oscillator determines the maximum data rate that the transmitter can send. Data rate could be controlled by the oscillator startup time. It is on the order of 40 μs, which limits the maximum data rate to 4.8 kbit/sec. In the transmitter SAW stabilized oscillator is used, basically the transmitter is a negative resistance LC oscillator, whose center frequency is tightly controlled by a SAW resonator. SAW (Surface Acoustic Wave) resonators are fundamental frequency devices that resonate at frequencies much higher than the crystals.

433 MHz RF Receiver STR-433

The receiver module requires no external RF components except for the antenna. It generates virtually no emission. It is low cost, operating voltage is 5V and the operating current is typically 3.5 mA and requires no external parts. Receiver frequency is about 433.92 MHz, whose sensitivity is -105dBm. Data rate of the receiver is 3 K bits/s.

The STR – 433 [8] uses a super – regenerative AM detector to demodulate the incoming AM carrier. A super regenerative detector is a gain stage with positive feedback greater than unity so that it oscillates. An RC time constant is included in the gain stage so that when the gain stage oscillates, the gain will be lowered over time proportional to the RC time constant until the oscillation eventually dies. When the oscillation dies, the current draw of the gain stage decreases, charging the RC circuit, increasing the gain, and ultimately the oscillation starts again. In this way, the oscillation of the gain stage is turned on and off at a rate set by the RC time constant. This rate is chosen to be super audible but much lower than the main oscillation rate. Detection is accomplished by measuring the emitter current of the gain stage. Any RF input signal at the frequency of the main oscillation will aid the main oscillation in restarting. If the amplitude of the RF input increases, the main oscillation will stay on for a longer period of the time, and the emitter current will be higher. Therefore, we can detect the original base-band signal by simply low pass filtering the emitter current. The average emitter current is not very linear as a function of the RF input level. It exhibits a 1/ln response because of the exponentially rising nature of oscillator start-up. The steep slope of algorithm near zero results in high sensitivity to small input signals.

Another important block in the receiver is Data slicer, which converts the base band analog signal from the super-regenerative detector to a CMOS/TTL compatible output. Because the data slicer is AC coupled to the audio output, there is a minimum data rate. AC coupling also limits the minimum and maximum pulse width. Typically data is encoded on the transmit side using pulse width modulation (PWM) or non return to zero (NRZ). The most common source for NRZ data is from a UART
embedded in a microcontroller. Applications that use NRZ data encoding typically involve microcontrollers. Data is sent as a constant rate square wave. The Duty cycle of that square wave will generally be either 33% (a zero) or 88% (a one). The data slicer on the STR-433 is optimized for use with PEM encoded data, though it will work with NRZ data if certain encoding rules are followed.

Power supply is another important factor to work with any passive components. The STR-433 is designed to operate from a 5V power supply. It is crucial that this power supply be very quiet. The power supply should be bypassed using 0.1µF low – ESR ceramic capacitor and a 4.7 µF tantalum capacitor. These capacitors should be placed as close to the power pins as possible. The STR-433 is designed for continuous duty operation. From the time power is applied, it can take up to 750 ms for the data output become valid.

STR-433 support most antenna type, including printed antennas integrated directly on to the PCB and simple single core wire of about 17cm. the performance of the different antennas varies. Any time a trace is longer than 1/8th the wave length of the frequency it is carrying, it should be a 50 ohm microchip.

HT–12 E Encoder
HT-12E is the encoder [9] capable of encoding information which consists of N address bits and 12- N data bits. Each address/ data input can be set to one of the two logic states. The programmed addresses/data are transmitted together with the header bits via RF or an infrared transmission medium upon receipt of a trigger signal. Its operating voltage is 2.4V – 12V. it is fabricated using CMOS technology, housed in 18 pin DIP. Other features are listed as follows;

- Low standby current:0.1μA at VDD = 5V
- Minimum transmission is four words
- Built in oscillator needs only 5% resistor
- Data code has positive polarity
- Minimal external components.

The status of each address / data pin can be individually pre-set to logic “high” or “low”. If a transmission- enable signal is applied, the encoder scans and transmits the status of the 12 bits of address/data serially in the order A0 to A11. during information transmission these bits are transmitted with a preceding synchronization bit. If the trigger signal is not applied, the chip enters the standby mode and consumes a reduced current of less than 1µA for a supply voltage of 5V.

HT-12D Decoder
HT-12D decoders [9] receive serial addresses and data programmed series of encoders that are transmitted by a carrier using RF or an IR transmission medium. They compare the serial input data three times continuously with their local addresses, if no error or unmatched codes are found, the input data codes are decoded and then transferred to the output pins. The VT pin indicates the status of transmission, when it is high means, it is valid transmission. This decoder is capable of decoding information that consists of N bits of address and 12-N bits of data. For proper
operation a pair of encoder/decoder with the same number of addresses and data format should be chosen.

Features of 89S52 microcontroller
The AT89S52 microcontroller [1] is a low power, high performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable flash memory. The specialty over its predecessor is on-chip Flash memory which allows the program memory to be reprogrammed in-system. This controller consists of 8-kbytes of Flash, 256 bytes of RAM, 32 I/O lines, watchdog timer, two data pointers, three 16-bit timer/counters, a six vector two level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. The AT89S52 has three ports which are having multiplexed functions.

Functional Description of the circuit
The AT89S52 microcontroller has programmed to transmit the 4-bit data through the port signals P2.0 – P2.3, which are connected with data lines of HT12-E encoder. These data lines are known as the unique address of Institutions, where speed to be lowered. In this work, the encoder address lines are normally tied with logic 0 as it is a single module placed in the road of particular institution. The encoder then, transmits this information through Dout pin serially to the RF transmitter with appropriate synchronization bit. Upon receiving this information RF transmitter, transmit this information over the space. The typical foot coverage of the transmitter is 400 foot for the outdoor and 200 foot for the indoor. However we used this module in the outdoor only. The figure (3) shows the transmitter module placed in the pedestrian signal nearby the educational institution.

Figure 3: Transmitter module.
In the receiver side, the antenna output is connected to the input pin of STR – 433, which demodulate the incoming AM carrier, then outputted to decoder HT – 12 D, where the serial information about the zone is converted back to the 4-bit data. This data will be accessed by the microcontroller through the port signals P2.0 – P2.3 and then pulse width modulated (PWM); according to the zonal information the speed of the vehicle will be controlled. We used a DC motor in the laboratory to reduce the speed. The figure (4) shows receiver module with toy car, to be placed in the vehicle, developed in the laboratory for demonstration.

![Receiver module developed in the laboratory.](image)

**Conclusion**
This paper deals with 89S52 microcontroller with RF sensor based speed control of the vehicle at the Educational institution, which can help to decrease one of the major cause of fatalities due to the excessive vehicle speed. Aim of this paper was developed based on the application of microcontroller and RF modules. However practically, there is a need of speed measurement devices and controlling devices. Speed can be measured from the speedometer, but precision is limited to four pulses for one turn of the vehicle’s wheels, which gives insufficient resolution at low speeds. In order to obtain the high precision speed measurement differential Hall effect sensor could be used, which gives not only high precision and whose output easily processed by converting analog to digital form. To lower the speed, the throttle automation is required. The throttle can be controlled with an analogue signal generated with the automation circuit. Similarly automatic breaking system is required when automation system is failed. Although the experiments reveals that effective speed control, much more required for effective speed control system to meet the challenges exist in various situations.
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Design of remote EB metering system with Arm controller

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ABSTRACT
This paper emphasis the automatic remote EB metering system using the existing GSM technology to reduce the human intervention, in order to save invaluable man time and to reduce the cost. Though both analog and digital meters are widely used, in this work the existing analog reading meter with additional circuity of IR sensor is used for demonstration. Nowadays GSM network is not only used mere mobile conversation, its applications are countless. At the end of every month or the date programmed in the controller, the actual readings (units consumed) will be sent to the consumer by the SMS (Short Messaging Services). ARM microcontroller has been programmed to govern all these works. A prototype system has been developed for experimentation.

Introduction
The paper aims at instantaneous transmission of the quantity of power consumed as measured by the energy meter and also sensing any misusage by the consumer. The implementation of these automated systems (communication and security alert) is realized using ARM controller[1] with GSM technology[2]. In EB meters there are two types, analog meters and digital meters. The analog meters are mostly used in olden days and even it is used in many countries. These meter readings are calculated under the basis of the number of rotation made by the rotating disc. The digital meter is commonly used EB meters now a day. This meter works on the basis of the flash made by the LED and according to that the reading are calculated.

On approach of EB metering system is that enumerator has to go every home or industry with paper and pen to note the readings or should have any handheld devices. This approach seems the wastage of invaluable human time and it is tiresome. In [3], getting meter readings, using PSTN networks have been introduced. In another approach of remote metering system[4],[5],[6], wireless networks have been proposed. Some commercial remote metering system products use the internet for the data transmission. The MainsTalk[7] and Arehnet[8] use power line carrier(PLC ) technology to remove extra wiring for inlemet connection with the meter. In [9], Bluetooth technology has been proposed for remote metering.

In our idea we are using ARM micro controllers namely LPC2148 in both receiving and transmitting part and also in detecting faults and controlling security systems. The power measured by the energy meter is sensed using infrared sensor[10],[19] and given to the microcontroller for manipulation and storage purpose. The Wireless transmission is carried out using the GSM technology. The microcontroller in the receiver part (EB meter) had been programmed to sense/store the status of the IR sensor in order to count the rotation of the disc which in turn used to calculate the kilowatt-hour[11]. Whenever the date and time programmed comes, the ARM controller latch the number of units calculated for the month and send this information to GSM module namely SIM 300[12] and later same will be communicated to the consumer’s mobile through SMS. Remote meter can be used in residential apartments and industrial consumer where bulk energy consumed. The figure (1) shows block diagram of the modules used in transmission and reception.

Circuit Description:
The major hardware modules used in this work are 1. EB meter, 2. IR sensor, 3. GSM modem (SIM 300), 4. LCD, 5.

**Description of existing EB meter:**

Energy[13],[14] is the total power delivered or consumed over a time interval. Energy consumed is measured with the help of an energy meter. The induction type of energy meter[15] is used universally for measuring energy consumed in domestic and in industry purpose.

**Ferraris meter:**

Electricity is measured in kilowatts-hours. The Ferraris meter[16] is also referred to as an induction meter. Ferraris meters are in wide use due to their simplicity of design and low cost for mass production. The single-phase, watt-hour meters found in many homes are usually of this type. The meter has an electromagnet, called the stator, which consist of voltage coil and current coil. These coils are connected to the incoming line and react electro magnetically in proportion to the line voltage and current, or power. Meter readings may be displayed on dials, recorded in graphic form on chart[17], or transmitted electronically to digital read-out devices[18]. There are different ways to measure the rotation of the disc.

The old mechanical way is to let the disc drive a gear train connected to a series of dials that indicates the kilowatt-hour (kWh) reading. Sequence of the switching will determine the direction of the rotation. An alternative is to use Tram missive sensor, in which a slot on the disc will replace the dark tape to actuate the sensors. In this paper we have designed a prototype model with energy meter which is having a rotating disc mounted on a AC motor.

**IR sensor:**

An IR sensor capable of detecting a contrast between adjacent surfaces, such as difference in color, roughness, or magnetic properties. The simplest would be detecting a difference in color, for example black and white surfaces. Using simple optoelectronics, such as infrared photo-transistors, color contrast can easily be detected. Infrared emitter/detectors or photo-transistors are inexpensive and are easy to interface with a microcontroller.

Theory of the operation[19] is simple concept, consider the basic effects of light and what happens when it shines on a black or white surface. When light shines on a white surface, most of the incoming light is reflected away from the surface. In contrast, most of the incoming light is absorbed if the surface is black. Therefore, by shining light on a surface and having a sensor to detect the amount of light that is reflected, a contrast between black and white surfaces can be detected. Figure (2) shows an illustration of the basics just covered.

**GSM modem:**

GSM is a cellular network, which means that mobile phones connect to it by searching for cells in the immediate vicinity. There are five different cell sizes in a GSM network—macro, micro, Pico, femto and umbrella cells. One of the key features of GSM is the Subscriber Identity Module, commonly known as a SIM card[20]. The SIM is a detachable smart card containing the user's subscription information and phone book. This allows the user to retain his or her information after switching handsets.

Figure (3) shows a GSM modem is a specialized type of modem which accepts a SIM card, and operates over a subscription to a mobile operator, just like a mobile phone. From the mobile operator perspective, a GSM modem looks just like a mobile phone. When a GSM modem is connected to a computer, this allows the computer to use the GSM modem to communicate over the mobile network. While these GSM modems are most frequently used to provide mobile internet connectivity, many of them can also be used for sending and receiving SMS and MMS messages.

**Figure 3. SIM 300 GSM modem**

A GSM modem can be a dedicated modem device with a serial, USB or Bluetooth connection, or it can be a mobile phone that provides GSM modem capabilities.

A GSM modem exposes an interface that allows applications such as Netf SMS to send and receive messages over the modem interface. The mobile operator charges for this message sending and receiving as if it was performed directly on a mobile phone. To perform these tasks, a GSM modem must support an "extended AT command set" for sending/receiving SMS messages.

A GSM modem is a wireless modem that works with a GSM wireless network. A wireless modem behaves like a dial-up modem. The main difference between them is that a dial-up modem sends and receives data through a fixed telephone line while a wireless modem sends and receives data through radio waves.

A GSM modem can be an external device or a PC Card / PCMCIA Card. Typically, an external GSM modem is connected to a computer through a serial cable or a USB cable. A GSM modem in the form of a PC Card / PCMCIA Card is designed for use with a laptop computer. It should be inserted into one of the PC Card / PCMCIA Card [21] slots of a laptop computer.

Like a GSM mobile phone, a GSM modem requires a SIM card from a wireless carrier in order to operate. In addition to the standard AT commands, GSM modems support an extended set of AT commands. These extended AT commands are defined in the GSM standards. With the extended AT commands, one can do things like:

• Reading, writing and deleting SMS messages.
• Sending SMS messages.
• Monitoring the signal strength.
• Monitoring the charging status and charge level of the battery.
• Reading, writing and searching phone book entries.

The number of SMS messages that can be processed by a GSM modem per minute is very low -- only about six to ten SMS messages per minute.
AT commands are instructions used to control a modem. AT is the abbreviation of ATention. Every command line starts with “AT” or “at”. That’s why modern commands are called AT commands. Many of the commands that are used to control wired dial-up modems, such as ATD (Dial), ATA (Answer), ATH (Hook control) and ATO (Return to online data state), are also supported by GSM/GPRS modems and mobile phones.

Features of LPC 2148 ARM microcontroller:
The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine the microcontroller with embedded high-speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. LPC2141/42/44/46/48 are ideal for the applications where miniaturization is a key requirement. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI to I2C-bus and on-chip SRAM of 8 kB to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and other applications.

Working Principle:
An IR Sensor is fixed across the EB meter armature and it is connected to the port of the Arm controller. A small black trap is placed in the armature of the EB meter for counting the rotation of the meter. IR sensor consists of IR LED and phototransistor. IR LED is a transmitter and phototransistor is a receiver. Normally the output of the IR sensor is in static high, whenever the black trap crosses the IR sensor a static low signal is provided to the microcontroller and microcontroller assumes the pulse as a count or unit.

Here the LCD is connected at the port 1 and used to display the units of the meter and the date. GSM modem is connected with the serial communication pin of the microcontroller. The TX and RX pin of the GSM modem connected to the arm controller for the serial communication. MAX 232 IC is used for establishing the serial communication between the controller and the modem. An ALP has been written for counting the EB meter reading for 30 days and to send the message to the consumer at the end of the month. In this project two switches are used to feed the EB count and date manually. When the microcontroller read the date as 30th of the month, it will communicate with GSM modem for sending the SMS using AT commands. GSM modem has a slot for SIM card at the backside of the modem SIM card number is stored in microcontroller memory to send the SMS. The message displays the user name, amount of unit consumed and total bill amount. Here limit switch is used for security purpose. If the user opens the EB box, the microcontroller will block the all operation and send the alert SMS to the electricity board. The operation will resumes after the EB person inspects the total box and instead of password receives the SMS with corresponding billing amount with account number. After the completion of one month, the microcontroller starts to reads the data from the EB meter for the consecutive months.

Experiment and Analysis:
We have developed the prototype system in our lab, and several experiments have been conducted. We have developed one metering system at the receiver end, and programmed the ARM controller to latch the EB meter readings for every unit. A specific register was used to hold the units consumed and later this data sent to the GSM modem with appropriate AT commands for every 30 days. GSM modem SIM 300 sent SMS to the consumer mobile with the number of units consumed. The delivery acknowledgement was monitored. In our experiment, 97% SMS was received successfully in one attempt. If failure, due to switch off and un coverage area, 3% was achieved in second and third attempt. Figure (4) shows a graph plot of the response time of the acknowledgement signal.

Conclusion:
In this paper, EB metering system with the control of ARM controller is proposed, consumption units intimated to the consumer through SMS. The various functional units of the system were described. We have received the expected experimental results. Further this work can be continued, and billing could be done on the internet by developing the software module. In order to get the faster data General Packet Radio Service (GPRS) modem could be used.

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FPGA Based SOC for Railway Level crossing Management System

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Abstract- It is to develop the FPGA based, System on Chip (SOC) to implement the safety system in Railways for level crossing. For the communication RF module[1] with the coverage of large distance, it is outdoor line-of-sight: up to 15 miles (24 km) with high gain antenna is used. RF Transceiver has many salient features[2], such as, Advanced Networking & Security, True peer-to-peer (no "master" required) communications, Packet-to-point and point-to-multipoint topologies supported, Continuous RF data stream up to 9600 bps. No configuration required for out-of-the-box and Support for multiple data formats (parity, start and stop bits, etc.). An article authored by Mr. R.K. Verma, Chief Engineer, Indian Railways exposes the Corporate Safety Plan [3] of reduction of accidents on Indian Railway (IR) by the year 2012-13. In which, he stated that Collisions of the Trains can be completely eliminated. Derailments can be reduced by 60% and fire accidents by 80%. But, he has not given assurance by the year 2012-13. In which, he stated that Collisions of the Trains can be completely eliminated. Derailments can be reduced by 60% and fire accidents by 80%. But, he has not given assurance. Therefore to avoid this, a well designed sophisticated electronic applications [6]. The objective of the work is to develop the FPGA based, System on Chip (SOC) to transmit and receive the RF signals to the safety of public at unmanned level crossing.

Figure 1 - Proposed system for the design of SOC with RF Transceiver.

Whenever the train arrives towards level crossing 15 Km ahead, the RF transmitter transmits the RF signal contains information bits to the receiver. Upon receiving the RF signal, SOC provides the warning signal to the Road crosser and this helps to reduce accidents at level crossings by giving adequate warning to road users.

The figure (1) illustrate the proposed system. The Train, and another transceiver mounted at the unmanned level crossing. The figure (1) illustrate the proposed system.

I. INTRODUCTION

Nowadays, Field Programmable Gated Arrays (FPGA)[4-5] based technology is very popular in designing embedded system. Specifically, in recent years, with the development of FPGA, wireless communication technology, RF technology have become hot technology in the field of electronic applications [6]. The objective of the work is to develop a system on chip to transmit and receive the RF signals to the safety of public at unmanned level crossing. Instead of SOC, microcontroller can be used, but SOC is designed specifically to govern and easily synchronize with RF Transceiver. An RF transceiver is mounted on the top of the Train, and another transceiver mounted at the unmanned level crossing. The figure (1) illustrate the proposed system.

II. FPGA AN OVERVIEW

A field-programmable gate array (FPGA) is an integrated circuit. It is designed to be configured by the designer after manufacturing, hence it is field-programmable. The FPGA configuration is generally specified using a hardware description language (HDLs), such as VHDL and Verilog HDL. FPGAs can be used to implement any logical function that an ASIC (Application Specific Integrated Circuits) could perform. FPGA has the ability to update the functionality after transformation, partial re-configuration of a portion of the design [11] also possible and it is low cost.

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FPGA Based SOC for Railway Level crossing Management System

In FPGAs programmable logic components are readily available known as logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be connected together. Logic blocks can be configured to perform any complex combinational/Sequential functions, or merely simple logic gates like AND, OR, NOT and XOR. In most of the FPGAs, the logic blocks also consists memory elements, which may be simple one bit storage or more complete blocks of memory.

In addition to digital functions, some FPGAs have analog functions. The most common analog function is programmable slew rate and drive strength on each output pin. Another relatively common analog function is differential comparators on input pins designed to be connected to differential signaling channels. Some of mixed signal FPGAs have integrated Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. In the year 2010, an extensible processing platform was introduced for FPGAs that fused features of an ARM high-end microcontroller with an FPGA IC to make FPGAs easier for designing embedded system. By incorporating the ARM microcontroller based platform into a 28 nm FPGA family, the extensible processing platform enables system architects and embedded software developers to apply a combination of serial and parallel processing to address the challenges they face in designing today’s embedded systems, which must meet ever-growing demands to perform highly complex functions. By allowing them to design in a familiar ARM environment, embedded designers can benefit from the time-to-market advantages of an FPGA platform compared to more traditional design cycles associated with ASICs.[12][13][14].

2.1 FPGA micro Architecture Block Diagram

The FPGA micro Architecture Block Diagram with its functional blocks is shown in figure (2)

Figure 2 - The FPGA micro Architecture Block Diagram

In the FPGA micro architecture has the following functional blocks, listed below
- Finite State Machine (FSM)
- RS 232 core
- On-chip Memory Blocks
- PLL
- PWM Generator

2.2 Finite State Machine (FSM)

FSM plays a vital role in the design, has nine states (exclude RESET and END states) of action to be carried out while functioning. Such as
- Wait for RI (receiver interrupt signal)
- Read the data from RF receiver
- Forward to data processing unit
- Enable PWM signal generator unit for generate the pulse signal close the gate step by step
- Enable red signal and buzzer
- Wait for train pass information from RF transceiver
- After receive the signal enable the PWM signal open the gate
- Enable green state
- Go to first state

The figure (3) shows the state machine diagram as follows:

Figure 3 - State machine diagram

2.3 RS232 Core

In this functional unit the asynchronous communication is enabled. Whenever the RF Signal comes from the Transmitter, it receives and communicates with FSM at a speed of 9600 bits/sec. (baud). Figure (4) illustrates the RS-232 transmitter module

Figure 4 - RS-232 transmitter module

It works like that:
- The transmitter module takes an 8-bits data, and serializes it (starting when the "TxD_start" signal is asserted).
• The "busy" signal is asserted while a transmission occurs. The "TxD_start" signal is ignored during transmit time.

The RS-232 parameters used are fixed: 8-bits data, 2 stop bits, no-parity.

2.4 On-chip Memory Blocks

On-chip memory can be divided into number of blocks, based on the requirements. Our case, a data memory was created and used for storing of information, such as Train number, Crossed time.

2.5 Phase Lock Loops (PLL)

The PLL block provides general purpose clocking with clock synthesis and phase shifting as well as external outputs for high-speed differential I/O support. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), FSM, and embedded memory blocks. The processor (FSM) was programmed to generate 9600 baud rate for RS232 core. The global clocking frequency is divided in the PLL. The simple calculation to get the baud rate as 9600 is:

\[
\text{Global clocking frequency} = 100 \text{MHz} \\
\text{PLL output} = \frac{100 \times 10^6}{2} = 50 \times 10^6 \text{Hz} \\
\text{Desired frequency} = \frac{50 \times 10^6}{9600} = 5208.33 \text{ Hz}. 
\]

2.6 Remote System Upgrades

Remote system upgrade capability in Cyclone II [9] devices allows transformation of system upgrades from the remote location is possible. In order to upgrade the system, Soft logic either the Nios II embedded processor or user logic can be used in a Cyclone II device to download a new configuration image from a remote location. It stores the program coding in the configuration memory. The dedicated remote system upgrade circuitry initiates a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process. It means Cyclic Redundancy Check is possible. This check facilitates to recover from an error condition by reverting back to a safe configuration image, also provides error status information. This feature supports both in serial and parallel flash configuration.

III. INTERFACING RF MODULES

3.1 433 MHz RF Transmitter STT-433

It is low cost RF transmitter used widely in the wireless communication system. Its operating voltage ranges from 1.5 to 12V DC supply. The transmitter employs a SAW stabilized oscillator, which ensures accurate frequency control for the best range of performance. It is small size, consumes 1mA at 3V. Its minimum data rate 200 bps and maximum is 3K bps. Also it has good temperature adaptability (from -20°C to + 60 °C).

3.2 433 MHz; RF Receiver STR-433

The receiver module requires only antenna and no need of any external RF components. It is low cost device, whose operating voltage is 5V and the operating current is typically 3.5 mA and requires no external parts. Receiver frequency is about 433.92 MHz, whose sensitivity is -105dBm. Data received in the rate of 3 K bits/s.

IV. GEAR MOTOR ASSEMBLY

In our work, to open and close the gate NR-DC-ECO DC geared motor [15] is used. It is simple weightless device and easy to interface with SOC using driver circuit. The construction of the motor has the sophisticated technology. In the motor gears are fixed on hardened steel spindles. These spindles rotate between bronze plates which ensures noise free running. It is DC operated device able to work with 4 to 12 V, and its speed is 30 RPM.

V. FUNCTIONING OF THE SYSTEM MODEL

The core embedded system in FPGA works as the processor. It is used to control the communication device 433 MHz RF Receiver STR-433. RF transmitter mounted on the top of the train emits series of the bit packets containing the information about the train to be crossed. Upon the receiving RF data packets, processor save the information about the train, the time to be crossed and enables the buzzer to give the warning level crosser. Also it activates the motor to close the gate. After the train crossed over place, it stops the buzzer and run the motor in the reverse direction to open the gate. In the laboratory a prototype system was implemented successfully with RF transceiver and gear motor.

VI. RESULT AND DISCUSSION

The working model developed in the laboratory produced the output shown in the figure(5). It is the synthesized RTL view of the functional blocks.

Figure 5 — Synthesize view of the Functional blocks.
Figure (6) shows the Chip planner view of the Functional blocks. It reveals that the number of logic elements used for the functional blocks of SOC are 90/32,216 (It is less than 1%). Other utilizations are

- Total combinational functions - 90/32,216 (< 1%)
- Dedicated logic registers - 55/32,216 (< 1%)
- Total registers - 55
- Total pins - 5/475 (1%)

Figure 6 - Chip planner view of the Functional blocks

VII. CONCLUSION

In the laboratory a prototype system was implemented successfully with RF transceiver and gear motor. This work is more useful in railway level crossing management, as it is required to avoid the railway level crossing fatalities. Now railway level crossing fatalities are more common, in almost all countries. Design of SOC in FPGA for wireless communication system with RF transceiver embedded system, provides better wireless data transmission. It is low cost system architecture. But, if needed more such SOCs, we have to go for ASCI (Application Specific Integrated Circuits) based SOCs, because FPGA is most suitable for low volume of ICs. This project can be further developed and can be used for real time application. This prototype system was successfully implemented and tested in Altera cyclone II device EP2C35F672C6.

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ABSTRACT
In the modern world, the information that could benefit the individual / a group also can be used against such individual or group. Encryption is the technique of converting a plaintext (original data packet) into cipher text (encrypted message) which can be decoded back into the original message. There are several types of data encryption schemes available which form the basis of network security. Our proposed work deals with the security based wireless communication system, with the NIOS-II soft core processor. Security in wireless communication is most essential, especially where hacking and tampering are threats of the data packet. Hence introduction of suitable security bits (Key) with the actual data packet is most important aspect in wireless communication to avoid such threats. It is really a significant and interesting area for the researcher. In this work, the data encryption standard technique is used for the safety transmission and reception, and implemented it successfully with the NIOS-II soft core processor.

Keywords
Wireless communication, NIOS-II soft core processor, FPGA, SOC, Data Encryption.

1. INTRODUCTION
In recent years, the wireless communication plays a vital role in industries, home and government departments [1]. It is the emerging field in electronic communication. One example of its growth is cellular systems. Cellular systems have experienced high growth over the last decade. Wireless networks currently replace wired networks in many homes, companies and other campuses. Many new applications, including smart homes, wireless sensor networks, automated factories and high ways, and remote telemedicine, are emerging from research ideas into concrete systems [2]. Although the wireless communication is having numerous applications, hacking and tampering the data packet are also quite common. There are plenty of techniques of hacking the data; especially in wireless communication is underway. Such hacking methods [3] are: 1. Diverse hacker attack methods, 2. Social Engineering, 3. Social spying, 4. Stuffing and more. In order to avoid hackings and tampering the data packets a suitable encryption technique has to be implemented. There are plenty of methods can be used to encrypt data packets, all of which can easily be implemented through software, but not so easily decrypted when either the original or its encrypted data stream are unavailable. (When both source and encrypted data are available, code-breaking becomes much simpler, though it is not necessarily easy). The best encryption methods have little effect on system performance (Slowing the system), and may contain other benefits such as data compression [4]. We have used the data encryption technique to implement the secured data transmission and reception with NIOS-II soft core processor [5]. It is having many features such as RISC (Reduced Instruction Set Computer) architecture, 32 bit processor, and its architecture consist of separate instruction and data bus (Harvard architecture). The SOPC (System on programmable chip) builder is a tool used in conjunction with the Quartus II CAD tool Software [6]. It allows the designer to easily create a system based on the NIOS II processor, by selecting the desired functional units and specifying their parameters. The NIOS II processor is a configurable soft core processor. Configurable means that can be added or removed any features or resources of the processor on the basis of performance or cost wise. Soft core means the processor core is not fixed in silicon chip, but can be targeted to any Altera FPGA family.

This paper is organized as 1. Overview, 2. Implementation, 3. Result and analysis, and 4. Conclusion.

2. OVERVIEW
Our approach to achieve the aim of the proposed work is based on Altera NIOS II embedded soft core processor that provides a highly configurable device and having excellent versatility. We have used Altera Cyclone Field Programmable Gate Array (FPGA) and its peripherals to make the design to be constructive. A well known Data Encryption Standard (DES) Algorithm[7] is chosen for Encryption for secured data transmission. The evaluation results obtained from the experiment are shown for analysis and verification of our design. The figure (1) shows block diagram of the proposed work. Referring the block diagram, the functional modules are 1. Various Wireless sensor outputs, usually analog signals (The Electrical output), 2. A/D converter, 3. Cyclone II FPGA, 4. GSM modem.
2.1 Analog to Digital Converter

Analog to Digital converter [8] is configured with processor is 8-bit converter, compatible with ADC 0809. The 8-channel (Inputs IN0 to IN7) multiplexer can directly access any of 8 single ended analog signals to be transmitted with the set of address lines A, B, C. The clock chosen for conversion 600Khz. The ADC 809 also having many desirable features, such as no zero or full scale adjust required, and 0V to 5V input range with single 5V power supply.

2.2 NIOS Embedded processor

The NIOS II Embedded processor is a general purpose configurable Soft core processor [9,10]. In practice, most FPGA designs implement some extra logic in addition to the processor system. The processor could be virtually realized on any of an Altera FPGA by using a System On a Programmable Chip (SOPC) builder. NIOS II embedded processor is having Custom instructions; means Nios II instructions, user-defined instructions accept values from up to two 32-bit source registers and optionally write back a result to a 32-bit destination register. Nios II families are 1. NIOS II/F (fast), 2. NIOS II/S (standard), and 3. NIOS II/E (economy). Any one of these can be used for design, depends on the requirement.

2.3 DE2 development board

DE2 development board consists of Cyclone II EP2C35F672C6 with EPCS16 16-Mbit serial configuration device, and many standard peripherals. It provides a high performance, low cost design with modern Altera devices and tools. With Quartus II CAD tool, the designer can develop hardware design using HDLs in the on board FPGA. A set of memory such as 8 MB SDRAM, 512 KB SRAM are also available. Hence, DE2 development board is much suitable platform for running NIOS II soft core processor. The figure (2) shows Altera’s DE2 development board.

2.4 RS-232 Serial Interface

An RS-232 interface [12] has many characteristics, 2. It allows bidirectional full-duplex communication, 3. It can communicate at a maximum speed, at the rate of 10Kbytes/s. Three are important pins for communication, they are RxD (Receive Data- Pin No. 2), TxD (Transmit Data- Pin No.3) and GND (Ground pin No. 5).

2.4.1 Serial communication

Data is sent on bit by bit basis, that is one bit at a time; a single wire is used for each direction. Since computers usually need at least several bits of data, the data is "serialized" before being sent. Data is commonly sent by chunks of 8 bits. The LSB (data bit 0) is sent first, the MSB (bit 7) last.

2.4.2 Asynchronous communication

This interface uses an "asynchronous" protocol. In asynchronous data transfer, handshake signals are used for testing the readiness of the receiver. In our case the RS232 is
function in the mode. In this mode of transmission, the speed and format has to decided before start the transmission. The TxD line sends logic “1” as long as the line is idle. The start bit (logic “0”) to be send before each byte of transmission. After the “start”, data comes in the agreed speed and format, so the receiver can interpret it. The stop bit is usually logic “0”.

The common baud rates of RS 232 Serial interface are 1200, 9600, 38400, and 115200. The speed can be easily calculated as, for example if the baud rate is 115200. \( T = \frac{1}{115200} = 8.7\mu s \). If 8-bits data to be transmitted, that lasts 8 x 8.7\( \mu s = 69.6\mu s \). But in the Asynchronous format of transmission, each byte requires an extra start and stop bit, so actually need of 10 x 8.7\( \mu s = 87\mu s \). That translates to a maximum speed of 11.5KB/second.

2.5 SIM 300 GSM modem

The figure (3) shows SIM 300 GSM modem. A GSM modem exposes an interface that allows applications such as NowSMS to send and receive messages over the modem interface.

2.6 Data Encryption Standard Algorithm

Data Encryption Standard Algorithm is chosen to achieve a good secured data transmission \([14,15]\). The implementation of this algorithm has been done with C++ language. A DES key consists of 64 binary digits of which 56 bits are randomly generated and used directly by the algorithm. In this technique, data can be recovered from cipher (Encrypted output) only by using exactly the same key used to encrypt it. Unauthorized recipients of the cipher who know the algorithm but do not have the correct key cannot derive the original data algorithmically. It is also possible to retrieve the original data by deciphering the text with original key and algorithm. A standard algorithm based on a secure key thus provides a basis for exchanging encrypted computer data by issuing the key used to encrypt it those authorized to have the data. The security level has been proven to be competent for efficiently defending the linear and differential cryptanalysis. The characteristics of this algorithm make it appealing security scheme for our proposed work.

3. IMPLEMENTATION

For transferring secured data transmission through wireless, we have designed NIOS II processor with necessary peripheral interface. The entire implementation process is thus assigned to two stages: 1. Hardware implementation, and 2. Software Implementation.

3.1 Hardware Implementation

In our design, we have effectively utilized the resources available in the Altera NIOS II embedded processor technology. In the laboratory we have taken the analog data which is then successfully converted to equivalent binary bits. These are the output bits of the ADC, which is 64-bit known as plain text. With these binary bits (Plain text), C++ program was executed in the NIOS II processor on DE2 development board to get the cipher text for secured data transmission, and then the cipher text was transmitted serially with RS 232 serial interface to the SIM 300, for transmitting the secured data (Cipher text) over the space. At another end the cipher text was received successfully with another SIM 300, and then the cipher text was deciphered. Since this process of communication is purely asynchronous, the excellent configurable and programmable properties of the NIOS II processor enable us to simply implement the encryption and decryption process on a single DE2 development board significantly reducing the cost of the platform. The core of the DE2 development board consists of Cyclone II EP2C35F672C6 with EPCS16 16-Mbit serial configuration device. The basic peripherals chosen are UART controller, A/D controller, On chip memory, I/O controller, and a timer in SOPC builder for the lowest Logic Elements (Les) consumption. The figure (4) Shows how the NIOS II soft core processor with the necessary peripherals are implemented in FPGA. The completed SOPC design is then downloaded via JTAG UART to DE2 Board.
Having built up the hardware, the Data Encryption Standard (DES) algorithm needs to be programmed in software. The software development environment of NIOS II processor that called NIOS II Integrated Development Environment (IDE) is based on the C/C++ compiler. The program was written in C++, and the specifications of DES carefully coded with suitable parameters.

The algorithm is designed to encipher and decipher blocks of data consisting of 64 bits under control of a 64-bit key (the left most bit of a block is bit number one). Deciphering must be accomplished by using the same key as for enciphering, but with the schedule of addressing the key bits altered so that the deciphering process is the reverse of the enciphering process. A block to be enciphered is subjected to initial permutation IP; then to a complex key-dependent computation and finally to a permutation which is the inverse of the initial permutation IP'. The key-dependent computation can be simply defined in terms of a function f, called the cipher function, and a function KS, called the key schedule. The figure (5) shows the illustration details of the DES.

**DES algorithm**

![DES algorithm](image)

**Input:**
- T: 64 bits of clear text
- k1, k2,..., k16: 16 round keys
- IP: Initial permutation
- FP: Final permutation
- f(): Round function

**Output:**
- C: 64 bits of cipher text

**Algorithm:**
- T' = IP(T), applying initial permutation
- (L0, R0) = (R0, L0 ^ f(R0, k1))
- (L2, R2) = (R1, L1 ^ f(R1, k2))
- ...
- C' = (R16, L16), swapping the two parts
- C = FP(C'), applying final permutation

where ^ is the XOR operation.

1. The round function f(R,k) is defined as:

**Input:**
- R: 32-bit input data
- k: 48-bit round key
- E: Expansion permutation
- P: Round permutation
- s(): S boxes function

**Output:**
- R' = f(R,k): 32-bit output data

**Algorithm**
- X = E(R), applying expansion permutation and returning 48-bit data
- X' = X ^ k, XOR with the round key
- X'' = s(X'), applying S boxes function and returning 32-bit data
- R' = P(X'), applying the round permutation

1. The S boxes function s(X) is defined as:

**Input:**
- X: 48-bit input data
- S1, S2,..., S8: 8 S boxes - 4 x 16 tables

**Output:**
- X' = s(X): 32-bit output data

**Algorithm**
- (X1, X2,..., X8) = X, dividing X into 8 6-bit parts
- X' = (S1(X1), S2(X2), ..., S8(X8))
- where Si(Xi) is the value at row r and column c of S box i with
  - r = 2*b1 + b6
  - c = 8*b2 + 4*b3 + 2*b4 + b4
- b1, b2, b3, b4, b5, b6 are the 6 bits of the Xi

4. RESULT AND ANALYSIS

In this work, the designed System on chip (SOC) on NIOS-II processor successfully implemented. The resultant hardware configuration implemented, as shown in the figure (6) as follows.
5. CONCLUSION

Based on our proposed work hardware implementation platform, we suggest a novel methodology for transmitting wireless data. This method takes into account the level of security, execution speed, memory usage and power consumption altogether, all of which are desired properties for wireless data transmission. With the comprehensive consideration of all these factors for certain application in wireless communication could be found with high efficiency and low cost. This paper has proposed a comprehensive approach of secured data transmission in wireless communication, and the feasibility of the design has been studied. Certain questions are to be answered in terms of speed in the future study.

REFERENCES


Figure (6)- RTL View of the NIOS II processor implementation

Test conducted on the prototype work by giving the analog data (Thermistor output) and transmitted successfully with encryption through GSM modem SIM 300. Also we have received appropriate message as output. The NIOS II/e (economy core) is designed to minimize the cost of the design. In this work, the total logic elements consumed only 20%, total logic functions are used only 17%. Other parameters are used in the work as shown in the table (1).

<table>
<thead>
<tr>
<th>Family</th>
<th>Cyclone II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>EP2C35F672C6</td>
</tr>
<tr>
<td>Total Logic elements</td>
<td>6,574 / 33,216 (20%)</td>
</tr>
<tr>
<td>Total combinational functions</td>
<td>5,557 / 33,216 (17%)</td>
</tr>
<tr>
<td>Dedicated Logic registers</td>
<td>3,524 /33,216 (11%)</td>
</tr>
<tr>
<td>Total registers</td>
<td>3641</td>
</tr>
<tr>
<td>Total pins</td>
<td>429 /475 (90%)</td>
</tr>
<tr>
<td>Total virtual pins</td>
<td>0</td>
</tr>
<tr>
<td>Total memory bits</td>
<td>387,584/483,840 (80%)</td>
</tr>
<tr>
<td>Embedded multiplier 9-bits</td>
<td>4/70 (6%)</td>
</tr>
<tr>
<td>Total PLLs</td>
<td>2/4 (50%)</td>
</tr>
</tbody>
</table>

Table (1) - consumption details of NIOS II core processor
Designing Of Reconfigurable MPNOC On FPGA For Processing The Wireless Sensor Networks

*R.Ramachandran, J. Thomas Joseph Prakash

Abstract - Designing of system on chip with the current algorithm and design methodology cannot meet the requirements of accommodating billion-transistor area in VLSI technology. There is a need of plat form based design and computing system design. It is to implement FPGA based reconfigurable Multiple Processor Network on Chip (MPNOC) which consists of Multiple Processing Units (MPUs), Communication controller (CC) and Memory Units (MU). The processing units are System on Chips; they are communicated each and other or connected with Routers. In this work NoC designed for processing the signals of wireless sensor networks, such as GPS, RF sensor, RFID, and Zigbee outputs. The proposed System was thus designed and simulated in ALTERA IDE's platform. In this work, the SOPC Builder component editor has been used to configure the node elements and to create Custom network interface component. In order to implement the designed NoC in FPGA chip, Altera Quartus II CAD tool was used, which compiles HDL written for configuring NoC, also generates RTL View and timing analyzer for the main components.

Key words - MPNoC, SoC, reconfigurable Network on Chip, Wireless system, WSN

I. INTRODUCTION

Wireless sensor networks (WSNs)\cite{1,2,3} consist of a large number of distributed communicating resource-constrained devices deployed to accomplishing monitoring and control goal. WSNs have some unique features, specifically handling the signals in terms of scale, communication pattern, resource level and mobility. E.g, they are typically orders of magnitude larger \cite{4,5} than other networks. The one more important task of the WSN is to manage the network traffic, usually it is asymmetric – mainly from sensor nodes to base stations. As a result, base stations are responsible for handling a large amount of data. Based on recent advances in WSN technology, the base stations will have must have built-in computational abilities to be capable of dealing with the collected data in large-scale WSNs. In a platform based system design Network on Chip (NoC)\cite{6,7,8} plays a vital role in the field of embedded system, and it is the replacement of bus based system architecture. The NoC architecture consists of Processing units, communication controllers and memory units with several routers. The routers are actually connected with one or more processing units (PU), also with neighboring routers. The NoC is thought to be future on chip interconnection. The concept of reconfigurable computing system means the processor with reconfigurable hardware. These system are having the feature of higher performance than general-purpose processors, also seems that more flexible than application specific integrated circuits (ASICs). Today Field Programmable Gate-arrays (FPGAs) are widely used in developing the applications of any sector, because of its low cost, low power consumption of novel reconfigurable hardware and high flexibility. Specifically the possibility of real-time reconfiguration of the hardware, FPGA architectures enables to introduce new ideas for adaptive hardware. Modern FPGAs support the partial dynamic run-time reconfiguration; this is the additional advantage of developing future applications demanding adaptive and flexible hardware. In this work we present network on chip concept for Wireless Sensor network whose architecture is tailored specially for handling information at wireless sensor network. NoC is intended to replace conventional processors in base stations and it can bring new levels of performance in information processing. This is the first attempt at optimizing this task and Results show that the novel architecture is at least 10 times faster than an architecture based on traditional RISC processor. The hardware/software code-design is a popular approach for accelerating various complex Algorithms and similar software applications. The time critical portion of the data processing algorithms can be implemented using hardware accelerator to reduce the processing time. FPGAs provide ideal template for run-time reconfigurable design. This paper is organized as follows 1. Related Work, 2. Proposed Network on Chip System Architecture, 3. Functional Description, 4. Implementation and Result Analysis, 5. Conclusion.

II. RELATED WORK

Wireless Sensor network plays vital role in monitoring and processing the information of the area or system. In which the studies particularly aimed at the processing information. Chu et al\cite{9} introduce general information representation architecture for designing distributed inference algorithm in WSNs. The architecture comprises a graphical information representation with processing mechanisms guided by sensor...
Designing Of Reconfigurable MPNOC On FPGA For Processing The Wireless Sensor Networks

evidence and provides global view of the set of computations occurring in the system. In [10], Ganessan et al. describes the Dimentions, a system provides a unified view of data handling in sensor networks. Here, Dimension incorporates long term storage, multi resolution data access and exploits spatio-temporal correlation in sensor data. In [11], Andre Motael et al. describes Wireless Sensor Network Processor (WISENEP), which is ASIC based processor. It is to develop FPGA based MPNOC for processing Wireless sensor Networks to optimize the information processing at base station.

III. PROPOSED SYSTEM

The Figure 1 illustrates proposed NoC, consists of heterogeneous processing elements connected in mesh network topology.

![Figure 1: proposed NoC](image)

The NoC module is designed in such a way to meet the requirements of the high speed application. In order achieve the speed, each processing units are connected with 4x4 router, which replace the bus for information sharing with other processing units, or communication controller or memory units. Modules programmed to construct the NoC system, are configured in field programmable gate array (FPGA), because it has reconfigurable property to meet the dynamically changing system demands. NoC framework contains of following components. They are processing unit, memory controller, serial communication controller, router. Each module in the NoC framework perform the following tasks:

- Decode the bit stream received from the network interface into the proper packet’s fields
- Update the information stored on the memory on each received packet data; and
- Perform the computations on these information and define proper actions.

MPNOC is so designed to govern the data and to process it effectively.

The Processing units are connected to each other via mesh topology and use Wormhole (WH)[12] switching for message forwarding. Processing core (units) in each node consists of heterogeneous processing elements, such as state machine based CPU, A/D controller, serial communication controller and on-chip memory.

IV. PROCESSING UNIT (SOFTCORE PROCESSOR)

ATmega103(L) AVR core processor, which has many features, such as low-power, CMOS, 8-bit microcontroller based on the AVR RISC architecture. The AVR core is based on an enhanced RISC architecture that combines a rich instruction set with 32 general purpose working registers. The ATmega103(L) AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/ simulators. The RTL view of softcore processor is shown in Figure 2, and it is executed on the task based Finite state machine is shown in figure 3. Softcore processor process the node data and send to memory controller and stored in EEPROM.
V. COMMUNICATION CONTROLLER

The communication controller is another important node in the design which consists of

- UART
- Packet classifier
- Router

![Block diagram of communication controller](image)

The decision to forward the data through router to the specified node. The router switches the data to the appropriate node.

VI. I2C CONTROLLER

I2C memory controller module used to interface I2C based EEPROM. In this system, I2C based EEPROM memory used for store the node values. I2C is a two-wire, bidirectional serial bus it has two data line called SDA(serial data) and SCL(serial clock). It supports three modes of operation: I2C master controller, I2C slave controller, and an 8-bit parallel I/O (PIO) slave device. Three I2C bus transmission speeds are supported: 100 Kbps (normal), 400 Kbps (fast), and 3.4 Mbps (high speed).

VII. NETWORK INTERFACE MODULE

Network interface (NI) is an interface between network router and processing unit. It packetizes data sent by a directly connected processing unit and transmits the packet through the network through the router. Besides, it receives other packets sent by other processing unit through the router, de-packetizes the received packets and sends the data to the directly connected processing unit.

VIII. 4X4 ROUTER ARCHITECTURE

The figure 5 shows the block diagram of 4 x 4 router architecture, which consists of FSM based control logic, FIFO, small cross bar switch, five ports east, west, north, south and local port and a central cross point matrix. Each port has its input channel and output channel. Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The movement of data from source to destination is called switching mechanism. The packet switching mechanism is used here, in which the flit size is 8 bits. Thus the packet size varies from 8 bits to 120 bits. Every link in the network is full duplex, i.e., two messages can simultaneously travel on the link in opposite directions. A link is available for communication if its associated channel is available to accept the packet. A READY and SEND signal is used to communicate between adjacent nodes. Whenever the channel is busy it informs this to every adjacent nodes by setting the READY signal low.
A. Input channel

Figure 6 shows the block diagram of the input channel of the router.

There is one input channel at each port and each has its control and decoding logic. It consists of three main parts i.e. FIFO, FSM, XY logic. FIFO is used as input buffer to store the data temporarily. The size of FIFO is 8 bits and depth is of 16 bits. The first 8 bits are the header which consists of coordinates of destination path. In this way the size of packet varies from 8 bits to 120 bits. The status of FIFO decides the communication can start or not. If the FIFO is empty the data can be written in it and communication can start. If FIFO is full, data can be read or can be forwarded to its destination router. Inside the router Grant/Acknowledgement signals are used to access the FIFO. The read and write operation of FIFO is controlled by FSM. FSM controls the read and write operation of FIFO according to its status. If FIFO is empty or having enough space to store the data, FSM will give acknowledgement signal in respect to the request coming from the input channel, thus write operation starts. If FIFO is full or not having enough space to store the data, FSM will give acknowledgement signal in respect to the request coming from the input channel, thus write operation starts. When FIFO is full, FSM will send request to other router, if grant signal is received by it, then read operation starts and continues until grant signal goes low or FIFO empties. Thus empty status of indicates the end of communication.

B. Routing method

XY routing first routes packets horizontally, towards their X coordinate, and then vertically, towards their Y coordinate. XY logic is commonly used in NoCs XY logic is the deterministic logic which analyses the header of data and send it to its destination port. The first four bits of the header are the coordinates of destination port. In XY logic a comparator is used which compares the header of the data to the locally stored X and Y coordinate and send the packet according to its destination address.

C. Output channel

Each port of the router contains one output channel which has its control and decoding logic. It also consists of three parts i.e. FIFO, FSM and arbiter. The Figure 7 shows the block diagram of output channel.

FIFO and FSM are same as in input channel but in place of XY logic, arbiter is used in output channel. FIFO in output channels used as output buffer to store the data temporarily. FIFO is of size 8 bits and its depth 16 bits. The first 8 bits are the header which is the coordinates of destination router. Thus size of the packet varies from 8 bits to 120 bits. The status of FIFO decides the communication can start or not. If the FIFO is empty the data can be written in and communication can start. If FIFO is full, data can be read or can be forwarded to its destination router. Inside the router the Grant/Acknowledgement signals are used to access the FIFO. The read and write operation of FIFO is controlled by FSM. FSM controls the read and write operation of FIFO according to its status. If FIFO is empty or having enough space to store the data, FSM will give acknowledgement signal in respect to the request coming from input channel, thus write operation starts. If FIFO is full or not having enough space to store the data, write operation terminates and the acknowledgement signal goes low. When FIFO is full, FSM will send request to other router, if grant signal is received by it, then read operation starts and continues until grant goes low or FIFO empties. Arbiter is used in output channel in place of XY logic in input channel. Arbiter is used to solve the problem of multiple requests coming at single output port. When there are more than one request coming from one input channels to a single output channel, arbiter selects one of the request and serve it. The Figure 8 shows the state machine diagram of output channel.
performance of router as each port gets chance to send its
data.

IX. IMPLEMENTATION & RESULTS

Thus the receiver module consisting MPNoC was designed
successfully with ATMEGA 8 AVR [14] microcontroller,
Communication controller, I2 C controller and router for the
base station of wireless sensor networks. The MPNoC is
capable of receiving the data serially from the transmitter
nodes connected with appropriate sensors. The transmitter
node may consists of microcontroller, A/D converter, UART
controller etc., or depends upon the need of sensor where the
data has to be monitored. In the laboratory for evaluating the
proposed system three avr processing core, communication
controllers and i2c based memory controllers are used. Each
wireless node at the transmitter end consist of ATMEGA 8
AVR microcontroller, zigbee transceiver and different analog
sensor such as humidity, pressure, temperature etc. Each node
has different addresses to identify the node name and each
node has to send a data to receiver through zigbee transceiver
serially.

X. SYNTHESIZE RESULTS

The extended RTL view of the softcore processor is shown
in figure 9, and the chip planner view also illustrated in the
figure 10. The Table I illustrates the consumption of the logic
elements in the FPGA for implementing Soft core processor.

<table>
<thead>
<tr>
<th>Quartus II Version</th>
<th>Revision name</th>
<th>Top level Entry name</th>
<th>Family</th>
<th>Device</th>
<th>Timing models</th>
<th>Met timing requirements</th>
<th>Total logic elements</th>
<th>Total combinational functions</th>
<th>Dedicated logic registers</th>
<th>Total registers</th>
<th>Total pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.0build 21505/29/2008 Sj full version</td>
<td>AVR</td>
<td>Mcu_core</td>
<td>Cyclone II</td>
<td>EP2C35F672C6</td>
<td>Final</td>
<td>yes</td>
<td>2,075/33,216 (6%)</td>
<td>2,045/33,216 (6%)</td>
<td>390/33,216 (1%)</td>
<td>390</td>
<td>111/475 (23%)</td>
</tr>
</tbody>
</table>

Table 1: Compilation report

Another important module in the MPNoC is Serial Controller.
Figure 11 shows the RTL View of serial controller, and
compilation report shown in Table 2.
Designing Of Reconfigurable MPNOC On FPGA For Processing The Wireless Sensor Networks

![Figure 11: RTL view of the Serial controller](image)

### Table (2) – Compilation report on Serial Controller

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NoC</th>
<th>ARM LPC2148</th>
<th>AT89c51</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART Speed</td>
<td>9600 –115200</td>
<td>9600</td>
<td>9600</td>
</tr>
<tr>
<td>Corr voltage</td>
<td>1.8 v &amp; 3.3v</td>
<td>3.3v</td>
<td>5v</td>
</tr>
<tr>
<td>Onchip memory</td>
<td>Configurable</td>
<td>16kb</td>
<td>256 byte</td>
</tr>
<tr>
<td>Speed</td>
<td>200 Mhz</td>
<td>Max 60 mhz</td>
<td>24 Mhz</td>
</tr>
<tr>
<td>Number of Serial port</td>
<td>User defined</td>
<td>Two</td>
<td>One</td>
</tr>
<tr>
<td>GPIO</td>
<td>User defined</td>
<td>46</td>
<td>32</td>
</tr>
</tbody>
</table>

Table 3: Functionality Comparison of MPNoC and Microcontrollers

from this table, the illustrated system carryout the task three time faster than conventional hard core processors ARM LPC 2148 because all the node are execute the task in parallel manner and also consume less power compare to conventional microcontroller based WSN. The speed of the processor has been enhanced in this work, Functionality of the modules tested successfully. The NoC architecture can be further improved to get high speed Networks-on-chip (NoC) . The most important research areas includes, 1. NoC architectures for CMP /MPSoCs (topology, routing, switching, flow control, etc.), 2. Novel interconnect link/switch /router designs, 3. Timing, Synchronization and Asynchronization communication, 4. Mapping of Applications on to NoCs, 5. Power, energy, and thermal issues, 6. Physical design of interconnect and NoC, etc... It is not limited in this area.

### REFERENCES

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