Abstract

On-chip interconnects in deep-submicron designs have large propagation delay and energy consumption due to dominant coupling capacitance. As delay and energy are main design constraints in deep submicron technologies, several data encoding techniques for on-chip interconnects have been proposed in literature to minimize delay and/or energy.

Our contributions in this thesis are two fold: (1) we propose data encoding techniques to minimize delay and energy-delay-product for on-chip interconnects; (2) we propose a heuristic algorithm to solve a well known problem, namely data sequencing problem, for minimizing energy.

A common point in most of the existing techniques is to consider uniformly distributed random data, but the propagation delay and energy consumption are data dependent and data is application dependent. Different applications may have different data behaviors. The existing techniques which consider uniformly distributed random data may not exploit the exact data behavior of an application and hence can give inferior performance results.

By exploiting similarity in the data transmitted on on-chip interconnects, we propose three delay minimization techniques, namely, data packing (DPack), data permutation (DPerm), and data replication with shielding and two-phase transmission (RESTP). We show that for a 1-cm 32-bit bus in 90nm CMOS technology, the DPack, DPerm, and RESTP techniques achieve 57%, 39%, and 69% delay savings, respectively, in the address bus case, while in the case of data bus, these techniques...
achieve 38%, 35%, and 50% delay savings, respectively. For a 32-bit bus, the DPack, DPerm, and RESTP techniques require 38, 34, and 48 wires, respectively. We next study the impact of increasing spacing between interconnects in our techniques in terms of delay and energy-delay-product (EDP) minimization and show that our techniques achieve better delay and EDP savings over the existing techniques such as shielding and crosstalk preventing coding.

We next solve the data sequencing problem (DSP). DSP is defined as follows: Determine the optimal sequence of transmitting a given set of datawords over a bus which minimizes the switching activity on the bus. It is proved that DSP is NP-complete. Approximate algorithms are proposed to solve this problem. We propose a heuristic algorithm to solve the data sequencing problem. Experimental validation reveals that the for complete sequences, our technique achieves the optimal solution. For incomplete sequences, our technique significantly reduces the switching activity as compared to the random case. We show that the running time of our algorithm is $O(n \log_2 n)$, where $n$ is the number of datawords in a sequence.