CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

This chapter presents an overview of the field of Very Large Scale Integration (VLSI) design enabling the reader to understand the basic concepts, principles and features of low power design methodology and outlines the motivation for this research study. This chapter also gives an overview of the design space exploration of the low power VLSI domain with specific reference to arithmetic modules and concludes with identification of problem definition and the scope of this work.

1.1.1 Introduction to VLSI Design

During 1960s, the use of integrated circuits (IC) was confined to traditional digital electronic systems such as communication systems, and portable devices. But during 1990s the digital electronic circuits are becoming more application specific. According to Moore's law, the number of transistors quadruples every two to three years and hence hundred billion transistors on a single chip are projected before 2020. As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance and area remain to be
two major design goals, power consumption has become a critical concern in today’s VLSI system design.

1.1.2 The Need for Low Power Design

Over the last few years, there has been a growing interest in low power processors and Digital Signal Processors (DSPs). High speed circuits dissipate large amounts of energy in a short amount of time due to high power density of devices on a single die, generating a great deal of heat as a by-product. A survey report shows that power density of some designs can reach the power density of a rocket nozzle, as shown in Figure 1.1 if power aware design approaches are not used. Serious reliability issues arise when working at such high temperatures.

Therefore, the lower the power consumption, the lesser the heat generated and so the lower the cost required for extra cooling systems in offices and homes. Also this heat needs to be removed by the package on which integrated circuits are mounted. Hence heat removal becomes the first limiting factor if the heat sink cannot adequately dissipate the heat, or if the required thermal components are too expensive.

The second limiting factor of high-power circuits relates to the increasing popularity of portable electronic devices. A limited amount of energy stored in a small battery requires extensive power management techniques to lengthen battery lifetime for as long as possible. Hearing aids are a typical example of a portable device which includes digital signal processing algorithms, demanding considerable computing power. The exploding market growth of portable electronic appliances increases the demand for complex integrated systems that can be powered by lightweight batteries with long times between re-charges. To extend battery life, low power operation is desirable in integrated circuits.
Due to the steady growth of operating frequency and processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques and battery life in portable electronic devices is limited.

Figure 1.1 Heat dissipation of modern processors

1.1.3 Power Consumption in VLSI Circuits

Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, has shown its wide application in many key consumer products from computers, consumer electronics, cellular phones, digital cameras, personal digital assistants (PDA), automobiles, and high speed networking devices. Power consumption of CMOS circuit consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power is related to circuit switching activities or the changing events of logic states, including power dissipation due to capacitance charging and discharging, and dissipation due to short-circuit current. In CMOS logic, the leakage current, either reverse biased PN-junction current or sub-threshold channel conduction current, is the only source of
static current. The total power consumption is summarized in the following equations.

\[ P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} \]  
(1.1)

\[ = P_{\text{cap}} + P_{\text{SCC}} + P_{\text{static}} \]  
(1.2)

\[ P_{\text{cap}} = \alpha_{0\rightarrow1} F_{\text{clk}} C_L V_{DD}^2 \]  
(1.3)

\[ P_{\text{SCC}} = \alpha_{0\rightarrow1} F_{\text{clk}} I_{\text{peak}} \left( \frac{t_r + t_f}{2} \right) V_{DD} \]  
(1.4)

\[ P_{\text{static}} = I_{\text{static}} V_{DD} \]  
(1.5)

\[ P_{\text{cap}} \] in Equation (1.2) represents the dynamic power due to capacitance charging and discharging of a circuit node, \( C_L \) is the loading capacitance, \( F_{\text{clk}} \) is the clock frequency, and \( \alpha_{0\rightarrow1} \) is the \( 0 \rightarrow 1 \) transition probability in one clock period. In most cases, the voltage swing \( V_{\text{swing}} \) is the same as the supply voltage \( V_{DD} \). \( P_{\text{SCC}} \) is power consumption due to short-circuit current. The peak current, \( I_{\text{peak}} \), is determined by the saturation current of the devices and is hence directly proportional to the sizes of the transistors. \( t_r \) and \( t_f \) are rise time and fall time of short-circuit current, respectively. The static power \( P_{\text{static}} \) is primarily determined by fabrication technology and is usually smaller than the dynamic power. The leakage power problem mainly appears in very low frequency circuits or ones with “sleep modes” where dynamic activities are suppressed. Power optimization of digital systems has been studied at different abstraction levels, from the lowest technology level optimizing the factors \( C_L \), \( V_{DD} \), and \( F_{\text{clk}} \), to the highest algorithm and architecture level affecting all factors \( \alpha_{0\rightarrow1} \), \( C_L \), \( F_{\text{clk}} \), and \( V_{DD} \) and thus low-power design often becomes the task of minimizing \( \alpha_{0\rightarrow1} \), \( C_L \), \( V_{DD} \) and \( F_{\text{clk}} \), while retaining the required functionality.
1.1.4 Power Estimation in VLSI Circuits

One of the important requirements to know during a design process is how much power the circuit should dissipate considering its application. So after the designer writes the required code or designs the circuit using schematic entry keeping in mind all the specifications, power calculation needs to be done to confirm if the design meets the required specifications. This is done prior to sending the chip for fabrication. So it is extremely important to get accurate power values using power analysis tools running at certain input conditions.

Numerous Electronic Design Automation (EDA) tools have been developed to not only determine power but also help in power reduction. The usage of these tools is classified depending on the layer of abstraction they are used in. The three main layers of abstraction include the Register Transfer Level (RTL), the gate and the transistor level.

1.1.5 Power Reduction in VLSI Circuits

Minimizing the power consumption of circuits is important for a wide variety of applications, both because of the increasing levels of integration and the desire for portability. Since performance is often limited by the speed of arithmetic components, it is also important to maximize the speed. Power reduction has to be addressed at every design level, like system, RTL, gate and transistor-level, technology level where most power can be saved at the system level.

At the technology level, power consumption is reduced by the improvement in fabrication process such as small feature size, very low voltages, copper interconnects, and insulators with low dielectric constants. Lowering of $V_{DD}$ is a well-accepted method of reducing chip power, and even
the most high-performance microprocessors are run at lower supply voltages. Other schemes, such as using multiple supply voltages have been proposed. At floor plan level the power characteristics for the entire die are planned and power or delay constraints are allocated. Power due to the assembly of macro blocks is optimized, subject to delay and area/ routability constraints. The lowest level stage visible to the designer is gate/circuit level where transistors are assembled into basic gates.

Frequently, the compromise between the demands of performance and speed can be accomplished by selecting the optimum circuit architecture. At the circuit level, power reduction is achieved by transistor sizing, transistor network restructuring and reorganization, and different circuit logic styles. A full custom approach may succeed in achieving lower power than a standard cell approach, as individual transistor sizing may overcome certain obvious inefficiencies.

1.1.6 Low Power Design Metrics

Design of low-power high-performance CMOS circuits is a big challenge. Often, an adder or multiple adders will be in the critical path of the design, limiting the performance of a design. At the circuit level, an optimized design is desired to avoid any degradation in the output voltage, consume less power, have less delay in critical path, and be reliable even at low supply voltage.

Good driving capability under different load conditions and balanced output to avoid glitches is also important. Since the arithmetic cells are duplicated in large numbers, layout regularity, and interconnect complexity are vital. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit.
Power refers to the number of Joules dissipated over a certain amount of time whereas energy is a measure of the total number of Joules dissipated by a circuit. The maximum power at any time, peak power, is often used for power and ground wiring design, signal noise margin and reliability analysis. Energy per operation is a better metric of the energy efficiency of a system, especially in the domain of maximizing battery lifetime.

One of the most effective dynamic power reduction techniques is lowering the supply voltage of CMOS transistors because the power consumption of CMOS transistors increases proportional to the supply voltage. However, transistor switching delays are increased due to lowering of supply voltage. In order to realize maximum performance, these circuits are designed at the transistor level using full-custom design style.

The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and intra- and inter-cell wiring capacitances. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. Power dissipation is determined by the switching activity and the node capacitances due to gate, diffusion, and wire capacitances.

Finally, the wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.

In digital CMOS low power design, the power-delay product is commonly used design metric to assess the merits of designs. Instead, the term energy-delay product could be used since it involves two independent measures of circuit behaviors. Therefore, when power-delay products are used
as comparison metric, different schemes should be measured at the same
frequency to ensure that it is equivalent to energy-delay product comparison.

1.1.7 Low Power Arithmetic Modules

When designing new embedded systems it is important to have
efficient components to build from. Arithmetic circuits are especially
important, since they are extensively used in all applications. For high-speed
DSPs, one of the main processing bottlenecks is the Multiply and
ACcumulate unit (MAC).

Adder is one of the most important components of a central
processing unit (CPU), Arithmetic logic unit (ALU), floating-point unit and
address generation units like cache or memory access unit. Arithmetic
functions such as addition, subtraction, multiplication and division are some
examples which use adder as a main building block to apply the energy-
efficient design methodologies.

Multiplication is a fundamental operation in most signal processing
algorithms. Multipliers have large area, long latency and consume
considerable power. Therefore, low-power multiplier design has been an
important part in low-power VLSI system design. Typically, 16 bit multipliers
are used for digital signal processing and 53/64 bit multipliers are used in
microprocessors. The primary objective in any VLSI design is power
reduction with small area and delay overhead. By using new algorithms or
architectures, it is possible to achieve both power reduction and area/delay
reduction.
1.2 MOTIVATION

The need for low-power VLSI systems arises from two main factors. The first factor is attributed to problem of heat removal due to large power consumption using proper cooling techniques. The third generation (3G) wireless protocol provides real-time streaming video at a high data rate on a 3G-enabled cellular phone. Such a computation intensive application can impact the battery life of the portable device.

The portable digital hearing aids due to the advances in integrated circuit technology have extremely low power consumption requirements in the order of 0.5 - 1.0 mW at 1.0 V supply based on hardwired ASIC. Bio medical devices and personal home health monitoring systems are hand held devices now due to CMOS implementation in DSPs. Hence second factor is due to the limited battery lifetime in portable devices. Designing low power circuits for DSPs directly leads to prolonged operation time in these portable devices which is the motivation for this study.

Arithmetic circuits are important modules in microprocessors and DSPs and they are power-hungry and performance-limiting. In fact, multiplication combined with accumulation of products is one of the most common operations performed in signal processing involving heavy use of multiply-accumulate operations. Faster multiplication hardware yields faster performance in many DSP algorithms, and for this reason all modern DSP processors include at least one dedicated single-cycle multiplier or combined MAC unit.

There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. By improving the design of arithmetic circuits, the overall performance of a system can be significantly improved. This thesis will present an investigation on the various designs of
adders and multipliers and propose efficient implementations of CMOS adders and multipliers in hybrid CMOS logic style. Well-known multipliers such as array, Wallace tree multipliers, Dadda tree multipliers are included in the study.

1.3 A REVIEW OF LITERATURE

Multiply-Accumulator (MAC) is a very common digital block in embedded processors and programmable DSPs. The MAC unit always lies in the critical path that determines the speed of the overall hardware systems. Hence the need arises for investigating the designing of high-speed energy-efficient MAC architectures for programmable processors.

A MAC unit consists of two main components, a multiplier and an accumulate adder, while accumulate result is fed back to the top of the accumulate adder. In order to obtain high speed, the multiplier is divided into Partial Product (PP) unit and a carry-propagate final adder (CPA). Additionally, the PP unit is divided into two a Partial-Product Generation (PPG) and Partial Product Reduction Tree (PPRT).

There has been extensive work on the main components of the MAC namely the multiplier and the adder. There had been lot of research work going on in the design of PPRT, PPG, and final adder of a multiplier as early as 1963. Recently due to the importance of DSPs in hand held devices, there is a spurt in research in energy efficiency of these components.

Compressors are a critical component of the multiplier circuit, which greatly influence the overall multiplier speed. High-speed compressors can add several partition products at once to reduce logic depth of the PPRT unit but they require more efforts in custom design. There are other studies on reducing delay of the PPRT by using either high-speed compressors or speed-
optimized structures. Researchers have tried to explore higher order compressor families like (6: 2) and (9: 2) by interconnecting (3: 2) and (4: 2) compressors.

Hence this literature survey had been presented in such a way that it addresses existing work relating to low power processors, design and architecture of MAC units. Also it presents the works on implementation, architectures, power, delay, performance and area characteristics of PPRT, PPG, arithmetic components of full adders, compressors and counters which form the basics of MAC unit in different technology nodes.

This section discusses the existing literature works on Low power trends and Programmable DSP processors.

Gary Yeap (2013) has stressed that numerous challenges are ahead for the growth of mobile SoCs but tremendous opportunities exist for innovations in the industry. The growth of smart mobile wireless devices has transformed the semiconductor industry which was achieved mainly through silicon technology scaling, and from single to dual- and quad-core. For mobile SoCs to continue offering new and exciting user-experiences, and longer battery life, a different approach to speed x density/power/cost constrains is necessary.

Lunner & Hellgren (1991) presented the design of a digital filter bank that can be used in a hearing aid with a total of 27 multiplications. Complementary interpolated linear phase impulse-response filters are used to minimize the number of multiplications per sample. The hearing aid was implemented on a general-purpose digital signal processor based on TMS320E25 for real-time evaluations.
Mutoh (1996) presented this 1 V DSP LSI chip with 26 MOPS and 1.1 mW/MOPS adopting a multi-threshold-voltage CMOS (MTCMOS) technique for battery-driven mobile phone equipment. The design uses small embedded power-management processor decreasing power during waiting periods and reduced supply voltage as a direct approach to power reduction.

Meindl (1997) reports that the invention of the bipolar transistor in 1948 and the integrated circuit in 1958 as well as the announcement of CMOS logic circuits in 1963 demonstrated the basis for modern low power electronics. He discusses that there is future opportunities for low power giga scale integration. Dancy & Chandrakasan (1997) showed that the key to low power design is aggressive voltage scaling to 1V and below through technology, circuit, and architecture optimization. Threshold voltage scaling enables aggressive supply scaling but increases leakage power. Technology and circuit trends to control idle leakage power are presented including MTCMOS, variable $V_T$ bulk-CMOS, and variable $V_T$ SOI.

Nielsen & Sparso (1998) showed asynchronous re-implementation of a 7-band interpolated FIR (IFIR) filter bank as part of the Digi Focus digital hearing aid manufactured by Oticon Inc. When processing typical data of less than 50 dB sound pressure, the power consumption of the asynchronous chip is only 85 µW which is 5 times lower than the existing synchronous implementation. Verbauwhede & Touriguian (1998) developed a programmable highly parallelized 16 bit DSP engine specifically for next generation wireless digital systems and speech applications efficient for compute-intensive tasks such as vector quantization and Viterbi operations. The data path contains two Multiply-Accumulate units and one ALU. This efficiency is reflected in the very low MIPS requirement to implement cellular standards.
De & Borkar (1999) discuss key barriers to continued scaling of supply voltage and technology for microprocessors to achieve low-power and high-performance. Moller et al (1999) in their paper present a 1 V first general purpose programmable digital signal processor used in behind-the-ear (BTE) and in-the-ear hearing aid manufactured by GN Danavox. In a 0.5μm technology at 2 MHz processing speed, the processor consumes 800 μA from a single cell battery. Using a dual multiply-accumulate architecture, the processor executes a 256 point block floating-point finite Fourier transform (FFT) in just 2900 instruction cycles.

Mosch et al (2000) illustrated the flow and techniques used in designing a DSP chip in conventional 0.25 μm process to be used in a new hearing aid implementing multi-band compression, noise cancellation, pattern recognition and adaptive filtering. The processor implemented by them consumes 720 μW under the nominal 1.2 V supply and performs 50 M 22 b operations per second. The DSP achieves 0.015mW/MOP/s, 6x times better than prior results in this field.

Lai et al (2001) used the instruction level clock gating technique to achieve lower power for a low power 32-bit 20 MIPS DSP core designed for MPEG1 Audio Layer III portable MP3 decoder besides other effective dynamic power management schemes. It has an architecture designed specifically for MP3 decoding algorithm implementation.

This following section gives an overview of existing MAC architectures in the literature.

Ram Krishnamurthy et al (1998), describe an on-chip series-regulated mixed swing methodology with sleep-mode control for lowering the power consumption of high-performance DSP multiplier-accumulator circuits. A 16*16+36-bit Overlapped bit-pair Booth recoded, Wallace tree
MAC is fabricated in a commercial 0.5mm CMOS process in the proposed series-regulated methodology and conventional static CMOS. They report up to 2.55X reduction in energy/operation over static CMOS, while achieving a simultaneous 1.8X improvement in low-voltage manufacturability.

Aamir Farooqui & Vojin Oklobdzija (1998) report the data-path and VLSI implementation of a 32x32 bit signed/unsigned multiply accumulate unit. This MAC unit can perform 32x32, 32x16, and two 16x16 multiplications, on signed/unsigned operands with a throughput of 2, 1, and 1 cycle, respectively. The Booth encoding technique reduces the number of partial products (PP) by half. Further increase in speed is achieved by using Three Dimensional reduction Method (TDM) to add the partial products. The MAC unit has been modeled in VHDL, and it implements an algorithm which makes this data path organization fast and efficient in silicon.

Elguibaly (2000) proposed a fast pipelined implementation to lower the MAC architecture’s critical delay. Liao & Roberts (2002) propose a high-performance and low-power 32-bit multiply-accumulate unit. The last mixed-length encoding scheme used in the MAC without adding extra delay to the faster four-stage Wallace tree of a 12-bit encoding scheme. With this new encoding scheme, one-cycle throughput for 16-bit ×16-bit and 32-bit ×16-bit MAC instructions was achieved at very high frequencies. A mixture of static CMOS logic and complementary pass-gate logic was used to achieve the high-speed and low-power goals. Several power-saving techniques were also implemented in this MAC.

Chen et al (2003) present low-power 2's complement multipliers by minimizing the switching activities of partial products using the radix-4 Booth algorithm. Two multipliers based on row-based and hybrid-based adder trees are realized with operations on effective dynamic ranges of input data. The
proposed 16 x 16-bit multiplier with the column-based adder tree conserves more than 31.2 percent, 19.1 percent, and 33.0 percent of power consumed by the conventional multiplier, in various applications respectively. Li Hsun & Chen (2005) proposed a low-power Multiplication-Accumulation Computation unit using the radix-4 Booth algorithm, by reducing its architectural complexity and minimizing the switching activities.

Tung et al (2009) propose a high-speed and energy-efficient 2-cycle Multiply- Accumulate architecture. By performing carry propagation only in the second stage of the MAC pipeline, Multiplication and accumulation have similar delays. But in contrast to previous MAC architectures that propose to only use one carry-propagation stage, this architecture requires no extra cycles to produce the final result. The place-and-route evaluation shows that the proposed architecture, averaged across several operand sizes, offers a 33 percent improvement in speed and a 37 percent reduction of energy over conventional 2-cycle MAC architecture.

Wang et al (2004) propose a fixed-width multiplier using the left-to-right algorithm for partial-product reduction. The high-speed feature of this design is used to trade for low power. In one design, the proposed multiplier not only owns 8 percent speed improvement but also gains 14 percent power and 13 percent area reduction. When applying the voltage scaling to balance the speed, the power reduction is increased to 29 percent.

Lee (2004) addresses energy efficient design, of a power-aware scalable pipelined Booth multiplier that makes use of common functional unit, optimized Wallace-trees and a 4-bit array-based adder-tree for DSP applications. The multiplication mode is determined by the dynamic-range detection unit, which generates and dispatches the control signals for the pipeline stages. For the 8-bit and 4-bit computations, the proposed Booth
multiplier leads to a 29 percent and 58 percent power consumption reduction over a non-scalable Booth multiplier, respectively. The proposed scalable pipe lined Booth multiplier proves to be globally 20 percent more power efficient than a non-scalable pipe lined Booth multiplier, and also it has fast speed due to pipelining.

This section presents the literature review on multipliers and compressors.

Wallace (1964) presented a design for fast multiplication based on parallel pseudo adders and is simply a (3, 2) counter which avoids carry propagation in a multiplier using purely combinational logic in one gating step. A rapid square-root process is also outlined. Earl Swartzlander, Jr (1973) described, analyzed, and compared in this work three types of parallel counters which are multiple-input circuits that count the number of their inputs that are in a given state. The first counter consists of a network of full adders. The second counter uses a combination of full adders and fast adders while the third type of counter uses quasi-digital like techniques to generate an analog signal proportional to the count which is then digitized.

Dadda (1976) later refined Wallace’s method by a counter placement method that required fewer counters in the partial product reduction stage at the cost of a larger carry-propagate adder (CPA) postponing the reduction to the extent possible without causing additional delay. Weinberger (1981) introduced the next higher-level compressor (4:2) compressor which consists of five inputs and three outputs, and compresses four partial products into two, thus offering a higher compression ratio and a more regular interconnection structure than its 3: 2 counterparts.

Bose et al (1987) in their paper present the design of a fast and area-efficient multiply-divide unit used in building a VLSI floating-point
processor (FPU), conforming to the IEEE standard 754. The multiplier and divider are implemented in 2 micron CMOS technology with two layers of metal, and occupy 23 square mm (23 percent of the entire FPU).

Mehta et al (1991) reported the design of a fast multiplier implemented using either (7,3) parallel counter of (7:3) compressor circuits for implementation in CMOS technology. It is shown that parallel multipliers implemented using (7,3) counters exhibit better performance than those implemented using (7:3) compressors. They exhibit identical delay characteristics while the counter implementation requires fewer gates and lays out better. The (7,3) counter based implementation compares favorably with the (4:2) compressor implementation in terms of gate count, but has slightly higher delay for the 16-b by 16-bit multiplier.

Song & De Micheli (1991) discuss VLSI implementations of high-performance parallel multipliers. Circuit building blocks required for partial-product reduction are analyzed and two schemes leading to highly regular layouts are proposed. A silicon implementation of a prototype slice of an IEEE double-precision floating point multiplier in a 0.8-μm double-metal BiCMOS technology is presented. An (n,m) parallel counter is a circuit with n inputs that produces an m-bit binary count of the number of its inputs that are ones. The design of large parallel counters with up to 1022 inputs is reported. Design tradeoffs regarding the use of counter cells of size ranging from (3,2) to (31,5) as building blocks are examined, Robert F Jones & Earl Swartzlander Jr (1992).

K’Andrea Bickerstaff et al (1993) present the reduced area multiplier, with a novel reduction scheme resulting in fewer components and less interconnect overhead than either Wallace or Dadda multipliers. This reduction scheme is especially useful for pipelined multipliers, because it
minimizes the number of latches required in the reduction of the partial products. Area estimates indicate that pipelined reduced area multipliers require 3 to 8 percent less area than equivalent Wallace multipliers and 15 to 25 percent less area than equivalent Dadda multipliers. This work uses fast carry propagate adder as final adder.

Wang et al (1995) analyze the constraints for column compression (CC) with full and half adders analyse the flexibility for implementation of the CC multiplier, including the allocation of adders, and choosing the length of the final fast adder. They introduced a new technique for CC multiplication which is area efficient and have shorter interconnections than the classical Dadda CC multiplier.

Ohkubo et al (1995) fabricated a 54×54-b multiplier using pass-transistor multiplexer by 0.25-μm CMOS technology. To enhance the speed performance, a new 4-2 compressor and a carry look-ahead adder (CLA) have been developed. The new circuits have a speed advantage over conventional CMOS circuits because the number of critical-path gate stages is minimized due to pass-transistor multiplexers. The active size of the 54×54-b multiplier is 3.77 mm×3.41 mm. The multiplication time is 4.4 ns at 2.5 V power supply.

Oklobdzija (1995) discusses improvements in bit reduction techniques in a parallel multiplier and the use of a final adder which is optimized for the uneven signal arrival profile. The column compressors configuration is optimized in order to reduce the longest signal path. The final adder is designed for the uneven input arrival time of the signals originating from the multiplier tree. This results in more compact wiring and balanced delays yielding a faster multiplier. Breveglieri et al (1995) present a study on the introduction of pipelining in parallel VLSI multipliers, built according to
the column compression (CC) design techniques. CC multiplier schemes aimed at optimizing the required silicon area, the regularity and the locality of the interconnections among the adders, have been proposed. The authors discuss about the introduction of pipelining in these last structures and compare the obtained results with existing structures, in terms of required number of components and operation frequency.

Ciminiera & Montuschi (1996) present n x n multiplication schemes where an adder at the last step to convert the carry-sum representation of the most significant half of the result into a non-redundant form is performed with a circuit operating in parallel with the carry-save array. Johnny Pihl & Einar Aas (1996) present a multiplier and squarer structures generator suitable for high performance bit-parallel DSP applications in VLSI. The squarer structure employs a novel bit-parallel partial product reduction scheme, reducing delay and hardware by 50 percent, compared to a full multiplication. The generator is based on optimized Wallace trees, Booth encoding and binary tree vector merging addition. Results indicate a delay reduction of 10-20 percent compared to traditional designs for high speed, as well as a reduction in power and area, for a standard 0.8 μ CMOS process.

Ghosh et al (1994) propose a new architecture called Tree of Wallace Tree with XORs as Building Blocks (TWTXBB) and offers a 33 percent improvement in performance over that of the Wallace tree. It is highly regular rendering itself amenable to automatic generation. The multiplier achieves its high-speed from both a new architecture and a logic style called normal process complementary pass transistor logic (NPCPL). The architecture can provide both low latency and high throughput simultaneously.
This paper reports on the dynamic power dissipation and delay of CMOS implementations of four different multipliers. Simulation was used to establish a set of models for both delay and power dissipation, and those models were then used to compute the power-delay products of the multipliers Callaway & Swartzlander (1997).

Raghunath (1997) made use of a carry-save multiplier that can simplify sign extension and saturation, and further applies it on MAC architecture to reduce the unit’s area and power consumption. Alidina et al (1998) presented first 16 bit dual-MAC DSP core featuring a data path with two 16×16-bit multipliers and dual 40-bit adders that can all operate in one clock cycle to support compute-intensive DSP algorithms. In addition, the device includes special hardware to support all aspects of key communications applications such as wireless terminals, wireless infrastructure, and multichannel modems.

Shivaling et al (1999) present a work on improvement of throughput of multiplier based on a compact tiled structure, wherein the shape of a tile represents the delay through that tile. Based on simulation studies, a temporally tiled array multiplier achieves 50 percent and 35 percent improvements in delay and power dissipation compared to a conventional array multiplier.

Jinn-Shyan et al (2000) presents the importance of power consumption of the clocking system in the design of a low-power pipelined multiplier. A new pulse-triggered true single-phase clocking (TSPC) flip-flop (PTTFF) is proposed for this purpose in this design. Using the PTTFF together with the 14-transistor pseudo-NMOS full adder, an 8-b by 8-b pipelined multiplier has been designed and implemented, employing a 0.6- m
CMOS process. The chip has been fabricated, and the measured power is 52.4 mW when operated at 300 MHz and 3.3 V.

Lee & Rim (2000) proposed a hardware reduced multiplier using truncation scheme for Booth multiplier for DSP applications. Truncated Booth multiplier reduced area by about 37.48 percent and power consumption by about 44 percent. Ohsang Kwon et al (2000) presents a logical decomposition for fast 5:2 compressor and is proposed to be used for 16-bit×16-bit 2’s complement MAC designs. The use of the new 5:2 compressor leads to 14 percent speed improvement in the MAC design over the conventional designs using 4:2 compressors and 3:2 counters.

In this paper by Prasad & Parhi (2001) novel architectures and designs of high speed, low power 3:2, 4:2 and 5:2 compressors capable of operating at ultra-low voltages are presented. The proposed architecture shows the importance of multiplexers in arithmetic circuits that result in high speed and efficient design. Fayed & Bayoumi (2001) report power reduction by reducing the circuit activity at the architecture level by dividing the multiplication circuit into clusters of smaller multipliers. By applying clock gating techniques and preprocessing operations on the input pattern using simple logic functions, some of these clusters that are producing a zero result are disabled and hence saving the switching power component.

This paper presents a study in the switching activity of parallel multipliers. Modified-Booth multipliers are used to compare carry save implementations with different optimization techniques and multipliers using redundant binary representations. Signal correlation and random sets of data used for simulation show the impact on switching activity and how architectures are suited for different applications. de Angel & Swartzlander Jr (2001). Chang-Young Han et al (2001) propose a separated multiplication
technique (SMT) that can be used in digital image signal processing such that, the redundant multiplication of higher bits is avoided by separating multiplication into higher and lower parts thereby reducing the dynamic power by about 14 percent in multipliers and in a 1-D 4-tap FIR filter by about 10 percent.

Niichi Itoh et al (2001) designed an efficient layout method for a high-speed Wallace tree multiplier. A rectangular Wallace-tree construction method is proposed to reduce the number of adding stages in forward and downward by eliminating the dead area. Also, in a $54 \times 54$-bit multiplier the carry propagation between the two groups to realize high speed and a simple layout is optimized. Santoro & Horowitz (2002) reported the design of a $64 \times 64$-bit, the Stanford pipelined iterative multiplier (SPIM), with an array of a tree of $4:2$ adders. A $4:2$ carry-save accumulator at the bottom of the array is used to iteratively accumulate partial products, reducing area. The latency for a $64 \times 64$-bit fractional multiply is under 120 ns, with a pipeline rate of one multiply every 47 ns. It was shown in this paper that a $4:2$ tree is better suited for a VLSI implementation than Wallace tree.

Chang et al (2004) proposed tree architectures to improve the speed of the partial product addition process by introducing parallelism in ultra low power domain. The tree structure, using $3:2$ compressors suffer from irregular interconnections and are difficult to layout. It also results in high power consumption as a result of the capacitance introduced by large interconnections. Menon & Radhakrishnan (2006) propose two novel high performance $5:2$ compressor architectures limiting the carry propagation to a single stage, thereby reducing the overall propagation delay. The architectures are implemented with various XOR–XNOR circuits to identify the best one in terms of power and delay. The simulation results show lower power and 25
percent improvement in speed compared to the best architecture reported in
the literature for supply voltages ranging from 1.5V to 3.3V.

Yu Qian & Wang Dong-Hui (2003) proposed a regularized
multiplier generator, which can produce the source codes in VHDL
automatically. The generator chooses the 4-2 trees, which achieve the same
speed performance as equivalent Wallace trees in many cases, but require a
simple and regular interconnection scheme.

Earl Swartzlander Jr (2004) reviews a number of counter designs
that have been presented over the last four decades with the emphasis is on
(7, 3) counters as they are key elements of many arithmetic elements,
especially fast multipliers. Sreehari Veeramachaneni et al (2007) propose,
novel architectures and designs for high speed, low power (3, 2), (7, 3),
counters capable of operating at ultra-low voltages which are key elements in
fast multipliers. Based on these counters, a generalized architecture is derived
for large (m, n) parallel counters. The proposed counter designs have been
compared with existing designs and are shown to achieve an improvement of
about 45 percent in delay and a reduction of about 25 percent in power
consumption.

Vansantha et al (2007) propose a methodology based on reordering
the input vectors to reduce the power dissipated in combinational circuits and
the experimental results indicate that the proposed technique achieves
reduction in average power, reduction in peak power and reduction in
difference between maximum and minimum instantaneous power in array
multiplier.

Modugu Rajashekar et al (2009) uses novel compressor designs
and sparse tree adders module is completely redesigned using the novel
compressors and the final addition module is implemented using a new less
complex sparse tree based inverted end-around-carry adder. Dursun Baran et al (2010) analyzed 16x16-bit Booth and Non-Booth multipliers in energy and delay space under varying constraints and showed that Non-Booth multipliers start to become more energy efficient for strict delay targets. In addition, novel 3:2 and 4:2 compressors are presented to save energy at the same target delay. Dandapat et al (2010) proposed higher order compressors (5:3, 6:3 and 7:3) to improve the performance of multipliers. They have merged binary counter property into the high order compressors which have further reduced the partial product stages and power consumption.

Ravi (2011) presented a register Pipelined Modified Booth Multiplier (PMBM) to improve the speed of the multiplier with Carry Save Addition using 16-T Full adders. The PMBM proposed is 28.51 percent faster than the Modified Booth Multiplier (MBM). This is calculated with TSMC 0.18um technology using Hspice. The proposed modulo $2^n+1$ multiplier by as primitive building blocks for fast low-power operation. Marimuthu et al (2013) in their study, use 7-3 compressor which is designed by four full adders to improve the performance of multiplier. In this study, the authors have proposed 8-4 and 9-4 compressors which have further reduced the number of partial product stages of multipliers as compared to existing compressors. But the work does not discuss timing and power savings.

Also there are a number of research works carried out on the design of 1 bit low power full adders which can be used in cascaded multiplier circuits. Here is a brief literature review on the design of such adders.

MacSorley (1961) describes methods of obtaining high speed in addition, multiplication, and division in parallel binary computers and then compared with each other as to efficiency of operation and cost. The transit time of a logical unit is used as a time base in comparing the operating speeds
of different methods, and the number of individual logical units required is used in the comparison of costs.

Callaway & Earl Swartzlander Jr (1992) report on the speed and dynamic power dissipation of CMOS implementations of six different adders. The adders are constructed with inverters and two-to-four-input AND and OR gates. Extensive simulation was used to evaluate the switching characteristics, and the results are used to rank the adders in terms of speed, size, and the number of logic transitions. According to the figure of merit reported the carry look ahead adder is the best design for word sizes between 16 and 64 bits.

Thomas Callaway & Earl Swartzlander Jr (1993) examined six types of adders to model their power dissipation. The main discrepancy between the simple model and the physical measurements seems to be the assumption that all gates will consume the same amount of power when they switch, regardless of their fan-in or fanout.

Abu-Khater et al (1996) designed a novel complementary pass-transistor logic-transmission gate (CPL-TG) full adder circuit, simulated and fabricated using 0.8-μm CMOS in BiCMOS technology. The full adder implementation provided an energy savings of 50 percent compared to the conventional CMOS full adder. CPL implementation of the Booth encoder provided 30 percent power savings at 15 percent speed improvement compared to the static CMOS implementation.

Margala (1999) presents the results of a study of alternative adder architectures, implementing a full-swing Bipolar Double Pass-Transistor adder and a new full-swing BiNMOS adder. He claims that all remaining proposed adders have a lower crossover capacitance with a standard CMOS
adder than the previously reported low-voltage adders. The designs were implemented in 0.8 μm BiCMOS technology.

The Static Energy-Recovery Full adder (SERF) topology proposed by Shalem et al (1999) uses only 10 transistors which is the least number of transistors reported. For low supply voltages the circuit has a problem in the state when A=1, B=1, and Cin=0. Ahmed et al (2001) analyse the performance of twenty different 1-bit novel full-adder cells constructed by connecting combinations of different designs of anatomized adder cell modules. Each of these cells exhibits different power consumption, speed, area, and driving capability figures. Two realistic circuit structures that include adder cells are used for simulation. A library of full-adder cells is developed and presented to the circuit designers to pick the full-adder cell that satisfies their specific applications.

Bartlett & Dempster (2001) compare the effects on power consumption of using direct versus transposed direct forms, tree versus linear structures and carry-save (CS) versus carry-ripple (CR) adders for which multiplier block algorithms have been designed for a simple multiplier block FIR filter design. They report that tree structures and selective use of CS adders is shown to offer power savings provided that care is taken with their deployment.

Alioto & Palumbo (2002) analyzed the performance of 1 bit full adders for speed, power consumption and power-delay including the recently proposed adders. The investigation has been carried out with properly defined simulation runs on a Cadence environment using a 0.35μm process, also including the parasitics derived from layout. They show that, except for short chains of blocks or for cases where minimum power consumption is desired, topologies with only pass transistors or transmission gates are not attractive.
This paper examines the design of a hybrid prefix adder under the condition of non-uniform input signal arrival. This is encountered in the final adder for fast parallel multipliers, which use column compression reduction. The prefix graph scheme efficiently accommodates the non-uniform arrival times. Choi & Swartzlander Jr (2002). Goel et al (2004) present several designs for 1-bit full adder cell featuring hybrid CMOS logic style. These designs are based on a novel XOR-XNOR circuit that simultaneously produces XOR and XNOR full-swing outputs and outperforms its best counterpart showing 39 percent improvement in PDP. All the designs are able to operate at low voltages without significant loss in signal integrity. The improvement in terms of PDP obtained by the best full-adder cell as compared the best standard design amounts to 24 percent.

Jiang et al (2004) present a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). Intensive simulation shows that the new adder has more than 26 percent in power savings over conventional 28-transistor CMOS adder and it consumes 23 percent less power than 10-transistor adders (SERF and 10T) and is 64 percent faster.

Chip-Hong Chang et al (2005) investigate the area and power-delay performances of low-voltage full adder cells in different CMOS logic styles for the predominating tree structured arithmetic circuits and present a new hybrid style full adder circuit in 0.18-µm CMOS process technology. The proposed hybrid full adder exhibits not only the full swing logic and balanced outputs but also strong output drivability and energy efficiency. A systematic procedure to scale the transistor for minimal power-delay product is proposed. Fartash Vasefi & Abid (2005) present their work on low power N-bit adders and multiplier using lowest number of transistors 1-bit Adders with one Vt degradation in the output levels and claimed a power saving of 43.68 percent.
over C-CMOS 28 T adder. They have designed 4 bit RCA and 12 bit Carry
Save Adders with Braun multiplier to evaluate the performance of the adder.

Sumeer Goel et al (2006) present the new full adder based on a
novel XOR-XNOR circuit that generates full-swing outputs simultaneously.
This circuit outperforms its counterparts showing 5-37 percent improvement
in the power-delay product (PDP). A novel hybrid-CMOS output stage that
exploits the simultaneous XOR-XNOR signals is also proposed. There is
approximately a 40 percent reduction in PDP when compared to its best
counterpart.

Lin et al (2007) propose a novel high-speed and energy efficient 10-
transistor full adder design. This novel adder adopts inverter buffered
XOR/XNOR circuits avoiding threshold voltage loss achieving low voltage
operation, high computation speed and energy efficient.

Farshad Moradi & Ali Peiravi (2008) in their work presented a new
full adder circuit optimized for ultra-low power operation on SERF full adder
based on modified XOR gates to minimize the power consumption. This
circuit design lacks driving capability when cascaded.

Senthilpari et al (2008) have developed a new full-adder cell using
multiplexing control input techniques (MCIT) for the sum operation and the
Shannon-based technique to implement the carry. The proposed adder cell is
applied to the design of several 8-bit array multipliers, namely a Braun array
multiplier, a CSA multiplier, and Baugh–Wooley multipliers. From the
analysis of these simulated results, it was found that the proposed multiplier
circuit gives better performance in terms of power, propagation delay, latency
and throughput than other published results.
Subodh Wariya et al (2012) discuss a high-speed conventional full adder design combined with MOSCAP Majority function circuit in one unit to implement a hybrid full adder circuit. This technique helps in reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. But no power reduction reported.

This concludes the section on literature review for trends in low power design and arithmetic modules.

1.4 IDENTIFICATION OF PROBLEM

From the detailed literature survey it can be concluded that energy efficient parallel multiplier design requires the exploration of many application algorithms and circuit implementation techniques. For higher order multiplications, a huge number of adders or compressors are to be used to minimize the partial product addition. There are works relating to either high speed area efficient MAC or energy efficient MAC. Most of these works have utilized Booth Multiplier or Wallace tree structure. While the above mentioned designs may address the computational performance or power dissipation of MAC architectures, these schemes are applied on one type of MAC architecture instead of exploring the other types, which implies that there still is room to improve on a conventional architecture. From the existing literature it is also found that column compression multipliers have been overlooked in VLSI due to its irregular structure. Only a handful of previous works have been addressed at column compression modified Wallace tree or Dadda tree structures. There is no work carried out in full custom style for the design of a higher order (31,5) counter implemented with internal logic of modified SERF full adders in the existing literature to my knowledge. All the work reported in the literature on the compressor has been carried out either using the decomposition of synthesized logic gates or the
classic full adder structure with 28 Transistors as the basic component. Most of these works have been modeled in HDL utilizing the standard cell libraries. Also there are no previous implementations for a low power 32 X 32 bit MAC units using Dadda tree architecture utilizing an energy efficient adder in hybrid CMOS logic in full custom style. The mentioned gap in the design architecture of compressors and adders are identified and a new design is proposed and validated through a 32 x 32 MAC unit.

1.5 PROPOSED ARCHITECTURE OF ARITHMETIC MODULES

The architecture of MAC proposed consists of Partial Product Generation (PPG) logic, Partial Product Reduction (PPR) stage followed by an accumulator. The performance is mainly determined by compressor and adder cell design. The concentration is on the second step which consists in reducing the partial product array and designs a compressor algorithm which will produce fewer partial product rows. By having fewer partial product rows, the reduction tree can be smaller in size and faster in speed reducing unnecessary switching activities resulting in lower power consumption.

In literature the counter and compressor terminologies have been used interchangeably. Binary counter property has been merged with the compressor property to develop high order compressors. Uses of these compressors permit the reduction of the vertical critical paths. This approach has been widely used in fully customized circuit implementations of large multipliers where interconnection complexity and design modularity are major design bottlenecks. Based on this counter compressor idea a novel full custom implementation is proposed for fast (31,5) counter built using two (15,4) and four (3:2) blocks which in total amounts to eleven full adders. This high speed counter constitutes the partial product reduction stage of the multiplier. A 64 bit Ripple Carry Adder (RCA) is used for final addition and a
D register is used as the accumulator register for the MAC. Use of these compressors not only reduce delay but also reduce the stage of operations. This stage reduction eventually reduces the glitches and so the glitch power. Thus, by utilizing these compressors high order multiplication can be made faster without providing extra power.

There is a broad range of the implementations for the (3:2) compressors which is basically a full adder. A 24 T modified SERF full adder is proposed as (3,2) counter for low supply voltage with rail to rail output voltage swing. In addition to reduced transition activity and charging recycling capability, this adder circuit has no direct connections to power supply nodes and the entire signal gates are directly excited by the fresh input signals, leading to noticeable reduction in power consumption. The internal blocks of counters are implemented using the proposed adder.

1.6 OBJECTIVES

The research opportunities in low power VLSI arithmetic module design are aplenty. The objective of this study is to identify the shortcomings in the existing literature work and design an energy efficient architecture for an arithmetic module like MAC unit which forms the constituent part of a DSP of a bio medical device. MAC units are the major blocks of any DSP processor and energy efficient design of such a unit is a challenge. Keeping this in mind, this investigation aims at contributing to the reduction in power consumption of 32 X 32 bit MAC unit for DSP processor targeting a digital hearing aid. The performances of the proposed architectures are evaluated in terms of delay and power consumption. The main objectives of the present investigation are as follows:
To investigate and analyze the design of arithmetic circuits like adder and compressors in PPRT of MAC, in CMOS logic style with specific reference to reduction of power and delay under various supply voltages.

To design and implement energy efficient parallel multiplier in full custom style using Dadda column compression tree technique and also estimate the power consumption of multiplier in semi custom ASIC style.

To implement a fast low power MAC circuit and analyze the impact of power reduction and speed by using the proposed power efficient multiplier.

1.7 CONTRIBUTION OF THE THESIS

This investigation on design of Arithmetic modules has the following major contributions:

A novel implementation is proposed for fast (31, 5) compressor built using modified (15, 4) and (3, 2) blocks which takes 20 XOR delays instead of 21 XOR delays in a conventional design, which is 14.3 percent speed improvement.

The new implementation of (3:2) is based on the proposed modified SERF full adder of 24 Transistors with reduced delay and power consumption.

1.8 RESEARCH METHODOLOGY

An extensive literature review regarding the source of power dissipation of arithmetic circuits including column compression multiplier and MAC units has been undertaken prior to proceeding with the design step. Since minimization of power is the primary aim of this research, the starting
point for low power design is to investigate transistor behavior and characteristics in the low operating region.

The low-power MAC design problem is approached in a bottom-up fashion. Firstly adders are the most common and frequently used building blocks in the data path. Accordingly, their power consumption accounts for a significant portion of total power consumption. Therefore, a crucial first step when building a low-power system is to find adders which have good power and delay properties. A detailed study on the designs of high speed compressors is carried out which forms the partial product reduction module of a multiplier. A new implementation of (31,5) is proposed based on the new energy efficient adder and high speed compressor. 16 x 16 bit multiplier is implemented and this functional block is replicated to realize 32 x 32 bit MAC unit with 64 bit final adder and accumulator register.

1.8.1 Tools and Methodology used

The sequence of steps followed in implementing the proposed designs in full custom style is shown in the flow chart of Figure 1.2. The front end design is the transistor-level model coupled with the manufacturing models to create and simulate the circuit in an analog environment, producing accurate simulation estimates of timing, power, and area. The front-end is considered complete when the model has acceptable results based on a true floor plan and routing parasitic calculations. The final level of design, called the back-end design, is the fine-tuning and physical routing of the circuit. This level uses pre-routing, auto-routers, and routing editors to physically add and adjust the interconnection of the circuit in a model that may tapeout to the GDSII manufacturing mask standard.

A schematic is the graphical representation of the logic circuit design either by discrete devices or by logic elements. To create a schematic
design, a schematic editor is used. Symbols are created to represent the main blocks in the schematic and the primary input and output pins are added to the symbol. Pins are used to connect the symbol to the rest of a schematic. The Spectre simulation package is integrated with the Cadence tools. With the stimulus defined, we need to choose what type of analysis we wish to perform.

For functional verification setup, a transient over time analysis is experimented and to simulate different performances DC analysis is done. Then simulation is run and from the results browser the simulated waveforms are studied.

After the schematic and symbol have been designed, the next step is to move onto the layout of the circuit. The layout consists of rectangles, instances, and pins. A rectangle is used to create gate, diffusion, and metal regions for the transistor. Layout must be drawn according to strict design rules. After finishing layout, an automatic program will check each and every polygon in the design against these design rules and report violations. This process is called Design Rule Checking (DRC) and must be done for every layout to ensure it will function properly when fabricated.

This step is to compare physical layout data against fabrication-specific rules. Typical checks include spacing, enclosure and overlap. Device parameter and connectivity are extracted from the layout in order to perform ERC, Short Locator, LVS and post-layout simulation and analysis. The next successive step is parametric extraction. The mask layout contains only physical data. The extraction process identifies the devices from the layout and generates a SPICE-like netlist and other files necessary to complete the design process. Layout Versus Schematic (LVS) compares a physical layout design to the schematic from where it was designed.
Passing LVS for a circuit is critical to ensure the physical design will perform as intended when the circuit is fabricated. In LVS always verify the operation of a circuit via simulations at the schematic level before attempting to layout the cell. The design is done in a hierarchical fashion, building lower level cells before constructing larger circuit blocks from the lower level cells and hence pass LVS on lower level cells before attempting to check LVS on a higher-level cell.

The LVS Output File provides a lot of useful information about a cell, including the number of devices, nets, etc. within the cell. The netlist summary for the layout and the schematic are provided. Post layout simulation is done using the stimulus files and the parametric extracted cell view.

After a successful simulation, an output signal plot will pop up. The propagation delay time is measured by taking average of 50% of voltage levels and also the rise and fall time are measured. All of the power measurements such as static, dynamic can be made by first measuring the current drawn from the power supply over the appropriate interval of time, multiplying it by the supply voltage $V_{DD}$ and then performing calculations on the resulting waveform. Alternatively, in the result browser we can determine the current (i) and voltage (v) of the circuit and find out the average power using $\text{pwr} = v \times i$.

The following tools from Cadence tool suite has been used for this work. For the transistor level schematics of all the designs in full custom style the process design kit (PDK) provided by Cadence Foundry Solutions in 180nm CMOS technology, 1.8V has been used with Virtuoso® Schematic Composer. Analog Design Environment (ADE) is used for DC analysis of adder, compressor and MAC circuits. For design simulations and SPICE net
list generation SPECTRE simulator have been used. All layouts were created using Virtuoso® Layout Editor and Assura for Design Rule Check (DRC), LVS and RCX Layout verification were used. RC extraction was successfully done and tape out format Graphical Data Stream Information Interchange (GDSII).

Figure 1.2 Full custom design flow

1.9 OVERVIEW AND THESIS CHAPTER ORGANIZATION

This chapter presents a brief introduction of the field of VLSI Design. A review of literature is done where the low power design space
exploration with specific reference to arithmetic modules are reviewed. The circuit design architecture of arithmetic modules is proposed to overcome the short comings in the existing literature. The comparison results show that the proposed architecture for the adder shows better power delay product than the existing design for the same specified conditions. High speed compressor architecture is also proposed using the 1 bit adder cell architecture. This shows better performance in terms of delay and power consumption when implemented in 32 x 32 bit multiplier architecture. A block wise shut down technique for the compressors are proposed which reduces power by appreciable amount. A 32 x 32 MAC unit is proposed using the said high speed compressor to improve its speed and power performances. The power consumption of the proposed design of MAC in full custom style is compared with the results of RTL level power estimation using Cadence tool suite. The numerical results for power dissipation and delay are validated for different simulation scenarios and compared with RTL results.

The remainder of the thesis is organized as follows.

**Chapter 1** gives a brief introduction of field of Low Power VLSI design and presents the motivation for this research study. This chapter also identifies the problem definition and the scope of this work.

**Chapter 2** presents the existing literature on Design, Implementation of adder circuits and comparison with proposed design. The results of power reduction and delay are also compared with existing adder cells.

**Chapter 3** presents the proposed architecture of the higher order compressor by comparing the scenario of low power multiplier design with column compression techniques already existing in literature.

**Chapter 4** analyses the design implementation of the proposed MAC architecture in full custom design style for digital systems. The power
consumption of proposed MAC with specific reference to low power devices like hearing aids is presented.

Chapter 5 presents the power estimation of 32 bit multiplier and MAC at RTL level using standard cells library.

Chapter 6 summarizes the findings of this work and the scope for future work.