ABSTRACT

The increasing demand for portable electronic devices has led to emphasis on power consumption within the semiconductor industry. Power is a problem when cooling and battery are a concern. However, there is no universal way to avoid tradeoffs between power, delay and area, and thus designers are required to choose appropriate techniques that satisfy application and product needs. At the circuit level, an optimized design is desired to avoid any degradation in the output voltage, consume less power, have less delay in critical path, and be reliable even at low supply voltage as we scale towards deep sub micrometer. A majority of portable multimedia and biomedical devices which meet the requirement of small size, ultra-low power are Digital Signal Processing (DSP) circuits interfacing with real-world acting as personal aid devices. Speaking of DSP processors, one of the main processing bottlenecks is the Multiply and ACcumulate unit (MAC) whose area and speed are the most important factors. But increasing speed also increases the power consumption, so there is an upper limit of speed for a given power criteria. A fast and energy-efficient multiplier is always needed in MAC of DSP, image processing and arithmetic units in microprocessors contributing to the total power consumption of the system. Considering the battery operated portable multimedia devices, low power and fast designs of multipliers are more important than area. Therefore the driving motivation for this research study is to investigate multiple architectures and circuit design techniques for arithmetic modules in MAC unit that are suitable to achieve low power consumption with high speed. The design of a low power, high speed multiplier architecture for a MAC unit and its implementation with power estimation is the goal of this thesis. From the comparative analysis of
the full adders for a supply voltage of 1.1v it is proved that the proposed adder shows an improvement of 37.3 percent in terms of power saving compared with static CMOS full adder in 90 nm at 200 MHz with negligible area overhead. The proposed full adder design has been compared with static CMOS, TG adder, Multiplexer based adder cells existing in literature and it shows 31.16 percent improvement in terms of PDP at 100 MHz 180 nm technology at 1.8v.

The Simulations were also conducted for different frequencies, i.e. 5MHz, 50MHz, 100MHz, and 200MHz for different supply voltages ranging from 0.7v to 1.5v in both 180 and 90 nm technologies. Approximately 400 input patterns are applied to the multiplier to verify its functionality. All the 3 variations of MAC implementations have been simulated using a common test setup in Cadence®. The 32x32 bit MAC unit designed using proposed full adder as the basic building block gave a power saving of 24.27 percent over 32 bit MAC designed using SERF full adder and 35.07 percent power savings over 32 bit MAC designed using conventional 28T static CMOS full adder.