CHAPTER 6

CONCLUSION AND FUTURE SCOPE

The research work has addressed the possibilities of improving the design of Non-binary LDPC decoder at the algorithmic level. Non-binary irregular quasi-cyclic LDPC decoder has been designed with two variations of the algorithm. This includes different code construction methods and message reduction technique. Three different code construction methods, namely, LDPCM, DDPCM and HDPCM are proposed with the variation in the parity check matrix structure. The decoding performance of all these code construction based decoder techniques have been analyzed for message passing algorithms such as FFT-SP algorithm, Min-sum algorithm and Min-max algorithm. The impact of these matrices have also been analyzed in terms of the computation strength and other terms like Girth, Sparsity, Degree Distribution, EXIT chart and covering radius. Comparing the proposed three matrix variations, LDPCM based decoder has its significance in terms of reduced computation strength with nominal decoding performance. Also, HDPCM based decoder has the better decoding performance than the other two matrix structures based decoder. These statements also agree over the above mentioned three decoding algorithms.

Even more, to make a better trade-off between the decoding performance and computation strength of the decoding algorithm, a variable threshold based message reduction technique has been proposed. The effectiveness of this technique has been evaluated in terms of the computation strength. The reduction of the computation strength at CNU and VNU has been inferred as 68% and 43%, in terms of multiplication and addition respectively.
To strengthen the analysis of the proposed algorithmic variations, stochastic computation based decoder and protograph based decoder are also taken into consideration. The above inferences for the probabilistic codes, applies for the stochastic and protograph based LDPC codes.

The inclusion of these two variations of the decoding algorithm has been transformed into hardware architecture design of the decoder. The architecture has been targeted to IEEE 802.11n standard, with the specification of code length 648, rate 1/2 code, BPSK modulation and considers AWGN channel model. The proposed different code construction methods supports in scheduling the CNU and VNU for semi-parallel operations. For the FFT-SPA based Non-binary LDPC decoder, the effect of message reduction reflects in the power reduction of 18% and 4% in CNU and VNU, respectively. The power reduction of the decoder with message reduction and code construction methods (LDPCM, DDPCM and HDPCM) are evaluated as 1.86%, 1.32% and 3.72%, respectively. The decoder architecture also presents the nominal area consumption with the throughput of 480Mbps. This research work suggests HDPCM based Non-binary LDPC coder suitable for better decoding performance and optimized hardware complexity. This method also supports in terms of reduced power consumption.

The proposed code construction methods and message reduction approach has been tested only for the codes over GF (4), over AWGN channel and with BPSK modulation. The reliability of the decoder has been tested only for the rate 1/2 and 648 code lengths. The designed architecture is mainly focused towards the better performance and optimized hardware complexity but not towards the area optimization and throughput improvement.
FUTURE SCOPE

The algorithmic improvements suggested in this research work can be extended in different directions as:

The proposed code construction methods can be applied to the decoder of different code rate and wide range of code length. The impact of this algorithmic variation can be analyzed for different channel conditions.

The designed decoder can be employed with the image transmission systems, wherein the concept of cellular automata can be inculcated to optimize the computation complexity.

Joint encryption and error correction methods can be evolved, thereby attaining both secure and reliable data transfer in applications like satellite communication and underwater communication.

At the hardware realization of the decoder architecture, various numerical strength reduction techniques can be employed to improve the throughput and reduce power consumption.

The significance of reconfigurability in FPGA based designs can be explored to design a rateless codes, with the suggested algorithmic improvements of LDPC decoder.