CHAPTER 7

RESULTS OF HARDWARE DEMODULATOR

7.1 VERIFICATION

Fig. 7.1 shows the blocks of the part of the demodulator implemented using Verilog and, the necessary Matlab modules required for its verification. Matlab generates the input signal for the Modulator. For the sake of testing, ten sine wave frequencies, 2 KHz to 20 KHz, one at a time, are used as input. The Matlab Modulator output is signed, 16 bits wide. This serves as the input for both the Matlab and Verilog demodulators as shown. It may be noted that the input to the Verilog demodulator is MSB 12 bits (and not the entire 16 bits) so as to keep the same precision as the ADC output in the existing ADSP implementation. 16-bit precision has been retained for the input to the Matlab demodulator since it serves as a better standard reference for verifying the Verilog implementation. The modulated signal, thus produced, is applied to both the Matlab and Verilog demodulators.

The I and Q channels are the required outputs, and are each of width 16 bits, signed. The Verilog design requires two clocks, clk_bit (13.056 MHz) and clk_word (1.536 MHz) for its operation. The I and Q outputs from Verilog demodulator compare favorably with the corresponding outputs of Matlab demodulator, which has served as the reference for verification of the hardware implemented on FPGA. Matlab and Verilog Response of I channel and Q channel results for various frequencies ranging from 2 KHz to 20 KHz are shown in figures. 7.2 to 7.21. They present the modulated input from the Matlab and the
demodulator outputs (both in-phase and quadrature parts) assuming sinusoidal signals of frequencies 2 KHz to 20 KHz as modulating signals from the Matlab Modulator. In each of these figures, the first (top) window presents the modulated signals to the Demodulator. The second (middle) window presents the output of the Matlab based demodulator (indicated in blue) overlapped with those from that of the Verilog based demodulator hardware design (indicated in red). Further, in the third (bottom) window, part of the demodulator window (shown in the middle window) is magnified to depict the details in a clear manner. In all these cases, the hardware design output from the Verilog based design is found to be in agreement with the simulated results obtained using Matlab.

**Figure. 7.1** Blocks of the Part of the Demodulator Implemented Using Verilog and the Matlab Modules for its Verification
The synthesis part of the demodulator, Top layer thro’ the Bottom most layer of the FPGA implementation is depicted in Fig. 7.22 through Fig. 7.29. These levels present different functional entities of the FPGA based demodulator. Design summary of the final FPGA design is presented in Fig. 7.30.
Figure 7.2 Matlab and Verilog Response of I channel and Zoomed View of I Channel at 2 KHz
Figure 7.3 Matlab and Verilog Response of Q Channel and Zoomed View of Q Channel at 2 KHz
Figure 7.4 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 4 KHz
Figure 7. 5 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 4 KHz
Figure 7. 6 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 6 KHz
Figure 7. 7 Matlab and Verilog Response of Q Channel and Zoomed View of Q Channel at 6 KHz
Figure 7.8 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 8 KHz
Figure 7.9 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 8 KHz
Figure 7. Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 10 KHz
Figure 7.11 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 10 KHz
Figure 7.12 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 12 KHz
Figure 7.13 Matlab and Verilog Response of Q Channels and Zoomed view of Q Channel at 12KHz
Figure 7. 14 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 14 KHz
Figure 7. 15 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 14 KHz
Figure 7. 16 Matlab and Verilog response of I channels and Zoomed view of I channel at 16KHz
Figure 7. 17 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 16 KHz
Figure 7. 18 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 18 KHz
Figure 7.19 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 18 KHz
Figure 7.20 Matlab and Verilog Response of I Channels and Zoomed View of I Channel at 20 KHz
Figure 7.21 Matlab and Verilog Response of Q Channels and Zoomed View of Q Channel at 20 KHz
Figure 7.22 Top Level of the FPGA Part of the Demodulator
Figure 7.23 Internal of top level Synthesis RTL View of FPGA Part of the Demodulator
Figure 7.24 Clock Generator Internal Synthesis RTL View of FPGA
Figure 7.25 ROM Internal level 1
Figure 7.26 ROM Internal level 2
Figure 7.27  ROM Internal level 3
Figure 7.28 ROM Internal level 4
Figure 7.29 Internal View of Mixer
Figure 7.30 Design Summary of Demodulator