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VISIBLE LIGHT EMISSION FROM SILICON MOSFETS

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Abstract—We observe visible light emission from Si MOSFET beyond source–drain breakdown. The intensity as well as location varies with gate bias. For zero gate-voltage \( V_g \) light is seen from four sides of the drain region. But for positive \( V_g \) values to \( V_d \) the drain–gate boundary and has a peak in emission intensity at a certain gate bias beyond which it decreases. The initial increase in light intensity is attributed to minority-carrier injection and the decrease at higher gate bias is due to a reduction of lateral field beyond pinch off, which causes a decrease in carrier multiplication. For negative gate bias, the source–drain breakdown voltage decreases and hence the light intensity increases. A theoretical model for the drain current beyond breakdown is presented and compared with experimental light-intensity curves. The substrate current, which is a measure of the avalanche mechanism by an electron–hole pair generation in the drain depletion region, is measured and compared with light-intensity values.

INTRODUCTION

It is well known that visible light emission occurs from silicon \( p-n \) junctions at reverse biased breakdown\[1, 2\]. However, this phenomenon has been little discussed for MOS (metal-oxide-semiconductor) discrete devices as well as ICs. The mechanism of photon generation in reverse-biased \( p-n \) junctions is due to intraband transitions between heavy and light-hole bands and interband transitions of carriers between conduction and valence bands\[3\]. Hence, carrier generation–recombination and the related photon emission is an essential subject to understand high field phenomena in semiconductor devices.

In the case of MOSFETs (metal-oxide-semiconductor field-effect transistors), the field distribution in the source–drain depletion region is different from that for simple \( p-n \) junctions. The presence of the gate electrode induces minority-carrier injection into the drain depletion region\[4, 5\]. As the drain–substrate junction is reverse biased, electron–hole pair generation occurs in the accompanying depletion region. If the gate voltage \( V_g \) is increased positively, electrons are injected from the channel into the reverse-biased drain depletion region. This causes an increase in carrier generation through impact ionization. The electrons which have energy higher than the Si–SiO\(_2\) barrier height (3.2 eV) are injected into the Si\(_{2p}\) causing gate current to flow\[6\]. On the other hand, holes move to the substrate, causing the flow of substrate current\[7\]. Hence, the variation of gate and substrate current with various modes of device operation is a measure of the avalanche multiplication phenomenon in the drain–source depletion region. Since the origin of these two types of current is the same, Tanaka et al.\[8\] presented a simple formula relating the above two currents, from which one can be evaluated if the other is known. As the device dimensions are scaled down with the advancement of technology there exists a very high electric field even for a low biasing voltage. Hence, hot carriers generated due to this high field can recombine resulting in photon emission. Recently, studies have been made on light emission from GaAs MESFETs (metal-oxide-semiconductor field-effect transistors)\[9\] as well as Si MOSFETs\[10\]. However,\[10\] does not give any quantitative analysis of the variation of light intensity with different modes of the device operation. This paper presents a detailed study on light emission whose intensity, as well as position, varies with different bias conditions.

In a MOSFET at high \( V_g \) values the saturation channel current multiplied by avalanche multiplication factor through drain–substrate depletion region reaches the drain region. Hence, the excess current produced by electron–hole pair generation by avalanche process adds to the usual saturation channel current to give the drain current. The generation–recombination component of drain current is termed avalanche drain-current \( I_{dav} \) and is a measure of photon generation. A theoretical model is presented for \( I_{dav} \) and the calculated values are compared with experimentally obtained light-intensity data. A good agreement is obtained for the variation of both \( I_{dav} \) and light intensity with gate bias. Since the origins of the substrate current and
the photon emission are the same, i.e. due to avalanche mechanism of carrier generation, a comparative study is made of these two quantities. It is seen that the intensity of light emission follows similar behaviour as substrate current, but its peak position with respect to $V_g$ is different. The photons generated in the $p-n^+$ junction when observed in the substrate generate electron–hole pairs, which degrades the MOS random-access memory (RAM) refresh time [11] and causes an upset in logic circuits [12]. Hence, the photon emission or absorption process in MOS devices is an important research topic that should be studied in detail. This paper presents a detailed study of the physics of various high field phenomena in MOS devices.

The experimental procedures and the results are presented in Section 2. In Section 3 the theoretical models of the avalanche drain-current and substrate current are presented. In Section 4 both the theoretical calculation and experimental results are compared and discussed. Finally, Section 5 summarizes the main results arrived at in this work.*

II. EXPERIMENTAL PROCEDURE

(i) Device fabrication

The MOS field-effect transistor was fabricated on a $5 \Omega \text{cm} (100)$ $p$-type Si with $(500 \mu)^2$ gate area by standard N-MOS technology. Different processing parameters were Boron field-implantation of $5 \times 10^{12}/\text{cm}^2$ dose at $120 \text{ keV}$, $x_j = 1.8 \mu$, $d = 0.12 \mu$ and Ti–Au double layer metalization. A grating structure having $20 \mu$ periodicity with $6 \mu$ width of gold metal was made on the top of the gate electrode. The grating structure was made to observe IR radiation from the gate area and in fact is not important for the present visible light emission study. The device was mounted and bonded on a To-5 header. The processed chip is shown in Fig. 1. The source–drain breakdown voltage of the fabricated MOSFET is $50 \text{ V}$.

(ii) Measurements

Visible light is seen in a dark room to be emitted from the MOS transistor when the drain bias exceeds the breakdown value. A linear increase of light intensity with drain bias is observed. Initially with zero gate voltage, light is seen emitting from four sides of the drain region. As $V_g$ is increased positively, the light intensity is observed to decrease from the outer sides of the drain region and to concentrate at the drain–gate boundary. The intensity of light from the drain–gate boundary initially increases with gate bias and after reaching its peak value it decreases. The variation of drain current with gate bias is shown in Fig. 2(a). Figure 2(b) shows a light-emission photograph from the drain–gate boundary. The chip was placed on an IC prober under a Bausch & Lomb microscope fitted camera. The photograph was taken in two steps using high-speed Polaroid film. The first exposure was made with faint light falling on the chip and later in a dark environment for one hour by biasing the device. Since after long exposure the photograph could not be taken properly, the line shown in Fig. 2(b) is drawn by hand to show the light emission from drain–gate boundary. The light intensity is measured by using an EMI 6094B-model photomultiplier tube with Si11 spectral response characteristics. The detail measurement procedure is given in [13].

The measured light intensity is plotted against various gate voltages as shown in Fig. 3. Measurements were done for three different drain-bias values. A higher $V_D$ corresponds to higher electric field, therefore a higher $V_g$ is required so as to reduce the lateral field for avalanche multiplication. Hence the peak position shifts to higher $V_g$ values.

When the gate is negatively biased there will not be an electron channel from source to drain. In this case the device operation is said to be similar to that of a gated diode. For each increase of negative gate-bias step the breakdown voltage occurs at lower $V_D$ values as shown in Fig. 4(a), in which the mini-

Fig. 3. Light intensity vs gate voltage.
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Fig. 1. Photograph of processed chip.
Fig. 2. (a) $I-V$ characteristics of MOSFET for positive gate voltages. (b) Light emission at drain–gate boundary.
Fig. 4. (a) $f-V$ characteristics of the device for negative gate voltages. (b) Light emission of four sides of drain region.
mum gate pulse amplitude starts from right and goes on increasing to left. The current beyond breakdown increases and so does the light intensity. As the photograph of Fig. 4(b) shows, light emission occurs from four sides of drain region for negative gate-bias values. The intensity of light emission for negative gate-bias is measured and plotted as shown in Fig. 5. Within the limit of applied gate-voltage an approximately linear increase of emissivity occurs. In this case a higher drain-bias corresponds to a higher lateral field. Therefore it is natural that the light emission is stronger for higher $V_D$ values.

We have measured the substrate current of the device under similar conditions for light emission. The measurement was done in the dark by using a Keithley 602-model electrometer. The substrate current is plotted in Fig. 6 vs $V_g$ for three different $V_D$ values. With increase of gate voltage, the substrate current first increases and after reaching a maximum decreases. It follows similar behaviour as the light-intensity curve, except for the fact that the peak position occurs at lower $V_g$ values. The reason for this phenomenon is discussed in Section 4.

III. THEORETICAL APPROACH

(a) Avalanche drain-current

In this section the results of the calculation of the drain current due to multiplication of saturation channel current are presented. The inset of Fig. 7 describes the schematic diagram of the device and the relevant current paths in the $n$-channel MOSFET. The channel current leaves the surface at the so-called pinch-off point and flows deep within the substrate to reach the drain region. The electric field is highest just beneath the surface. The primary channel current is multiplied by the high electric field at the drain–substrate depletion boundary. Thus the drain current is given by

$$I_D = M I_s,$$

where $I_D, I_s$ are the drain and channel current, re-
Fig. 7. Insert shows schematic diagram of the MOSFET. Calculated \( I_{DSat} \) vs gate voltage.

spectively, and \( M^* \) is the multiplication factor. The channel current at the pinch-off point is the saturation drain-current and depends only on the gate voltage through the following relation[14]:

\[
I_s = I_{DSat} = \frac{mZ}{L} \mu_n C_i (V_g - V_T)^2. \tag{2}
\]

The light emission occurs after the source–drain breakdown is reached beyond which the drain current rapidly increases. The avalanche drain-current is defined here as the excess drain current added to the normal channel current due to the flow of highly energetic carrier generated by avalanche mechanism in drain depletion region. It is given by

\[
I_{Dav} = I_D - I_{DSat} = (M^* - 1) I_{DSat}. \tag{3}
\]

\( I_{Dav} \) is a measure of photons generated in reverse-biased drain junction. To derive the expression for the multiplication factor, it is assumed that the electron current initiates the carrier multiplication. The ionization integral is given by

\[
1 - \frac{1}{M^*} = \int_0^{E_M} \alpha_e \exp \left[ -K \int_0^{E_M} (\alpha_e - \beta_p) \, dE' \right] \, dE,
\tag{4}
\]

where \( K = \epsilon/\Omega N_a \), \( \alpha_e \) and \( \beta_p \) are the ionization coefficients of electrons and holes, respectively. The above integral is calculated by the methods in [15], in which the actual depletion width \( W \) is replaced by an equivalent one having a uniform field \( E_M \) and depletion width \( W_{eq} \). Thus, after simplification

\[
1 - \frac{1}{M^*} = \frac{\alpha_M}{\beta_M - \alpha_M} \exp \left[ (\beta_M - \alpha_M) W_{eq}(E_M) - 1 \right]. \tag{5}
\]

The exact expression of \( W_{eq}(E_M) \) can be expressed with respect to an abrupt junction by the relation\( W_{eq}(E_M) = m_n W \) with \( m_n \) being a proportionality factor. The value of \( m_n \) depends on the electric field \( E_M \). At the breakdown field \( E_B \), the left-hand side of eqn (5) is equal to 1. Hence, \( m_n \) can be approximated from the above equation to the following relation for \( E_M > E_B \)

\[
\ln \frac{\alpha_B/\beta_B}{\alpha_B - \beta_B} = \frac{m_n}{kT} \frac{K E_B}{E_M} \tag{6}
\]

where \( \alpha_B \) and \( \beta_B \) are ionization coefficients at field \( E_B \). The field-dependent ionization formula is taken to be \( \alpha_n = A_n \exp \left[ -b_1/E_M \right] \) for electron and \( \beta_p = B_p \exp \left[ -b_2/E_M \right] \) for hole[16]. Hence, we can write
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the eqn (5) as

\[
1 - \frac{1}{M^*} = \frac{\alpha_m}{\beta_m - \alpha_m} \exp \left( \frac{\beta_m - \alpha_m}{\beta_m - \alpha_m} \right) \times \left[ \frac{E_m}{E_m} \left( \ln \frac{\alpha_m}{\beta_m} \right) - 1 \right].
\]  

(7)

The maximum lateral field at the drain-substrate depletion region depends upon \( V_D \) and \( V_g \) through the following relation:

\[
E_M = \sqrt{2/K} \left( V_D - \left( V_g - 2 \Psi + K_1 \right) \left( 1 - \sqrt{1 + 2 \frac{V_D}{K_1}} \right) \right)
\]  

(8)

where \( K_0 = \sqrt{\epsilon qN_A / C_i} \). Now the avalanche multiplication factor can be evaluated at the field \( E_M \) from the eqn (7). With the help of eqn (3) we get the expression for avalanche drain-current as

\[
I_{Dav} = \left[ (M^* - 1) \frac{mZ}{L} \mu_e C_i (V_g - V_T)^3 \right].
\]  

(9)

It is seen that \( I_{Dav} \) depends directly on \( V_D \) and \( V_g \). Equation (9) is solved numerically for different gate voltages with three different \( V_D \) values. The result of the calculation is shown in Fig. 7. All other parameters taken are as given in Table 1.

It is seen from Fig. 7 that \( I_{Dav} \) increases initially with \( V_g \), and after reaching a maximum it decreases. From eqn (3) we have seen that \( I_{Dav} \) depends on both \( M^* \) and \( I_{DSat} \). With the increase of gate voltage, \( I_{DSat} \) increases but \( M^* \) decreases. When these two factors compromise we get a peak in avalanche drain-current. The avalanche multiplication factor

\[
M^* \text{ will be more for higher } V_D \text{ values. Hence the peak position will be at higher } V_g \text{ values from which decrease of } M^* \text{ predominates.}
\]

(b) Substrate current

- A theoretical model has been presented by Kamata[7], who assumed that the substrate current \( (I_{Sub}) \) of a MOSFET is directly proportional to the drain current \( I_D \) when the device is being operated in its linear and saturation region. For the case of light emission from the device, the drain voltage exceeds its breakdown value and hence the drain current \( I_D \) is multiplied by the avalanche multiplication factor \( M^* \), so we get

\[
I_{Sub} = M^* I_D \alpha_a \Delta L.
\]  

(10)

\( M^* \), \( I_D \) and \( \alpha_a \) are defined in the preceding section, and \( \Delta L \) is the pinch-off length between the drain and the end of the inversion layer, given by

\[
\Delta L = \frac{V_D - V_{DSat}}{E_T}.
\]  

(11)

The transverse electric field is the sum of the following three components:

(i) The electric field \( (E_1) \) due to fixed charge on the reverse-biased drain junction, which is given by

\[
E_1 = \frac{\sqrt{qN_A (V_D - V_{Dsat})}}{2 \epsilon \varepsilon_0}.
\]  

(12)

\[ Fig. 8. \text{ Theoretical } I_{Sub} \text{ vs gate voltage.} \]
(ii) The field \( E_2 \) due to the potential drop between drain and gate, at the drain side of the depletion width region, is given by

\[
E_2 = \frac{\varepsilon_0 V_D - V_g}{d}
\]

(iii) The third component \( E_3 \) is due to the potential drop between gate and end of inversion layer, is given by

\[
E_3 = \frac{\varepsilon_0 V_g - V_{DSat}}{d}
\]

where \( a \) and \( b \) are empirical fringing factors \((a = 0.2, \ b = 0.6)\) and \( d \) is the oxide thickness. Now the transverse electric field \( E_T = E_1 + E_2 + E_3 \) is calculated by above formulas and hence, on substitution in eqn (10), we get values of the substrate current. The calculated values are plotted in Fig. 8 for three different drain voltage values. Both the theoretical and experimental substrate current (Figs. 8 and 6) have peak position at same \( V_g \) values. But from the comparison with \( I_{sat} \) values in Fig. 7 it is seen that \( I_{sat} \) has its peak at relatively lower \( V_g \) values than \( I_{DSat} \).

**DISCUSSION**

From our experimental observation we conclude that the electric field intensity is a maximum at the curved junction as light is seen first from four corners of the drain region beyond the source-drain breakdown. Since the drain region has a comparatively large area, its light is seen clearly under the microscope. As the gate voltage is increased positively, the position of light emission shifts to the drain–gate boundary. Hence for positive \( V_g \) values minority-carrier injection occurs only at the drain–gate boundary. For low positive values of \( V_g \) the light intensity increases and the emission pattern becomes sharper. As the gate-bias value increases, the light intensity reaches its peak at a certain \( V_g \) and then decreases. It is also observed that for higher \( V_g \) values the light emission vanishes for a particular \( V_D \) value. This is due to the decrease of lateral field, which reduces the avalanche multiplication of carriers in the drain–substrate depletion region.

In the theoretical calculation \( I_{DSat} \) is taken to be a function of both \( M^* \) and \( I_{DSat} \). As \( V_g \) is increased, \( M^* \) decreases and \( I_{DSat} \) increases. For lower \( V_g \) values, increase of \( I_{DSat} \) predominates due to minority-carrier injection. For higher \( V_g \) values, a decrease of \( M^* \) predominates, resulting in a decrease of \( I_{DSat} \). Thus the model is capable of giving a qualitative explanation of the gate-bias effect on emission intensity from the MOSFET. Good agreement between experimental results and theoretical calculation is achieved with respect to peak position of different curves. The \( V_D \) values taken for theoretical computation are higher than experimental source–drain breakdown voltage because in the theoretical approximation \( E_m \) is taken to be greater than \( E_B \). All other parameters taken for computation are realistic values for light emission conditions. From Figs. 3 and 7, it is concluded that intensity of light emission follows similar behaviour as \( I_{DSat} \). The present study also confirms the earlier approximation [17] for simple \( p-n \) junctions, that light emission is proportional to junction current beyond breakdown. We have not studied the effect of gate bias on the spectrum of light emission but do believe this would result in interesting conclusions.

When a negative bias is applied to the gate of a MOSFET, it behaves as a gated diode. The breakdown voltage for each negative gate-pulse voltage decreases. It is seen from Fig. 4(a) that as the height of the negative gate-bias pulse is increased, i.e. curves from right to left, the breakdown voltage decreases and current beyond breakdown increases. In this case, approximately, a linear increase of light intensity with negative gate-bias is observed as shown in Fig. 5. A higher drain voltage corresponds to higher electric field for avalanche multiplication and the light intensity is higher for these values. It is observed that light is emitted from all four sides [Fig. 4(b)] of the drain region. Due to the field implantation of boron atoms the surface of silicon at drain boundaries has excess of \( p \)-type impurities relative to the bulk. As the gate bias is increased negatively, holes accumulate at the surface and get a conducting path to the four sides of drain region. Hence surface breakdown occurs at four sides simultaneously and thus light starts emitting with high intensity from drain boundaries.

As for the substrate current, the substrate current due to flow of holes from drain depletion region is a measure of avalanche mechanism of carrier generation in NMOS transistors [18]. We have measured the substrate current under a similar condition for light emission. The experimental results and theoretical calculations are shown in Figs. 6 and 8. They are in good agreement except that the magnitude of the experimentally observed current is higher. This may be due to the fact that, experimentally, the depletion width may be greater than the theoretically assumed case. From a comparative study of the light-intensity curves (Fig. 3) and the substrate current curves (Fig. 6) it is concluded that both the terms behave similarly with gate bias, but the peak position of the light-intensity curves occurs at higher \( V_g \) values than that of substrate current. The substrate current is directly proportional to the electron ionization coefficient which depends on maximum electric field at drain junction. Since \( V_g \) causes a direct reduction of electric field, at lower \( V_g \) values, the lowering of \( E_m \) predominates. Thus the substrate current attains a peak at lower gate-voltage than the light intensity.

**CONCLUSION**

The effect of gate bias on light emission from Si MOSFET is studied in detail. We believe the variation of light intensity with gate bias from a field-effect transistor is presented for the first time. For low positive gate voltages the light emission is con-
centrated at the drain–gate boundary. After reaching a maximum intensity, the light emission decreases for higher \( V_g \) values. A numerical model of junction current beyond breakdown has been presented. The comparison of light-intensity values and \( I_{Dav} \) confirms the fact that light emissivity is proportional to avalanche drain-current in a MOSFET. When the gate is negatively biased the drain depletion region behaves as a gated diode. In this case breakdown and the light emission occur from four sides of drain boundaries. The substrate current, which is believed to be due to avalanche multiplication of carriers in the drain depletion region, is calculated theoretically and measured experimentally. Both results agree with each other with respect to their peak position for various gate bias values. We conclude that for higher drain-voltage values, light-intensity measurement gives the quantitative measure of both generation and recombination of carriers in the drain–substrate depletion region and hence can be utilized as an useful tool for studying high field phenomena in MOSFETs.

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REFERENCES

Light Emission from Si Junctions

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ABSTRACT

Visible electroluminescence from silicon p-n junctions, schottky junctions and MOSFET devices is reviewed. The spectrum of reverse bias emission is interpreted in terms of intraband and interband transitions of carriers in the silicon band structure. In the case of reverse biased schottky barrier with silver, an additional peak is observed probably related to the excitation of plasmons in silver. The light emission from MOS transistors for various gate bias conditions arises from avalanche multiplication in the drain gate depletion region. Various cases such as linear variation and saturation in light emission in depletion mode device are considered.
1. INTRODUCTION

Visible electro luminescence from p-n junctions has been known and studied for the past several years [1,2]. We report here the luminescence from silicon p-n junctions, Schottky junctions and MOSFETs.

2. P-N JUNCTION

In a silicon p-n structure the reverse current starts growing sharply above the breakdown voltage and is usually accompanied by light emission above a threshold value of current. The spectral response of the visible light emitted from the surface of a shallow p+n+nn+ diode is shown in Fig. 1. The physical interpretation of the spectrum is based on intraband transitions between heavy and light hole bands and on interband transitions between conduction and valence bands as indicated [3,4] in the inset in Fig. 1. The cut-off wavelength (630 nm) is reached when holes reach their ionization energy \( \frac{\hbar W_{\text{low}}}{m^*_{\text{oh}}} \) (1 - \( m^*_{\text{oh}} / m^*_{1h} \)), where \( E_{\text{oh}} \) is the threshold energy for pair production by a hole and \( m^*_{1h} \) and \( m^*_{2h} \) are effective masses of the light and the heavy hole respectively. \( E_{\text{oh}} = 2.9 \text{ eV} \) and \( m^*_{1h} / m^*_{2h} = 0.32 \). The high frequency limit is given by interband transitions:

\[
\hbar \omega_{\text{high}} = E_{\text{oe}} \left( 1 + \left( \frac{m^*_{2h}}{m^*_{1h}} \right) \right) \left( K_c^2 / (K_c - K_0)^2 \right) + E_G, \]

where \( K_0 \) is the wave vector for conduction band minimum (2/3 \( K \) for silicon), \( E_{\text{oe}} \) is ionization threshold (1.0 eV) for an electron and \( m^*_{1h} \) is the effective mass of a conduction electron, \( m^*_{2h} = 1.94 \), \( K_c \) is the wave vector of recombining electron and \( E_G \) is the band gap. For \( K_c = 0.26 K \) in \( \langle 100 \rangle \) direction, we obtain a cut-off \( \lambda_{\text{high}} = 360 \text{ nm} \) for the high frequency limit.

3. SCHOTTKY JUNCTION

Visible electroluminescence has been observed in a silver n-silicon Schottky structure. When the structure is reverse biased, visible light is emitted from the diode surface and its intensity increases with the current across the junction.

The spectral response of the device is shown in Fig. 2. The device is biased to 50 to 100 mA reverse current with voltages up
to 30 V. The measurement was carried out by using EMI 6094 photo-multiplier tube together with narrow passband filters. The light output increases with reverse current and it is higher for longer wavelength, except for a small peak at 390 nm.

The energy levels of a metal-n silicon junction, under reverse bias condition are shown in the inset in Fig. 2. With increase in the reverse voltage, the thermionic field (T-F) emission and field emission (F) of the carriers result in increase in the reverse current. These carriers are energised by the high field across the junction causing carrier multiplication leading to emission of photons. With the increase in reverse current the number of the carriers increases which enhances light output. The increase in photon yield at longer wave lengths is due to interband and intraband transitions as described earlier. The peak at 390 nm is probably due to silver plasmon excitation by the hot carriers [5, 6].

4. MOSFET

Visible light emission is seen at drain and gate regions for various ranges of operation of the device. This phenomena is similar in nature to the light emission from reverse biased p-n junction, however, the field distribution which causes the avalanche multiplication is modified by the gate voltage [7, 8]. We have studied this phenomena for buried channel MOSFET devices.

The structure of the device is shown in inset of Fig. 3. Depletion type transistors are fabricated by phosphorous implantation through the gate oxide at 140 Kev with three different doses before metalisation. The chip is mounted on a To-5 header. The visible light emission can be observed by naked eye adopted to darkness. Light output is measured by PMT as mentioned above.

In figure 3, the light output is plotted against the gate voltage for the various depletion mode devices. For low dose implantation channel there exist low peaks in the output, the peak disappears for higher dose of the channel implant and the output decreases monotonically with gate voltage. For low dose implants, the channel conductivity is modulated with bias and it has a maximum. The channel current is injected into the avalanching drain region giving a maximum in multiplication current with bias and consequently a peak in the light output. This does not happen in the higher dose channel as the channel conductivity is already high to begin with and cannot be increased further by gate bias. If the gate bias is increased, the channel current cannot increase but the drain saturation voltage is increased. A reduction in the lateral field
ensues in the channel region near the drain \cite{9,10}, the multiplication decreases and thus the light output is reduced with gate bias.

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References


Fig. 1. Spectral response of a light emitting silicon p+ n+ nn+ device under reverse bias; energy bands in Si and optical transitions in the inset.
Fig. 2 Spectral response of a light emitting silver-n-silicon schottky diode in reverse bias; energy levels under reverse bias with TF and T emission.
Light emission for different buried channel MOSFET's.

Depletion implant doses are (i) $1 \times 10^{12} / \text{cm}^2$
(ii) $5 \times 10^{12} / \text{cm}^2$ (iii) $8 \times 10^{12} / \text{cm}^2$. Inset shows the MOSFET structure.