CHAPTER - IV

HOT CARRIER EFFECTS IN DEPLETION MODE MOSFET

4.1 Introduction

The depletion mode MOS transistors are increasingly used as the load element in conjunction with enhancement mode drivers. The use of depletion mode transistors as load device offers the following advantages [61].

i) Large voltage gain per stage

ii) Improvement of the power delay product

iii) Reduced size per inverter

The depletion mode or normally on MOSFET is fabricated by implantation of oppositely charged carriers to that of the substrate in the gate region. In general for p-type silicon, Group V elements like phosphorous, arsenic and antimony are used for fabrication of depletion mode transistors and Group III elements like boron and indium are used for controlling the threshold voltage of enhancement mode transistor. Depending on the energy of the implanted ion species and hence the ion range values, depletion mode devices are classified into two categories. They are: (i) implantation range more than the maximum depletion width at semiconductor surface, (ii) implantation range less than the maximum depletion width due to gate biases. The maximum space charge depletion width depends on the threshold voltage and the bulk resistivity of the semiconductor substrate.

In case of depletion mode transistor, the conducting channel is in the bulk semiconductor rather than at the Si-SiO₂
interface as in the case of enhancement mode transistor. The conducting channel width is modulated by the applied gate bias \[62\]. The total charges in the channel region of this type of transistor are the sum of the charges due to ionized donor impurities and impurities of the implantation species.

In the section 4.2, the method used in fabricating this type of device is given and the obtained results are discussed. Also presented in this section are the detailed study of light emission characteristics due to hot carrier recombination phenomena and the related field distributions. The relevant theory for light emission is given in section 4.3. The difference of observation due to different implantation doses is also discussed. We have measured experimentally and calculated computationally both substrate and gate current as a measure of hot electron effects in depletion mode transistors and presented these results in the section 3.4. The position and magnitude of various current values differ with implantation dose and biasing voltages. Finally section 4.5 contains the conclusions arrived at in this study.

4.2.1 Light Emission from Depletion Mode Transistor

A cross-sectional view of n-channel depletion mode transistor is shown in the Fig. 4.1(a). Various depletion width and current paths are also shown in this figure. The n⁺-p junction is formed under the gate insulator interface. Since we have the p-type substrate, phosphorous implantation is made in the gate area to make n-type channel. All other processing steps
such as field implantation, source drain diffusion, gate oxidation and metallization remain the same as those for the enhancement mode transistor. The implantation is done before metallization which is followed by a high temperature $N_2$ anneal. Actual doping profile and the step profile approximation for the channel are shown in Fig. 4.1(b). Since our device consists of two layers i.e. Si and $SiO_2$, the range of phosphorous atoms in silicon is calculated in the following manner.

i) From the standard table, first the range corresponding to a particular implantation energy is seen for $SiO_2$ layer. Let it be $R_0$.

ii) The thickness of the gate oxide ($d$) is subtracted from $R_0$, say $x_p = (R_0 - d)$.

iii) Now the corresponding energy value for $x_p$ range in $SiO_2$ is seen from standard table.

iv) We determine the range of implantation species in silicon from standard table for the energy calculated in step (iii).

The impurity profile $N(x)$ in ion implanted substrate resembles a Gaussian profile in which the impurity distribution is related to projected range $R_p$ and standard deviation $\Delta R_p$ by

$$N(x) = \frac{0.4 N_s}{\Delta R_p} \exp \left(-\frac{(x-R_p)^2}{\Delta R_p^2}\right)$$

where $N_s$ is dose per unit area of implantation species. $\Delta R_p$ and $\Delta R_p$ have been taken from standard table which is obtained by experimental results.
FIG. 4.1 (b)
4.2.2 Device Fabrication

Depletion mode transistors have been made by phosphorous implantation in Kasper ion-implantation machine keeping the substrate at room temperature. Three different doses at the same energy have been used to fabricate the devices. Table 4.1 contains the detailed specifications followed. The choice for high energy used is to get a junction depth of 500 Å in silicon. High doses of impurities are taken to make the channel $n^+$ with respect to the bulk resistivity of the silicon substrate. During the implantation photoresist is kept over all the regions except the gate area of the device. After implantation the chip is annealed at 900°C for 30 min with $N_2$ flow in the tube. Annealing is done to activate the implanted impurities and remove the damage caused by bombardment of high energy atoms on Si substrate [63]. Annealing is made in such a manner that there is negligible increase of junction depth. All other fabrication procedures are the same as those for the enhancement mode transistor. After final testing the devices are mounted and bonded on TO - 5 header.

<table>
<thead>
<tr>
<th>Type of impurities</th>
<th>Implantation energy</th>
<th>Dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phosphorous</td>
<td>140 keV</td>
<td>$5 \times 10^{12}/\text{cm}^2$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$8 \times 10^{12}/\text{cm}^2$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1 \times 10^{13}/\text{cm}^2$</td>
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</tbody>
</table>
4.2.3 Light Emission Due to Hot Carrier Effects

The current voltage characteristics beyond drain breakdown which varies with gate bias is as in Fig. 4.2(a), (b), for different channel implants: 5 x 10^{12}, 8 x 10^{12} / \text{cm}^2 dose respectively. It is a higher dose device is having a higher drain current for the same \( V_g \) values. This is due to, the channel being more conducting as concentration of n-type impurity is more. But the source-drain breakdown voltage is the same for the three devices. Since the channel conductance in the range of gate bias applied, the devices are in the saturation region. In case the drain bias is beyond the breakdown value, light emission is observed. Optical photographs are taken by the method as described in the chapter III and shown in Fig. 4.2(c). Since exposure the photograph could not be taken fairly well, the lines shown in this figure are drawn by hand to indicate light emission boundaries of the device. As it is seen, light is emitted from three sides of drain region. Light is not emitted from drain-gate boundary. The reason that the junction for phosphorous implantation is 500 Å below the Si-SiO₂ surface. Hence photons from this junction lose their energy while reaching the surface. It is clearly seen in the microscope that light intensity decreases with increase of gate bias at a particular value light is not observed. The measurement was done and its variation with gate bias is shown in Fig. 4.2(c).
(a) I-V characteristics of $5 \times 10^{12}$ dose device beyond source and drain breakdown

(b) I-V characteristics of $8 \times 10^{12}$ dose device beyond source and drain breakdown

(c) Light emission photograph from drain boundaries
Fig. 4.3. It is seen that with increase of the gate bias positively, PMT output decreases. At low negative gate voltages, small peaks exist for various channel doses. As gate breakdown limits the maximum voltage, our measurement is carried out between \(-20\) V and \(+20\) V. The drain voltage in a particular device is varied and the results are plotted as shown in Fig. 4.4. The higher the drain voltage, the larger is the emitted intensity. The decrease of light intensity at higher gate voltages confirms the assumption that as \(V_g\) increases, lateral field at the drain source depletion region decreases and hence carrier multiplication decreases. This results in lowering of the photon generation process. However the peak for the lower \(V_g\) is not a predominant one, because the channel concentration due to implantation has already reached a strong inversion and hence, minority carrier injection in the channel does not appreciably change the channel conductance. From a comparative study of Figs. 4.3 and 4.4, it is concluded that the decrease of implantation dose for depletion transistor makes an effect similar to the increase of the avalanche field for photon generation. This effect becomes predominant in VLSI circuits in which the excess current due to photon absorption influence the carrier flow in the circuit \([64]\).

4.3.1 Theory of Depletion Mode MOSFET Operation and Light Emission

Both theoretical and experimental works on depletion mode transistors were initiated abroad in early 70's \([65,66]\). A computational model of the device in the linear region
Fig. 5.3, (I) $1 \times 10^{13} / \text{cm}^2$, (II) $8 \times 10^{12} / \text{cm}^2$, (III) $6 \times 10^{12} / \text{cm}^2$
Fig. 4.4 Light emission from $5 \times 10^{12}/\text{cm}^2$ dose device
of operation was given in 1979 [67]. In this section we present an improved capacitance model for IGFET operation and the model for qualitative explanation of light emission from the device. To derive an expression for the drain current, we assume that the implantation range of phosphorous atoms is greater than the maximum depletion width \( W_m \) in strong inversion condition and thus the surface region is considered to be a uniformly doped region with concentration \( N_a \). A schematic diagram of depletion mode transistor and relevant current paths are shown in Fig. 4.1(a). The conducting channel between the source and drain is in the bulk of the semiconductor unlike conventional MOSFET in which the channel exists at the Si-SiO\(_2\) interface. The channel conductance is modulated by the gate electrode through the extension of space charge region of the \( n-p \) junction. The doping profile of implanted zones is Gaussian in nature. All the voltages given in this section are taken with reference to the source which is grounded. The drain current is given by the relation

\[ I_D = \mu (\mu q_1 - \mu q_s - \mu q_B) \frac{dV}{dy} \] ...

(4.2)

where \( q_1 \) is the net charge due to implanted impurities and is given by

\[ q_1 = \int_{x_0}^{x_j} (N(x) - N_A) \ dx = (N_D - N_A) x_j \] ...

(4.3)

and \( q_s \) is the surface depleted charge,

\[ q_s = \bar{C} \left[ V_G - \phi_{ms} - V(y) \right] \] ...

(4.4)

\( \bar{C} \) is the average gate capacitance,
\[ \bar{C} = \frac{C_0}{C_0 + \bar{C}_s} \]  
\( ... (4.5) \)

with \( \bar{C}_s = \frac{2.77 \varepsilon_s \varepsilon_0}{d} \) as the capacitance due to substrate. We have also \( Q_B = \sqrt{2 \varepsilon_s \varepsilon_0 q N_A' (V_{bi} + V(y))^{1/2}} \)  
\( ... (4.6) \)

the depleted charge of the channel substrate junction with \( N_A' = N_D N_A / (N_D + N_A) \) and \( V_{bi} \) is the built-in potential of implanted region with the substrate. Assuming the carrier mobility is the same as that in the bulk region, as the conducting channel is away from the surface, we get by substituting Eqs. (4.3), (4.4), (4.6) in (4.2) and integrating from zero to \( L \) (channel length),

\[ I_D = \frac{\mu_B}{L} \int \bar{C}_s \left[ (V_g - \phi_{ms}) V_D - \frac{1}{2} V_D^2 \right] \]
\[ - \frac{2}{3} \sqrt{2 \varepsilon_s q N_A'} \left[ (V_{bi} + V_D)^{3/2} - (V_{bi})^{3/2} \right] \]

\( ... (4.7) \)

From the above equation, it is seen that for small values of \( V_D \), \( I_D \) increases linearly with \( V_D \) but as \( V_D \) increases to higher values, the channel depth \( x_j \) at \( y = L \) becomes zero and this is called the pinch-off point. Now putting the mobile carrier concentration value at \( y = L \) to zero, we get saturation drain current as

\[ I_{D_{Sat}} = \frac{m_z}{L} \mu_B (V_g - V_T) \]
\( ... (4.8) \)

where \( V_T \) is the threshold voltage. \( V_T \) is obtained from Eqn. (4.7) assuming very small \( V_D \), by series expansion and ignoring higher
hence $V_T$ directly depends on donor impurity concentration $N_D$.

For the calculation of the avalanche drain current, we follow the method as is done for the enhancement mode transistor i.e.,

$$I_{Dev} = (N^* - 1) I_{Dsat}$$  \hspace{1cm} \ldots(4.10)$$

$N^*$ is the multiplication factor of the carriers reaching the source drain depletion region and thus depends on the maximum electric field $E_m$ at this region. $E_m$ depends on $V_D$ and $V_g$ by the following relation,

$$E_m = \sqrt{\frac{2}{K} (V_D - (V_g - \Phi_{ms} + Q_1/C) + K_0^2 (1 - \sqrt{1 + 2 \sqrt{\frac{V_g (K_0^2)}}})}$$  \hspace{1cm} \ldots(4.11)$$

where $K_0 = \sqrt{\frac{E_o C_F N_A^0}{U}}$. $N^*$ is calculated from ionisation integral formula at the above field value. We calculate $I_{Dev}$ by using Eqn. (4.10) and it is plotted for three different dose values as shown in Fig. 4.5. Other parameters used in the above calculations are given in the following Table 4.2.
(i) $N_D = 1 \times 10^{13} \text{ cm}^{-2}$
(ii) $= 8 \times 10^{12} \text{ cm}^{-2}$
(iii) $= 5 \times 10^{12} \text{ cm}^{-2}$

FIG. 4-5.
TABLE - 4.2

<table>
<thead>
<tr>
<th>Name of the parameters</th>
<th>Symbol</th>
<th>Computational value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk acceptor concentration</td>
<td>(N_A)</td>
<td>(2.6 \times 10^{15}/\text{cm}^3)</td>
</tr>
<tr>
<td>Metal-semiconductor work function difference</td>
<td>(\Phi_{ms})</td>
<td>1.45 V</td>
</tr>
<tr>
<td>Silicon dielectric constant</td>
<td>(e_s)</td>
<td>11.7 (e_0)</td>
</tr>
<tr>
<td>Electromobility</td>
<td>(\mu_n)</td>
<td>1300 (\text{cm}^2/\text{V-sec})</td>
</tr>
<tr>
<td>Channel implantation dose</td>
<td>(N_D^*)</td>
<td>(5 \times 10^{12}/\text{cm}^2), (6 \times 10^{12}/\text{cm}^2), (1 \times 10^{13}/\text{cm}^2)</td>
</tr>
</tbody>
</table>

As the channel implantation dose increases, for a particular \(V_D\) value, the maximum electric field decreases as given in Eqn. (4.11). Hence the multiplication factor \(M^*\) decreases. Thus for higher implantation dose devices, the avalanche drain current decreases and this results in a decrease of light emission. This variation is in a way similar to the enhancement mode transistor behaviour operating beyond its saturation value.

4.4.1 Study of Hot Carrier Effects by Gate and Substrate

Current Measurements

Similar to the light intensity observations as a measure
of the avalanche multiplication phenomenon, substrate and gate current variation with gate bias can be used to study the same phenomenon. In this section, the gate current in the depletion mode MOSFET normalised to the source current is expressed as a function of the substrate current normalised to the source current by means of an impact ionisation model. Gate bias either enhances or reduces the carrier generation by impact ionisation. This carrier generation mechanism is the origin of the flow of both the gate as well as the substrate current in the device.

4.4.2 Substrate Current

The substrate current $I_{sub}$ of the MOSFET has an influence on its electrical characteristics such as electrical power loss, drain conductance and also hold on time of MOS memory devices. The measurement of $I_{sub}$ reported in this section are carried out at room temperature in a dark room to minimise the optical injection effect. All substrate and source voltages are zero unless otherwise stated. Figure 4.6 shows the typical substrate current $I_{sub}$ vs gate voltage for the n-channel depletion mode transistor. With an increase of gate bias positively, $I_{sub}$ decreases and it is observed that for low values of the gate bias, there exists a peak in the $I_{sub}$. For the same drain voltage value $V_D$, $I_{sub}$ is maximum for the lowest implantation dose device.

Figure 4.7 shows $I_{sub}$ vs $V_G$ characteristics for various drain voltages of $5 \times 10^{12}/\text{cm}^2$ dose depletion device. The
Fig. 4.6 Substrate current vs. gate voltage
variation of $I_{sub}$ with $V_D$ is similar in nature to that in low dose case. With an increase of $V_D$, the peak position of $I_{sub}$ shifts to more positive gate voltage. This result shows that $I_{sub}$ is proportional to $I_{Dsat}$ as given in Fig. 4.5.

It has been reported by other workers that $I_{sub}$ varies linearly with the gate width and inversely with insulator thickness and temperature [68].

### Comparison of Calculated and Experimental Substrate Current Values

The substrate current flows due to the transport of holes through substrate originating from drain depletion region. In the saturation region of the n-channel MOS transistor, electrons flowing from source to the drain are accelerated by the electric field within the pinch-off region and generate electron-hole pairs by impact ionization mechanism. Hence the substrate current is a function of the ionization coefficient, multiplication factor and the pinched off length, so we have:

$$I_{sub} = M \cdot I_D \alpha \Delta L \quad \text{...(4.12)}$$

$I_D$ is taken from Eqn. (4.10) and taking all other parameters as functions of maximum electric field similar to the case of enhancement mode transistor we solve the above Eqn. (4.12). The theoretical values and experimental results are plotted as shown in Fig. 4.8. Both the results agree qualitatively except that the theoretical values are an order of magnitude less than the experimental results. In case of various doses, $V_{Dsat}$ decreases with implantation dose and hence the lateral
4.4.3 Gate Current Due to Hot Carrier Transport Phenomena in Depletion Mode MOSFET

Due to the existence of a high field at the drain substrate depletion region, some electrons are attracted from the channel and can reach the drain giving rise to the drain current, while some others whose energy is more than the Si-SiO₂ barrier height, can reach the gate giving rise to the gate current. In addition to the above electron current, if the drain voltage is very high (compared to the gate voltage) then from the generated electron-hole pairs, some of the holes are attracted by the n-type impurities present in the SiO₂ during implantation and collected by the gate electrode. The n-channel depletion mode transistor therefore may have both hot hole and hot electron currents. In the p-channel devices hot-hole current has not been observed [69]. Among the various types of hot carrier effects, channel hot electron effect (CHE) and substrate hot electron effect (SHE) have been discussed below.

Experimental Results

The gate current is measured by using Keithley 602 model electrometer in dark room. In Fig. 4.9, gate current is plotted for a particular $V_D$ value for devices of various implantation...
Fig. 4-9, Gate current vs Gate voltage
doses. From the polarity of the current through the ammeter, it is seen that for lower values of $V_g$, current is due to flow of holes. For lower $V_g$ values, gate current decreases. The rate of decrease differs for the various doses. At a certain value of $V_g$, the polarity of the gate current for all three different devices changes. Beyond this point gate current increases with $V_g$ values. The measurement of the gate current is also carried out by varying $V_g$ and keeping both the source and drain at the ground potential. This current is due to the substrate hot electrons generated by the gate bias resulting in a transverse electric field. SHE currents for three different devices are plotted as shown in Fig. 4.10. As it is seen, SHE currents equal the CHE current at higher $V_g$ values. It is also seen that SHE current is more for lower dose devices. This is due to limited scattering of electrons with donor impurities in the channel region. Hence, there exists a direct proportionality between substrate hot electron and depletion implant dose of n-type impurity. Another interesting observation is that the position of change of gate current polarity due to CHE current remains the same, whereas the peak height varies with channel dose.

Measurements are also carried out for a particular dose device with various $V_D$ values. Drain voltage values are chosen similar to the values required for light emission. The variation is similar for higher $V_D$ values as in the case of low concentration device. Figure 4.11 shows the gate current vs gate voltage ($I_g$ vs $V_g$) for two $V_D$ values. The lower is the channel...
FIG. 4-10

\[ \log A \]

Gate bias in volts

\[ N_D = 5 \times 10^{12} \]
\[ N_D = 8 \times 10^{12} \]
\[ N_D = 1 \times 10^{13} \]
Electron current

Sample $N_D = 1 \times 10^{13} / \text{cm}^2$
implantation dose, the higher the lateral field leading to avalanche multiplication. Hence $I_g$ will be higher for this case. We have not studied the trapping of electrons in $SiO_2$ causing degradation in depletion mode transistor operation \[70\].

### 4.5 Conclusion

Depletion mode transistors have been fabricated by using various implantation doses. In the range of applied gate bias, the channel carrier concentration does not change appreciably. Since the concentration of implanted atoms is high, the carrier injection does not increase the intensity of light emission. Hence $V_g$ has the only effect of reducing the lateral field which results in less photon emission. The gate current study reveals that holes move from the drain substrate depletion region and can cause gate current to flow. The hole current decreases with an increase of $V_g$ due to reduction in the carrier generation. From the measured values of gate current due to SHE, the channel carrier concentration due to depletion implant can be evaluated using the experimental plots. In depletion mode transistors, one can independently inject either electrons or holes from $Si$ into $SiO_2$ by changing various bias values. This is useful in data storing process of EEPROM chips. Unlike enhancement mode transistor, photons are not seen at the drain-gate boundary as they are observed in silicon since the junction is in the bulk of semiconductor and not at the surface. The study of hot electron trapping in the depletion mode transistor is interesting as the donor impurities present give an additional component to this phenomenon.