ABSTRACT

There are two sources of power consumption in CMOS namely dynamic and leakage. The dynamic power in CMOS is a quadratic function of the supply voltage and the leakage power is its exponential function. Hence, the most effective way to reduce the power consumption is through supply voltage scaling. The extreme case of supply voltage scaling is the subthreshold regime in which it is scaled below the threshold voltage to achieve ULP. The leakage current is used as a driving current in subthreshold circuits and therefore, the speed degrades considerably. The design of ULP digital circuits has received widespread attention due to the rapid growth of ULP applications like body sensor networks and implantable medical electronics etc. Despite the speed degradation, few researchers have tried to improve the speed under subthreshold conditions. This thesis presents innovative techniques to enhance the speed and robustness of subthreshold circuits with a limited power budget to widen their application domain.

There is a significant market for ULP applications which is currently being dominated by ASIC. The cost of ASIC is exponentially rising due to high NRE cost. Hence, it is important to extend the domain of FPGA even under subthreshold conditions so that they can also be employed for reconfigurable ULP applications in place of the expensive and more rigid ASICs in future technologies. This thesis proposes a low power FPGA routing switch box that utilizes the leakage current for body biasing. This technique significantly enhances speed, lowers switching energy, and increases robustness. The device optimized for superthreshold circuits may not provide the optimum subthreshold performance. Hence, FPGA interconnect resources performance has been enhanced using device optimisation techniques under subthreshold conditions.

The interconnect primarily determines the performance of systems at the nanoscale. Hence, the design of interconnect is crucial in improving the performance under subthreshold conditions. Therefore, this thesis also successfully reported that conventional techniques are insignificant in improving the interconnect delay and switching energy. It proposes that device and/or interconnect optimization techniques significantly improve the interconnect performance. It also proposes that near threshold operation of device considerably increases speed and robustness against PVT variations.

It also explores the potential of carbon nanotube based interconnects over copper under subthreshold condition. The performance investigation of CNT and Cu interconnect shows that individual SWCNT interconnects have better performance in deep subthreshold region. However, Cu is found to be more suitable than single SWCNT in moderate subthreshold region for global interconnects. Whereas, SWCNT exhibits better performance for short and intermediate length interconnects. In addition, it also proposes that scaled Cu interconnects perform better than optimized mixed CNT for long interconnects under subthreshold conditions.

It is expected that emerging devices like CNFET and FinFET will replace the existing bulk CMOS technology. Therefore, this work also investigated and optimized the performance of these devices in the presence of PVT variations for different digital blocks under subthreshold conditions. Finally, device parameters like channel length, substrate and halo doping concentrations, and oxide thickness of Si-MOSFET are optimized under subthreshold conditions using TCAD tools for better circuit performance at 45nm technology node.