Chapter 5
Energy Efficient High Performance Interconnects
Chapter 5

ENERGY EFFICIENT HIGH PERFORMANCE INTERCONNECTS

The interconnect primarily determines the performance of systems at scaled technology node due to the increase in chip size and slow scaling of interconnect dimensions compared to the active devices. While the performance of subthreshold circuits is greatly improved in terms of speed and robustness [4, 9, 12, 14, 17, 24], very little progress has been made to improve the performance of interconnects under subthreshold conditions [10, 11]. Hence, interconnects for subthreshold circuits need to be further explored and optimized. Therefore, this chapter mainly focuses on the design of high speed interconnects for energy efficient circuits. The first part introduces different types of CNT interconnects along with their merits and limitations. The second part then compares the performance of Cu and SWCNT interconnects for different biasing voltages in the subthreshold regime. Finally, the performance comparison between Cu and mixed CNT bundle interconnects is carried out under subthreshold conditions.

5.1 Introduction

Scaling of device dimensions down to nanometer range has achieved higher switching speed for nano-electronics circuits and systems. However, interconnect performance in the existing and emerging applications is expected to become the major bottleneck unless radical changes are introduced in the design. The primary requirement for designing interconnects is to meet the high-speed transmission needs of chips despite further scaling of feature sizes [5, 16]. However, with the scaling of technology, while local interconnect capacitance reduces, the global interconnect capacitance increases significantly at nanotechnology node. This is because of increased chip size at every scaled technology node. This increases global interconnect length and hence, results in longer interconnect delay. To solve this problem, several interconnect optimization techniques are proposed to enhance the speed of superthreshold circuits [98-101].
order to overcome problems associated with Cu interconnect, CNT interconnects are currently being explored for future higher speed superthreshold circuits [102, 103].

CNTs are expected to play a significant role in the design and manufacturing of many nano-material devices and interconnect in future high speed VLSI circuits. Though, different CNT interconnects have shown a huge potential to replace the Cu interconnect due to their long mean free paths (MFP), high current carrying capability and high thermal conductivity [104], their suitability for subthreshold circuits has not yet been explored. Also higher current carrying capability and thermal conductivity are not required for subthreshold circuits. Furthermore, due to higher driver resistance, the interconnect resistance is less critical under subthreshold conditions [11]. Therefore, it is important to explore the suitability of CNT as an interconnect under subthreshold conditions. The next section briefly reviews different CNT interconnects along with their design metrics.

5.2 CNT Interconnects

The increasing resistivity of copper with technology scaling and demand for higher current density are motivations to explore new interconnect solutions for deep nanometer VLSI technologies. Metallic CNTs are found to be a promising candidate that can potentially mitigate the challenges faced by Cu, thereby extending the lifetime of electrical interconnects [105-108]. However, the high intrinsic resistance associated with an isolated CNT is \( \sim 6.45 \text{ K}\Omega \) [109]. To deal with this problem, use of a bundle of CNTs as an interconnect is proposed [102, 110]. The resistance of CNTs in a bundle comes in parallel and therefore, CNT bundle interconnects are having high conductance values. Hence, a CNT bundle carries higher magnitude of current and provides lower delay than Cu and individual SWCNT interconnect under superthreshold conditions.

CNTs can be broadly classified as SWCNTs [111, 112] and multi-walled carbon nanotubes (MWCNTs) [95, 113, 114]. SWCNTs consist of a single sheet of graphene rolled into a cylindrical tube with a diameter in the nanometer range as shown in Figure 5.1 (a). Depending on how the graphene is rolled up, it produces either metallic SWCNT or semiconducting SWCNT. MWCNT consists of two or more SWCNTs concentrically wrapped around each other with diameters ranging from a few to several hundred nanometers as shown in Figure 5.1 (b).
MWCNT is having lower resistance as compared to SWCNT interconnects [113]. SWCNT bundle consists of several SWCNTs packed together in parallel whereas a mixed CNT bundle consists of a combination of SWCNTs and MWCNTs packed together in parallel [94] [115]. SWCNTs can be either metallic or semiconducting depending on their chirality (the direction in which they are rolled up); giving rise to zigzag (mostly semiconducting), armchair (metallic) or chiral nanotubes (mostly semiconducting). MWCNTs are always metallic. Suitability of these CNT interconnects need to be investigated under subthreshold conditions.

5.2.1 SWCNT

To investigate the performance of SWCNT under subthreshold conditions, it is necessary to focus on its resistance, capacitance, and inductance for realizing its equivalent SWCNT circuit model. This section briefly explores the different equivalent circuit components of SWCNT interconnects shown in Figure 5.2.

A. Resistance of SWCNT

The resistance of a SWCNT consists of two parts specifically quantum resistance \( R_Q \) and contact resistance \( R_C \). \( R_Q \) is the lowest possible resistance of an isolated SWCNT assuming perfect metal-CNT contact and it is independent of SWCNT
Energy Efficient High Performance Interconnects

length. This is an intrinsic resistance of SWCNT [116]. The contact between the metal and nanotube cannot be perfect, which gives rise to an additional metal-nanotube $R_C$. This additional part of resistance varies from 20 to 120 kΩ [94], which is much larger than the $R_Q$. However, with improved nanotube fabrication techniques, additional $R_C$ has been significantly reduced [117].

The quantum resistance of an individual SWCNT is given by,

$$ R_Q = \frac{h}{4e^2} \approx 6.5 \text{kΩ} \quad (5.1) $$

For longer length, SWCNT resistance depends on its length and applied voltage. For bias voltage less than the critical bias ($< 0.16\text{V}$ for global wires [110]), the SWCNT resistance ($R_{CNT}$) is determined by [118] and is given as:

$$ R_{CNT} = \frac{h}{4e^2} \frac{l_{CNT}}{\lambda} \quad (l_{CNT} \leq \lambda) \quad (5.2) $$

$$ R_{CNT} = \frac{h}{4e^2} \frac{l_{CNT}}{\lambda} \quad (l_{CNT} > \lambda) \quad (5.3) $$

Where ‘$h$’ is the Planck’s constant, ‘$e$’ is the charge of an electron, ‘$l_{CNT}$’ is the length of SWCNT, and ‘$\lambda$’ is the MFP length.

This resistance, caused by scattering, depends on the SWCNT length. Authors in [119] reported the distributed resistance model of an SWCNT and is given below,

$$ R_{CNT} = R_C + R_Q \left(1 + \frac{l_{CNT}}{l_0}\right) \quad (5.4) $$

Where $l_{CNT}$ is the length of SWCNT, $l_0$ is the mean free path, $l_0=1\ \mu\text{m}$ for 1 nm tube diameter [119]. The resistance of a SWCNT bundle is simply a parallel combination of number of metallic SWCNTs present in that bundle [120].

**B. Capacitance of SWCNT**

The total capacitance of an isolated SWCNT is contributed by electrostatic capacitance ($C_E$) and quantum capacitance ($C_Q$) [109]. The effective capacitance of CNT interconnect is given by the series combination of $C_E$ and $C_Q$. $C_E$ of a SWCNT is the capacitance between SWCNT and a ground plane, and is dependent on CNT geometry parameters. The capacitance ‘$C_E$’ is calculated by treating the CNT as a thin wire with diameter ‘$d$’ placed at a distance ‘$y$’ away from a ground plane as shown in Figure 5.2 and is given by,

$$ C_E = \frac{2\pi \varepsilon}{\ln(y/d)} \quad (5.5) $$

where $\varepsilon$ is the permittivity.
CQ arises from the quantum electrostatic energy stored in the nanotube when it carries the current. Due to Pauli’s exclusion principle, it is only possible to add electrons into the nanotube at an available quantum state above the Fermi energy level. The SWCNT quantum capacitance per unit length is given by,

\[ C_Q = \frac{2e^2}{\hbar V_f} \]  

(5.6)

\( C_Q \) of individual SWCNT has a typical value of 100 aF/\( \mu m \). A SWCNT is having four co-propagating quantum channels. Therefore, the effective SWCNT quantum capacitance is given by,

\[ C_Q^{CNT} = 4C_Q \]  

(5.7)

The same effective charge resides on both these capacitances (\( C_E \) and \( 4C_Q \)) when the CNT carries current, as it is true for any two capacitances in series. Hence, these capacitances appear in series in the effective circuit model [121].

Interconnect delay under subthreshold conditions largely depends on the interconnect capacitance rather than its resistance. Hence, to achieve better performance interconnect geometry and process parameters need to be re-designed for minimum capacitance rather than minimum resistance.

**C. Inductance of SWCNT**

Inductance associated with CNT is having two components namely magnetic and kinetic inductance [122]. The magnetic inductance (\( L_m \)) depends on the magnetic field inside and between the tubes whereas the kinetic inductance (\( L_k \)) is extracted by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance [123]. These inductances are given by,

\[ L_m = \frac{\mu}{2\pi} \text{Cosh}^{-1} (2y/d) \]  

(5.8)

\[ L_k = \frac{\hbar}{2e^2 \cdot V_f} \]  

(5.9)

Since a nanotube has four co-propagating quantum channels, the effective value of kinetic inductance in the equivalent circuit is \( L_k /4 \). Due to higher driver resistance and lower operating frequency of subthreshold circuits, the inductance of interconnect has negligible impact on interconnect performance. To investigate the performance of SWCNT interconnect, the commonly used equivalent circuit model of SWCNT is shown in Figure 5.3.
5.2.2 MWCNT

A MWCNT consists of two or more concentric SWCNTs. MWCNT is essentially SWCNTs of varying diameters. Many properties of SWCNT are valid for MWCNT. The number of shells \(N_{sh}\) in a MWCNT is diameter dependent and is given by [110],

\[
N_{sh} = 1 + \frac{(D_{out} - D_{in})}{2\delta}
\]

(5.10)

Where ‘\(D_{out}\)’ and ‘\(D_{in}\)’ are the maximum and minimum shell diameter and ‘\(\delta\)’ is the Van der Waals distance between graphene layers in graphite (which is 0.34 nm). The approximate number of conduction channels \(N_{ch}\) per shell for a MWCNT given by [114] is,

\[
N_{ch} / d_{sh} = (ad + b) \rho_m
\]

\[
d > 6 \text{ nm}
\]

(5.11)

\[
= 2 \rho_m
\]

\[
d < 6 \text{ nm}
\]

(5.12)

Where \(a = 0.1836 \text{ nm}^{-1}\), \(b = 1.275\), ‘\(d_{sh}\)’ is the diameter of shell and ‘\(\rho_m\)’ is the probability of the CNT being metallic.

The resistance for the \(i^{th}\) SWCNT shell with diameter ‘\(d_{sh(i)}\)’ and length \(l\) is given by,

\[
R_{SWCNT(i, l)} = \frac{R_{SWCNT}}{N_{ch/d_{sh(i)}}}
\]

(5.13)

Therefore, the total MWCNT resistance \(R_{MWCNT}\) is a parallel combination of resistance of all the concentric SWCNTs and is given by [124],

\[
(R_{MWCNT}(D_{out}, l))^{-1} = \sum_{N_{sh}} [R_{SWCNT(i, l)}]^{-1}
\]

(5.14)

The potential of different shells cannot be assumed equal as in the case of SWCNT bundles that induces shell-to-shell capacitive coupling. The shell-to-shell capacitance \(C_s\) per unit length is given by the coaxial capacitance formula [125],

\[
C_s = \frac{2\pi\varepsilon}{\ln(D_{out}/D_{in})} = \frac{2\pi\varepsilon}{\ln(D_{out}/D_{in} - 2\delta)}
\]

(5.15)
The quantum capacitance $C_Q$ for MWCNT given by [126],

$$C_Q = 4e^2 N_{ch} L / h V_f$$  \hspace{2cm} (5.16)

Thus, $C_Q$ is in series with electrostatic capacitance including shell-to-shell capacitance $C_S$ and the ground capacitance $C_E$.

### 5.2.3 Mixed CNT Bundle

Higher resistance associated with individual CNT motivated researchers to use a bundle of CNTs to provide interconnects with higher conductance for superthreshold circuits [90, 94]. Theoretically, CNT bundles may contain only SWCNTs or only MWCNTs. However, almost all experimental results have demonstrated that a realistic nanotube bundle contains both SWCNTs and MWCNTs as shown in Figure 5.4, hence, called mixed CNT bundle [94]. Mixed CNT bundles have been largely investigated and optimized for interconnect applications under superthreshold regime. Depending on the process controls and conditions during CNT synthesis, CNT diameters inside a bundle follow normal distribution [94].

All the earlier models and current fabrication processes indicate that roughly $1/3^{rd}$ of the total CNTs in the bundle would be metallic, while the rest are semiconducting. Therefore, for superthreshold interconnects, these tubes must be densely packed and a large number of conducting tubes should be accommodated within a bundle for best performance. However, increasing the number of tubes inside a mixed CNT bundle, also increases bundle capacitance significantly. Therefore, under subthreshold conditions, there is a need to explore optimum values of number of tubes per bundle to increase the interconnect speed by reducing the capacitance with moderate increase in resistance.

A mixed bundle consists of SWCNTs with a diameter ‘$d$’ and MWCNTs with various diameters ($D_{in} < d_i < D_{out}$). It has been shown that a mixed CNT bundle is more realistic due to lack of chirality control techniques for CNTs. It has also been shown that the outer diameters follow a normal (Gaussian) distribution [94]. The total resistance for a mixed CNT bundle is given by [124],

$$R_{Mixed} = \left( \int \frac{N(D_{out}) \delta D_{out}}{R_{MWCNT}(D_{out})} \right)^{-1}$$  \hspace{2cm} (5.17)

Where, the tube count $N(D_{out})$ is obtained according to $D_{out}$ with a normal (Gaussian) distribution with mean diameter ‘$\overline{D_{out}}$’ and a standard deviation ‘$\sigma D_{out}$’.
For the number of CNTs in the bundle \( N_{\text{bundle}} \), the tube count \( N(D_{\text{out}}) \) for the given \( D_{\text{out}} \) estimated by [94],

\[
N(D_{\text{out}}) = \frac{N_{\text{bundle}}}{\sigma D_{\text{out}} \sqrt{2\pi}} \exp\left(-\frac{1}{2\sigma^2} \left(\frac{D_{\text{out}} - D_{\text{out}}}{\sigma D_{\text{out}}}\right)^2\right)
\]  

(5.18)

The capacitive characteristics of a mixed CNT bundle can be determined by the cross-sectional dimension of the bundle. Therefore, similar to the case of a SWCNT bundle, it can be assumed that a mixed bundle also has electrostatic capacitance to ground, coupling, and quantum capacitances. Finally, the total kinetic inductance of a mixed bundle is the parallel inductance value of all the conduction channels in the bundle.

Different geometric and process parameters such as (bundle width (W), bundle height (H), bundle length (l), and (average diameter of tube, tube density (D), the ratio \([D_{\text{in}} / D_{\text{out}} = (dR)]\), \( \rho \)m respectively in a bundle are having significant impact on the conductance, inductance, and capacitance of a CNT bundle which largely determines the interconnect delay and power consumption.

The major research challenge in the subthreshold operating region is to take the ULP benefits obtained by aggressive voltage scaling with minimal degradation in speed so that the application domain of subthreshold circuits can be extended significantly. Hence, the next section investigates the suitability of CNT interconnects for future subthreshold circuits and also designing high performance energy efficient interconnects for ULP subthreshold circuits.
5.3 Related Work

Significant research work has been carried out on the performance improvement of subthreshold circuits in terms of speed and robustness [9, 12] by either device and/or circuit level optimizations. However, very little progress has been made to investigate and improve the performance of interconnects under subthreshold conditions [7, 10, 11]. Authors [7] investigated the challenging design issues related with the subthreshold FPGA and observed that interconnect is its major performance bottleneck. They successfully reported that interconnect resources of subthreshold FPGA consume 70% of its total energy with delay contribution of 84%. This breakdown clearly indicates that more focus on interconnect is necessary to design energy efficient subthreshold circuits. Authors [10] proposed gate voltage boosting techniques to improve the interconnect speed and robustness by 84-88% and 66-74% respectively by shifting device operating point in superthreshold operating region from subthreshold regime. However, this work does not cover interconnect level analysis and optimizations.

In addition, Omar Jamal and Azad Naeemi proposed individual SWCNT as interconnect for subthreshold region [11]. Authors [11] proposed a SWCNT as interconnect instead of Cu under subthreshold conditions and reported maximum 5.5 times speed and 30 times EDP improvement over Cu. However, authors investigated the interconnect performance under deep subthreshold condition ($V_{DD}$=100 mV) at deep nanometer technology nodes (22/16/14 nm) by considering the low biased resistance model of individual SWCNT for only short and intermediate length interconnects. Arijit Raychowdhury and Kaushik Roy reported 160 mV as the critical low bias voltage for the validity of the low bias resistance model of CNT. Also, as the biasing voltage increases, conductance drops significantly due to optic and zone-boundary phonon scattering [127] thereby, degrading the interconnect speed. Furthermore, Armin Tajalli and Yusuf Leblebici experimentally and analytically investigated that scaling of $V_{DD}$ in deep subthreshold region increases energy consumption [17]. Authors also proposed that optimum $V_{DD}$ for minimum energy consumption lies in the moderate subthreshold region [17]. In addition, moving to deep nanometer technology node does not seem to be the best choice for reducing energy consumption especially below 45/32 nm nodes due to process variations [17]. Moreover, digital circuits operated in deep subthreshold region will have significant
delay and noise margin penalty along with robustness issues that cannot be ignored for portable devices used in real time applications [17, 52]. Hence, designing of robust and moderate performance subthreshold FPGAs is challenging at low bias voltage used in [11]. Repeater insertion technique commonly used in superthreshold domain may not provide any performance improvement in case of long interconnect under subthreshold conditions due to large driver delay. Clearly, the design of reliable, low power, and fast interconnect poses a challenging area of research for moderate performance subthreshold logic. Also, global interconnect drivers used for on-chip buses and clock distribution networks significantly suffer from performance degradation in the presence of PVT variations.

Therefore, to deal with speed and robustness degradation issues, it is necessary to operate subthreshold circuits in moderate subthreshold region instead of deep subthreshold region ($V_{DD}=100$ mV) so that ULP FPGA can meet the performance target of real time applications as well. Hence, for moderate subthreshold region, realistic SWCNT interconnect resistance model needs to be considered rather than the low bias resistance model used in [11].

In addition, mixed CNT bundle interconnect is suggested as possible replacement for long Cu interconnect under superthreshold conditions. However, the performance of mixed CNT bundle interconnects have not been explored for subthreshold interconnect applications. Therefore, this chapter also investigates the performance of different types of interconnects for varying interconnect lengths under both deep and moderate subthreshold conditions.

### 5.4 Performance Analysis of CNT Interconnects

It has been well established that individual SWCNT is not suitable for superthreshold interconnect applications due to its higher resistance. However, under subthreshold conditions, the interconnect resistance is less critical due to higher driver resistance. Besides this, the capacitance of SWCNT is lower as compared to conventional Cu. Therefore, it is important to explore the interconnect length at which the SWCNT resistance becomes critical design parameter rather than its capacitance under subthreshold conditions. Therefore, this section explores the performance and limitations of SWCNT interconnect under different subthreshold conditions along with its comparison with the conventional Cu interconnects [128].
The delay for RC Cu interconnect driven by a CMOS driver is given by [129],

\[
\Gamma_d = R_{\text{drive}} (C_{\text{drive}} + C_{\text{load}}) + 0.4 R_w C_w l^2 \\
+ (R_{\text{drive}} C_w + R_w C_{\text{load}})
\]  

(5.19)

Where \( R_{\text{drive}} \) and \( C_{\text{drive}} \) are the driver resistance and capacitance respectively, \( R_w \) and \( C_w \) are the interconnects resistance and capacitance, ‘\( l \)’ is the length of the wire and \( C_{\text{load}} \) is the load capacitance. \( R_{\text{drive}} \) increases exponentially as \( V_{DD} \) scales below \( V_{th} \) and it is very large compared to \( R_w \). However, \( C_{\text{drive}} \) is very small as compared to global \( C_w \). From equation (5.19), it is clear that subthreshold interconnect delay largely depends on \( R_{\text{drive}} \) and \( C_w \).

Energy-delay tradeoff as shown in Figure 2.12 and increased impact of PVT variations on device performance restrict further \( V_{DD} \) scaling towards deep subthreshold region for moderate throughput ULP applications [130]. To achieve minimum EDP and to reduce variability, it is necessary to operate subthreshold circuits in moderate subthreshold region instead of deep subthreshold region [17]. Authors [11] reported that individual SWCNT is suitable for interconnects under deep subthreshold conditions. However, as interconnect design for subthreshold circuits is at an early stage, this section investigates the performance of different types of interconnects at different operating points.

SWCNT interconnect resistance and electrostatic capacitance are calculated by using equations (5.4) to (5.6). For 1 nm diameter SWCNT, contact resistance is assumed to be 20 k\( \Omega \) [111]. The quantum capacitance of 400 aF/\( \mu m \) is added in the calculation of total capacitance of SWCNT. The equivalent circuit model, shown in Figure 5.5, is used to investigate the performance parameters of SWCNT interconnect under subthreshold conditions. Interconnect drivers are assumed to be an inverter with n-FET having \( W/L = 5 \) and p-FET 2.5 times that of n-FET at 32 nm technology node using the 32 nm High performance (HP) PTM parameters. The driver sizes considered for intermediate and long interconnect lengths are 5 times and 10 times the minimum driver size respectively. The equivalent resistance and capacitance of mixed CNT bundle interconnect is extracted using CNIA [96] [94] with interconnect geometry parameters as suggested by ITRS [16]. The inductance of interconnect is assumed to be negligible due to higher subthreshold driver resistance and relatively lower operating frequency of subthreshold circuits. This section investigates the performance benefits of SWCNT with realistic resistance over Cu.
High bias resistance model is considered because as explained in section 5.3, it is difficult to design robust subthreshold circuits for $V_{DD} < 160$ mV at deep submicron technology nodes [17]. Figure 5.6 shows the performance comparison of individual SWCNT and Cu interconnects up to 500 μm length [95]. Moderate and deep subthreshold regions are assumed at $V_{DD}=0.4$V and 0.2V respectively. The total propagation delay including the driver delay and the interconnect delay is measured between point 1 and 2 as shown in Figure 5.5.

Low Power (LP) and HP 32 nm PTM technology models are compared for driver transistors under subthreshold conditions for 500 μm interconnect length at 0.4V $V_{DD}$. It is observed that HP model provides 18.69 times and 6.89 times delay improvement over LP model for Cu and individual SWCNT interconnect respectively. However, the power dissipation for HP model is higher than that for LP model. Hence, further investigation of PDP design metric for exploring the suitability of HP and LP models shows that HP model provides 9.8 times and 4.5 times improvement in PDP for Cu and SWCNT interconnect respectively over LP model. Therefore, HP model is used instead of LP model for interconnects design.

The test setup, shown in Figure 5.5, is simulated for different interconnect lengths under subthreshold conditions. It has been observed from Figure 5.6 that for short and intermediate interconnect length, individual SWCNT shows 3 times speed enhancement over Cu interconnect at 500 μm interconnect length in deep subthreshold region. As interconnect length increases upto 400 μm, performance
Energy Efficient High Performance Interconnects

benefits offered by individual SWCNT interconnect over Cu, increases due to lower SWCNT capacitance and very high deep subthreshold driver resistance at $V_{DD}=0.2\text{V}$. However, as shown in Figure 5.7 and 5.8 at 500 $\mu$m interconnect length, speed and EDP improvement over Cu reduces due to significant increase in SWCNT resistance.

Performance benefits offered by individual SWCNT interconnect decreases as operating point is shifted from deep subthreshold to moderate subthreshold operating region. Individual SWCNT interconnect shows maximum 1.82 times speed enhancement over Cu in the moderate subthreshold region. As interconnect length increases beyond 500 $\mu$m, speed enhancement over Cu starts decreasing due to increase in individual SWCNT interconnect resistance. As shown in Figure 5.7, individual SWCNT in deep subthreshold region shows better performance benefit than that of the moderate subthreshold region. This is because in the moderate subthreshold region for 200 $\mu$m SWCNT interconnect length, interconnect delay starts dominating the driver delay due to higher SWCNT resistance, and relatively lower driver resistance over deep subthreshold region. Figure 5.8 shows that individual SWCNT interconnect can offer upto 28 times EDP improvement over Cu interconnects in deep subthreshold region. However, in moderate subthreshold region, maximum EDP improvement offered by SWCNT is upto 5.8 times over Cu for 80 $\mu$m interconnect length. Further increase in the interconnect length up to 500 $\mu$m reduces the EDP improvement by 2.5 times over Cu interconnect.

![Figure 5.6: Delay comparison of Cu and SWCNT interconnects at moderate subthreshold and deep subthreshold region (inset figure) at aspect ratio (AR) = 2.](image-url)
This section investigates and compares the performance comparison of Cu, individual SWCNT, and mixed CNT bundle for global interconnect applications. Theoretically, CNT bundles may have only SWCNTs or only MWCNTs. However, due to fabrication constraints, a CNT bundle consists of both SWCNTs and MWCNTs. Authors in [94] shows that realistic CNT interconnect will be a mixed
bundle of SWCNTs and MWCNTs. Figure 5.9 shows the speed improvement offered by Cu and mixed CNT bundle interconnects at AR = 3 over the individual SWCNT global interconnect. It shows that Cu and mixed CNT bundle interconnect provides almost 2.75 times speed improvement over individual SWCNT at 1000 μm interconnect length in moderate subthreshold region. This performance trend of long interconnect over that of short and intermediate interconnects is due to higher resistance of long individual SWCNT. However, as seen in inset figure, for deep subthreshold region, individual SWCNT shows upto 2.87 times and 3.3 times speed improvement over mixed CNT bundle and Cu interconnects respectively. From the above analysis, it is observed that for global interconnects, individual SWCNT is only beneficial when subthreshold circuits are operated in deep subthreshold operating region.

Furthermore, Figure 5.10 shows the effect of $V_{DD}$ scaling on speed and EDP performance enhancement for Cu and mixed CNT bundle interconnects over individual SWCNT interconnect. From Figure 5.10, it is observed that Cu and mixed CNT bundle interconnects perform better than individual SWCNT interconnect for $V_{DD} > 300$ mV for 1000 μm interconnect length. The driver output resistance becomes less than SWCNT interconnect resistance for $V_{DD}$ higher than 300 mV, thereby degrading the performance of individual SWCNT interconnects. For $V_{DD} < 350$ mV, SWCNT performs better than Cu and mixed CNT bundle at 500 μm interconnect length. Inset Figure 5.10 shows that above 350 mV $V_{DD}$, Cu and mixed CNT bundle show significant EDP improvement over individual SWCNT interconnect.

Figure 5.9 and Figure 5.10 show that for long interconnect length individual SWCNT provides better performance than Cu and mixed CNT bundle only when operated in deep subthreshold region. Cu and mixed CNT bundles are much better in moderate subthreshold region. Figure 5.9 and Figure 5.10 show that mixed CNT bundle provides a little better performance than Cu due to 14% lower capacitance than Cu at AR = 3. Mixed CNT process parameters used in this simulation are obtained from [94]. These parameters are designed for maximum conductance.

However, as interconnect capacitance is more important rather than its resistance, there is a need to optimize the mixed CNT bundle to investigate its performance for optimum subthreshold applications. The next section explores the optimization and comparison of mixed CNT bundle for long interconnect length.
Figure 5.9: Delay improvement offered by Cu and mixed CNT bundle over SWCNT interconnect at moderate subthreshold region and SWCNT over Cu and mixed CNT bundle in deep subthreshold region (inset figure) at AR = 3.

Figure 5.10: Effect of $V_{dd}$ scaling on interconnect delay and EDP (inset figure) improvement offered by Cu and mixed CNT bundle interconnect over SWCNT interconnects at AR = 3.
5.5 Mixed CNT Bundle for ULP Global Interconnects

Interconnect width and thickness are normally optimized to obtain the best possible RLC parameters of interconnect. Delay and electromigration problems of global interconnect due to increased resistance by technology scaling are mitigated by using wider wires than minimum–size provided by ITRS in superthreshold region. AR scaling in superthreshold region is further limited by increased electromigration problem. Increasing width of interconnect proportionally reduces $R_W$, however it is having negative impact on $C_W$. Hence, interconnect geometry parameters optimized for superthreshold region may not provide optimum performance in subthreshold region. Interconnect speed under subthreshold conditions is mainly dominated by the interconnect capacitance. Capacitance reduction with AR scaling and insignificant electromigration problem under subthreshold conditions permit the use of interconnects with lower width and thickness than provided by ITRS. Hence, dimensional control will be a key parameter for improving the performance of subthreshold interconnects.

5.5.1 Optimization of Mixed CNT Bundle Process Parameters

Interconnect geometry structure, shown in Figure 5.11 [111] and mixed CNT process parameters given in [94], are used to extract the RLC parameters from specific tool called CNIA [74]. The interconnect width is denoted by ‘W’, the dielectric thickness by (‘T’) and height ‘H’ = (AR·W), where the AR suggested by ITRS for global interconnect is taken as ‘3’ [16]. The interconnect geometry structure, shown in Figure 5.11, gives an opportunity for re-optimizing the values of width, thickness, and height especially for subthreshold applications. The spacing between two interconnect (‘S’) is assumed to be equal to the width of the interconnect [117].

It is important to explore the appropriate mixed CNT bundle process parameters to get better delay performance [131]. Mixed CNT bundle process parameters in [94] are optimized for maximum conductance to increase the speed of super threshold circuits. However, instead of resistance, capacitance is the most vital design parameter for subthreshold interconnects. In the previous work, the capacitance of mixed CNT bundle at $p_m= 1$ is assumed to be equal to that of Cu interconnect. However as $p_m$ decreases, the bundle capacitance reduces [117]. Hence, it is necessary to optimize the process parameters for minimum capacitance.
At first, the effect of different tube density and average tube diameter on subthreshold interconnect delay and EDP are explored. Figure 5.12 shows resistance as a function of tube density and average tube diameter for 1000 μm long mixed CNT bundle interconnect. The tube density is varied from 1E+12 to 5E+12 tubes/cm² and the average tube diameter is varied from 2 to 5 nm. ρm is assumed to be 33% and \( \frac{D_{outer}}{D_{inner}} = 0.5 \) is considered for the simulation purpose [94]. Figure 5.12 shows that minimum tube density (1E+12 tubes /cm²) and minimum avg. diameter (2 nm) corresponds to maximum resistance. Figure 5.13 shows that the minimum tube diameter gives minimum bundle capacitance and it almost remains constant upon varying the tube density from 1E+12 to 5E+12 tubes/cm².

Figure 5.14 and Figure 5.15 show the effects of avg. tube diameter and tube density on the delay and EDP of the interconnect under moderate subthreshold conditions (\( V_{DD} = 0.4V \)).

Figure 5.11: Schematic diagram of interconnect geometry under consideration for performance comparison.

Figure 5.12: Resistance as a function of tube density and diameter.
For long interconnect analysis, 10 times minimum driver size is assumed. As shown in Figure 5.14 and Figure 5.15, mixed CNT interconnect bundle shows minimum delay and EDP in moderate subthreshold region for avg. diameter = 2 nm and 5E+12 tube density due to lower resistance and capacitance. It is observed from Figure 5.14 that the delay increases by 4.43% as the tube density varies from 5E+12 to 1E+12 tubes/cm². Also by reducing the tube diameter from 5 to 2 nm improves the speed by 3.56%. EDP, obtained by diameter and tube density optimization for subthreshold region, is 6.7% better than EDP with superthreshold process parameters optimized in [94].
Figure 5.15: EDP as a function of tube density and diameter in moderate subthreshold region.

Figure 5.16: Delay and EDP as function of tube density and diameter at $V_{DD}=0.2V$.

Figure 5.16 shows EDP and delay response of mixed CNT bundle under deep subthreshold conditions ($V_{DD}=0.2V$). Increase in the tube diameter, increases the delay by 1.7% and it remains constant with the rise in tube density. This shows that smaller number of tubes per bundle is sufficient under deep subthreshold operating conditions due to increased driver resistance with $V_{DD}$ scaling. As metallic CNT density decreases, the bundle capacitance reduces. Further, decrease in metallic CNT density from 33% to 10% and increasing $D_{outer}/D_{inner}$ to 0.8 gives 6.13% improvement in delay under deep subthreshold region. However, for moderate subthreshold region, insignificant improvement in delay and EDP is observed due to large increase in bundle resistance. The bundle resistance increases by reducing the metallic tube
density due to the decrease in number of metallic CNTs in a bundle. Hence, by optimizing the process parameters of mixed CNT bundle under subthreshold conditions, the bundle capacitance reduces by 10% with significant increase in its resistance.

5.5.2 Effect of Aspect Ratio Scaling on Interconnect Performance

Interconnect geometrical parameters given by ITRS are typically optimized for superthreshold applications by considering the conductance and electromigration as major design issues. However, the resistance of interconnect is a less significant design metric for subthreshold interconnects due to the higher value of the driver resistance under subthreshold conditions. Hence, any decrease in interconnect capacitance with a moderate increase in interconnect resistance will improve the performance of subthreshold circuits. This can be achieved by using interconnects with smaller AR. For super-threshold operating region, higher AR is preferred to avoid electromigration. As electromigration problem is negligible in subthreshold region, AR scaling gives an opportunity to improve the performance of subthreshold interconnect in terms of delay and EDP. Hence, it is necessary to investigate the effect of interconnect height scaling on interconnect capacitance so that suitable AR can be chosen under subthreshold conditions. This section mainly contributes towards exploring the effect of AR scaling on the capacitance and hence, the delay of Cu and mixed CNT bundle.

Figure 5.17 shows the effect of AR scaling on the capacitance of mixed CNT bundle optimized in [94] for superthreshold region, mixed CNT bundle optimized in the above section for subthreshold circuits and for Cu interconnect. As shown in Figure 5.17, the opt. mixed CNT bundle shows significant reduction in capacitance over mixed CNT bundle optimized in [94] and Cu at AR=3. Hence, for ITRS defined AR, mixed CNT bundle performs better than Cu at value of $\rho_m$. However for AR=1, the capacitance of Cu interconnect is lower than even that of the optimized mixed CNT bundle for subthreshold circuits. It is important to investigate the performance of opt. mixed CNT bundle and Cu interconnects over a wide range of global interconnect lengths. Figure 5.18 shows that Cu performs better than mixed CNT bundle interconnect at AR=1 under subthreshold conditions.
5.5.3 Effect of Crosstalk on Interconnect Performance

As integration density of on chip interconnect increases at every technology node, the crosstalk effect becomes more pronounced [132]. In order to keep crosstalk minimum, the capacitance between two wires should not be too large [27]. This is feasible by breaking a long interconnect by inserting intermediate buffers. However, under subthreshold conditions, inserting repeaters increases the delay and switching energy and hence, this technique is not suitable for subthreshold circuits. Another approach of reducing the crosstalk is to use shielding wires [27, 133], which also increases the
capacitive load and therefore, the delay [27]. To study the effect of crosstalk on the victim line, test setup, shown in Figure 5.19, is simulated for different AR [134] and different signal directions on aggressor 1, aggressor 2, the victim line and the corresponding results are listed in Table 5.1. The driver size considered for the simulation purpose is 10 times the minimum driver size to drive 5 mm interconnect length.

To study the effect of crosstalk on transition-less victim line, a victim line is kept at low logic level whereas, a low to high transition is applied on both the aggressor lines. It is important to investigate and compare the effect of adjacent signal transitions on delay and PDP of Cu and mixed CNT victim lines due to crosstalk. The corresponding crosstalk induced noise for different AR is explored in Figure 5.20 and Figure 5.21 for Cu and mixed CNT bundle respectively. The delay variation due to crosstalk introduced by adjacent signal transition is improved by 31.58% for Cu and 20% for mixed CNT interconnects at AR= 1 over AR=3. This is due to the decrease in capacitance by AR scaling. From these Figures, it is found that mixed CNT bundle interconnects do not provide significant improvement in crosstalk over Cu. It is observed from Table 5.1 that if subthreshold interconnect lines are running parallel to the wires with high frequency signal, then the crosstalk effect reduces over the same frequency signal transition in opposite direction. From Table 5.1, it is clear that the crosstalk has a large impact on the delay and PDP performance of subthreshold global interconnect. Hence, there is a need to reduce the crosstalk so that subthreshold circuits perform well even for complex parallel interconnect architecture like in FPGA. Therefore, it can be concluded from the above analysis that mixed CNT bundle is not suitable for global interconnect as compared to Cu under subthreshold conditions.

![Figure 5.19: Schematic of equivalent circuit to model crosstalk between adjacent wires.](image-url)
Figure 5.20: Snapshot of signal transition due to aggressor transitions for Cu interconnect.

Figure 5.21: Snapshot of signal transition due to aggressor transitions for mixed CNT interconnect.

Table 5.1: Effect of signal transition on the performance of global interconnect at AR=1.

<table>
<thead>
<tr>
<th>Aggressors Transitions</th>
<th>Victim Transition</th>
<th>Mixed CNT bundle</th>
<th>Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Delay (ns) PDP (fJ)</td>
<td>Delay (ns) PDP (fJ)</td>
</tr>
<tr>
<td>Without Aggressor</td>
<td>Low to high</td>
<td>78.09 8.23</td>
<td>67.23 6.43</td>
</tr>
<tr>
<td>Low to high</td>
<td>High to low</td>
<td>147.51 34.7</td>
<td>125 23.36</td>
</tr>
<tr>
<td>Opposite direction</td>
<td>Low to high</td>
<td>108.09 16.68</td>
<td>85.96 11.7</td>
</tr>
<tr>
<td>Aggressor@ 0.9V Low to high</td>
<td>High to low</td>
<td>140 38.02</td>
<td>123 23.51</td>
</tr>
<tr>
<td>High to low @High Frequency</td>
<td>Low to high</td>
<td>114.47 19.4</td>
<td>100.9 17.4</td>
</tr>
<tr>
<td>Low to high @High Frequency</td>
<td>Low to high</td>
<td>98.41 13.7</td>
<td>85.43 11.5</td>
</tr>
<tr>
<td>Low to high Held at high</td>
<td>Held at high</td>
<td></td>
<td>Results in crosstalk induced noise on victim line as shown in Figure 5.20 and Figure 5.21</td>
</tr>
<tr>
<td>High to low Held at low</td>
<td>Held at low</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.6 Summary

This chapter has successfully carried out comprehensive performance investigation of SWCNT, mixed CNT bundle, and Cu interconnects under different subthreshold conditions. It has been proposed that individual SWCNT interconnect provides better performance under deep subthreshold conditions for all interconnect lengths. While Cu interconnect is found to be more suitable for global interconnect length under moderate subthreshold conditions. It also explored the effective reduction of crosstalk and delay for global interconnect by using AR scaling. Interconnect geometry parameters suggested by ITRS for superthreshold circuits are not suitable for optimum performance of subthreshold circuits. Re-designing interconnect geometry parameters resulted in improvement in delay, switching energy, and crosstalk for Cu and mixed CNT bundle. This chapter also demonstrated that mixed CNT bundle interconnects are not suitable in subthreshold operating region. It has also been found that Cu interconnects with AR=1 is more suitable for global interconnects due to lower interconnect capacitance as compared to a CNT bundle under subthreshold conditions.

As Cu interconnect is more suitable for long interconnects, the next chapter explores design challenges and proposes device and interconnect optimization techniques to improve the performance of ULP global Cu interconnect.