Chapter 1

Introduction
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There are two sources of power consumption in CMOS namely dynamic and leakage. The dynamic power consumption in CMOS is a quadratic function of the supply voltage ($V_{DD}$) and the leakage power is its exponential function. Hence, the most effective way to reduce the power consumption is through $V_{DD}$ scaling. The extreme case of $V_{DD}$ scaling is the subthreshold regime in which it is scaled below the threshold voltage ($V_{th}$) to achieve ultra low power (ULP) consumption. The leakage current is used as a driving current in subthreshold circuits and therefore, they are used only for low throughput applications. Moreover, in subthreshold region, exponential I-V characteristics makes device more sensitive to process, voltage, and temperature variations. Hence, to extend the application domain of subthreshold region, there is a need to address the speed and robustness issues. This thesis explores different techniques to improve the performance and robustness of subthreshold circuits and interconnects so that they can also be employed for moderate throughput applications. It also investigates techniques to enhance the performance and robustness of subthreshold FPGA so that it can replace the expensive and rigid ASICs for reconfigurable ULP applications.

1.1 Motivation

CMOS technology scaling helps in achieving the desired speed but at the cost of increased power dissipation [1-3]. However, there is a special class of emerging ULP applications like body sensor networks, RFIDs, pacemaker, etc. that do not require high speed. The primary motivation for these applications is ULP consumption so as to prolong the battery life or to employ energy harvesting effectively [4-5]. To satisfy the ULP demand of these applications, it is necessary to operate the circuit under subthreshold condition [4].

The application areas of FPGA are expanding rapidly due to significant improvement in its speed, area, and low non-recurring engineering (NRE) cost [6]. Field programmability and flexibility features of FPGAs are attractive even for ULP applications [7]. However, compared to ASICs, an FPGA consumes significant
amount of power. Existing approaches fails to provide both flexibility and desired energy efficiency. Subthreshold operation of FPGA will reduce the power dissipation significantly at the cost of huge delay penalty. Hence, it is important to enhance the speed of subthreshold FPGA so that it can compete with ASICs employed in ULP systems.

Interconnect primarily determines the performance at the nanoscale [3, 5]. Hence, the design of interconnect is crucial in enhancing the performance of VLSI circuits. Optimum subthreshold circuit performance is achieved by device and/ or circuit optimisation techniques [8-9]. However, very little progress has been made to improve the speed of interconnects under subthreshold conditions [7, 10-11]. Therefore, it is necessary to explore different materials (Cu, CNT, etc.) for interconnects and carry out parameter optimisation to achieve best performance under subthreshold condition.

The exponential relationship between current and voltage in subthreshold regime makes subthreshold circuits more prone to PVT variations [12]. Recent studies have demonstrated that the reduction in $V_{DD}$ increases the device susceptibility to process variations, resulting in spreading of circuit design metrics from their nominal values and reduced noise margin [8-9]. Therefore, while designing subthreshold circuits, it is essential to consider the robustness issue.

It is expected that emerging devices like Carbon Nanotube Field Effect Transistors (CNFET) and FinFET will replace the existing bulk Si-MOSFET technology in the future [13-16]. Hence, it is necessary to investigate and optimize the performance of subthreshold circuits using FinFET and CNFET under subthreshold conditions.

The device designed for superthreshold operation is not optimum under subthreshold condition [17-18]. Hence, it is necessary to design new device parameters to improve the drive current to enhance the speed of subthreshold circuits. While exploring high speed and robust subthreshold circuit design, various contributions made in this thesis are discussed in the next section.

1.2 Contributions

This thesis explores some novel techniques to enhance the speed and robustness of subthreshold circuits by keeping power dissipation within limit for ULP applications.
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The following are the key contributions made in this thesis while designing robust subthreshold circuits for ULP applications.

- The interconnect architecture of FPGA largely determines the total delay and power dissipation. The speed of FPGA interconnect is largely governed by the switch boxes used in its architecture to route signal vertically and/or horizontally. While dealing with this challenge, this thesis proposes robust and high-performance switch box in which leakage voltage is utilized for body biasing. The proposed novel self-body bias routing switch box has much better performance in terms of delay and PDP than the existing switch boxes for future subthreshold FPGA.

- It also demonstrates that repeater insertion in FPGA long interconnect lines and the use of mixed CNT bundle as interconnects instead of Cu do not provide any significant advantage in delay or energy contrary to superthreshold region.

- Furthermore, this thesis proposes a new design style for FPGA interconnect fabric in which the interconnect driver and buffer operating point is shifted towards near threshold region after optimizing the device parameters especially for subthreshold region. The results clearly demonstrate that the proposed method of designing subthreshold FPGA interconnect resource offers significant improvement in speed, switching energy, and robustness against PVT variations.

- It also proposes that the optimum performance of interconnect is obtained by selecting proper interconnect material (Cu or CNT) and $V_{DD}$ under different subthreshold conditions.

- The performance comparison between Cu, individual SWCNT, and mixed CNT bundle for Long interconnect shows that Cu performs best at reduced aspect ratio in moderate subthreshold region for global interconnect. It also demonstrates that individual SWCNT interconnect provides better performance under deep subthreshold conditions for different interconnect length.

- This thesis proposes that interconnect geometry parameters suggested by ITRS for superthreshold circuits are not suitable for optimum performance under subthreshold conditions. Aspect ratio scaling, which is not possible in
superthreshold domain due to electromigration problem, is feasible in subthreshold region due to lower current density. This thesis also explores crosstalk and delay reduction techniques in global interconnects by reducing the aspect ratio. It also shows that mixed CNT bundle interconnects are not suitable for subthreshold circuits.

- In addition, this thesis also highlighted the differences in the optimization and design of interconnects for subthreshold and superthreshold conditions. It also demonstrates that the driver delay rather than the interconnect delay dominates under subthreshold conditions. Further, this thesis has proposed that intermediate repeater insertion technique is not suitable for subthreshold regime contrary to superthreshold regime.

- This thesis has successfully demonstrated different techniques for interconnect driver optimization to improve the interconnect speed and switching energy. It also effectively investigates the effect of process and temperature variations on interconnect performance.

- Furthermore, this thesis successfully explores the performance and robustness comparisons of most emerging nano devices like CNFET and FinFET. The performance of CNFET circuits is greatly improved by optimizing the number of tubes and the pitch for minimum subthreshold slope and gate capacitance. It has investigated that CNFET drive current and performance parameters are less sensitive to process and temperature variations than FinFET. The performance optimization and comparison with Si-MOSFET are also successfully carried out using CNFET and DG-FinFET for digital circuits.

- The device designed for super-threshold circuits is not optimum under subthreshold conditions. Hence, this thesis proposes new device process parameters to improve the subthreshold slope and $I_{ON}/I_{OFF}$ to enhance speed of subthreshold circuits with reduced switching energy using TCAD tool.

### 1.3 Thesis organization

The core chapters of this thesis, from Chapter 3 to Chapter 8, are a collection of manuscripts published in reputed journals. This thesis specially targets optimization of the device parameters and interconnects for subthreshold applications. The structure of this thesis is as follows:
Chapter 2 covers overview of technology scaling along with challenges in further scaling the MOSFET device. It then presents review of different sources of power consumption in nanoscale CMOS. In addition, it gives an overview of subthreshold operating region and modeling of subthreshold leakage current. Moreover, this chapter also investigates the effect of PVT variations on subthreshold circuit performance to highlight the design challenges under subthreshold conditions.

Chapter 3 proposes high performance robust switch box for subthreshold FPGA. The first half of the chapter presents an overview of FPGA architecture along with challenging design issues for future subthreshold FPGA whereas the second half focuses on routing switch box design for subthreshold FPGA. This work has been published in ISI indexed International Journal of Electronics.

Chapter 4 investigates the performance improvement of subthreshold FPGA interconnect routing resources like Hex, Double, and Long in terms of delay and switching energy keeping power dissipation at ultra low levels. It then also explores the effect of PVT variations on the performance parameters of routing resources. It then also investigates the suitability of mixed CNT bundle as interconnects for subthreshold FPGA applications. This work has been published in ISI indexed Elsevier’s Microelectronics Journal.

Chapter 5 mainly investigates and compares the performance of single wall carbon nanotube (SWCNT), Cu, and mixed CNT bundle interconnects for different interconnect lengths and biasing levels under subthreshold conditions. It also presents a comprehensive analysis of Cu and mixed CNT bundle interconnects and investigates their performance in terms of delay and energy delay product (EDP) for future subthreshold circuits. This chapter then mainly contributes towards optimizing the geometrical and process parameters of interconnects especially for subthreshold circuits to increase their speed. In addition, it carries out crosstalk analysis with the optimized interconnect geometrical parameters. A part of this work has been accepted for publication in IEEE Transactions on Nanotechnology and the other part is submitted to ISI indexed Elsevier’s Microelectronics Journal.
• Chapter 6 explores global interconnect design challenges for subthreshold circuits. Subthreshold global interconnect at the nanoscale faces driver design challenges and problems due to increased interconnect capacitance. As Cu interconnect is more suitable than SWCNT for real time applications (moderate inversion) for global interconnect, this chapter at first explores the suitability of conventional interconnect strategies and challenges to reduce the total path delay. It also proposes device and interconnect optimization techniques to achieve higher performance and to reduce crosstalk in future subthreshold global Cu interconnects. Furthermore, this chapter also investigates the effect of process and temperature variations on subthreshold interconnects. This work has been published in ISI indexed Elsevier’s INTEGRATION, the VLSI Journal.

• Chapter 7 deals with the performance investigation of emerging nano devices under subthreshold conditions. Operating the Si-MOSFET under subthreshold conditions degrades the circuit performance in terms of speed and also increases the circuit parameters spreading due to PVT variations. Hence, this chapter explores the robustness of most emerging devices against PVT variations. It investigates and compares the performance of most promising upcoming devices like CNFET and DG FinFET in subthreshold region. It then also focuses on the performance investigation of digital blocks under subthreshold conditions. This work has been published in the SCI indexed Journal of Nanomaterials.

• Chapter 8 primarily investigates the effect of different process parameters on the performance of NMOS device design metrics using TCAD under subthreshold conditions. It then optimizes the NMOS device for better value of subthreshold slope and improved $I_{ON}/I_{OFF}$ ratio. This work is submitted in Elsevier’s Microelectronics Engineering Journal.

• Chapter 9 draws conclusions and the summary of the thesis and suggests areas of future research work.

The next chapter reviews technology scaling. It then presents an overview of different sources of power consumption in nanoscale CMOS, subthreshold operating region, and modeling of subthreshold leakage current. Moreover, this chapter also investigates the impact of PVT variations on subthreshold circuit performance to highlight the design challenges under subthreshold conditions.