CHAPTER 6

HARDWARE IMPLEMENTATION OF LCL-T SERIES PARALLEL RESONANT CONVERTER

6.1 INTRODUCTION

In this chapter contains a 300 W, 100 KHz LCL-T SPRC prototype is built. The performance of the LCL-T SPRC is implemented and it’s presented in section 6.2. The converter is analysed for the minimum input voltage \( V_i = 100V \) for RLE load conditions with an output voltage of \( V_o = 94V \). This section includes control circuit implementation of LCL-T series parallel resonant converter and their experimental result is present in section 6.3. The static and dynamic characteristics of the converter are present. The experimental results that confirm the simulation are described and discussed. The results are summarized and provided in the Table 6.2. The simulation results and experimental results of the LCL-T SPRC is provided and compared.

6.2 CONVERTER IMPLEMENTATION

The P89V51RD2 are 80C51 microcontrollers with 64 KB flash and 1024 B of data RAM processor is selected for generating pulses and controls the inverter circuit. It provides a low cost, low power and high performance platform for application such as automotive, industrial automation and power conversion. The block diagram of processor is shown in figure 6.1. Another way to benefit from this feature is to keep the same performance by reducing the clock frequency by half, thus dramatically reducing the EMI.
The key features of the 89V51RD2 are

- 80C51 CPU
- 5 V operating voltage from 0 MHz to 40 MHz
- 64 kB of on-chip flash user code memory with ISP and IAP
- Supports 12-clock (default) or 6-clock mode selection via software or ISP
- SPI and enhanced UART
- PCA with PWM and capture/compare functions
- Four 8-bit I/O ports with three high-current port 1 pins (16 mA each)
- Three 16-bit timers/counters
- Programmable watchdog timer
- Eight interrupt sources with four priority levels
- Second DPTR register
- Low EMI mode (ALE inhibit)
- TTL- and CMOS-compatible logic levels
Figure 6.1 Block diagram of the micro controller

The control circuit of LCL-T SPRC is shown in figure 6.2. A pulse width generator is necessary to control the on time of SPRC. This is accomplished by designing a pulse generator and comparator circuit. The modified version of 89c51 which has added SPI and PWM controllers with which 300 KHz. The frequency of the PWM generator is designed to be equal to the switching frequency of the converter. The rise time and fall time of the pulse generating output is less than one nano-second. By varying the magnitude of the reference voltage the width of the pulse generated is varied. This method is made use of in the closed loop system.
Figure 6.2 Control circuit for generating the driving pulses

The fuzzy controlling program is implemented by this microcontroller. Fuzzy program is programmed using C and compiled by KAIL compiler which is embedded in microcontroller. The Fuzzy algorithm execution should not take more than 1.5ms. The sampling frequency is 1KHz. Operating frequency @3.33 MHz (FOSC=40MHz/12) this speed is highly enough for the application. A drop in the output voltage level triggers the fuzzy controller to increase the output voltage of the inverter by modifying the duty cycle of the inverter switches. Figure shows the pulse width modulation pulses for $S_1$ and $S_2$ of SPRC in closed loop to produce the output. The driving pulses for the inverter circuit is shown in figure 6.3
6.3 RESULT AND DISCUSSION

The LCL-T SPRC is fabricated and tested. A prototype LCL-T SPRC is operating at 300 W, 100 kHz was designed. Microcontroller P89V51RD2 is used to generate driving pulses, these pulses are amplified using the driver IC IR2110, the IRF840 MOSFETs are used as the switches in the bridge converter. The diodes MUR 4100 are used for the output bridge rectifier. The hardware module is shown in figure 6.4. The Agilent Mixed Signal Storage Oscillogram (MSO) of inverter voltage, inverter current, voltage across parallel capacitor, current through inductance $L_1$ and output voltage fed with the RLE load are shown in figures 6.5 – 6.11.

Figure 6.3 Diving pulses for MOSFETs
Figure 6.5 presents the inverter voltage and current, its measure from the point A and B of the bridge inverter measured on the primary of the transformer. It is clearly shown in plot that the power losses in the occurrence of the turn on switching are maintained very low by means of the resonant operation i.e during the switching both the voltage and current are minimum.
Figure 6.5  CH1: Resonant Voltage [Volt. Scale: 40 V/div.], CH2: Resonant Current [Amp. Scale: 0.5A/div.]

Figure 6.6 shows the harmonic spectrum of the inverter side. It can be seen that the harmonic content is minimum and the fundamental THD presents a value of approximately 7.8 %. The plot clearly shows that the spikes are present due to the inverter MOSFETs switching operation, reverse recovery time of the diode and capacitor voltage drop during interval.

Figure 6.6  FFT spectrum for resonant current
It can be seen that the peaks are relatively high, but an almost constant level is presented, which is assured by the primary converter controller. It will drop with load current increase since the heavy load current reflected to primary causes more distortion on parallel capacitor. With FLC the harmonic content on capacitor is reduced significantly.

![Figure 6.7 Voltage across the parallel Capacitor [Volt. Scale: 20 V/div.]](image)

It can be seen from this figure 6.7 that the current contains low harmonics and it presents a nearly sinusoidal shape. Due to this effect in the experimental setup, the transformer and LCL-T SPRC network offers some internal resistance. During MOSFET switching transition, the resonant inductor current is divided into two portions. Half of amount of current charges up the output capacitance of outgoing MOSFET and half of current discharges the output capacitance of incoming MOSFET. So the MOSFET is turned on with zero drain-to-source voltage which results in lossless switch on. When MOSFET is turned off, with capacitive snubber, the most current flows into snubber capacitor and less current goes into channel of MOSFET. As a result, the turn-off switching loss can be greatly reduced.
The series inductor current $L_1$ waveform is shown in figure 6.8 and it is taken on the Agilent Mixed Signal Storage Oscilloscope. The transformer primary current is analyzed in harmonic spectrum analyzer. The figure 6.9 shows the FFT spectrum for current through series inductor $L_1$. It is clearly seen in the plot the unwanted spikes and noise are presented due to the parasitic capacitance, reverse recovery time of the antiparallel diodes, electromagnetic radiation and coupling within the transformer windings. The spectrum of the signal shows the noise components presents in the series inductor $L_1$. 

Figure 6.8 Current through Series Inductor $L_1$ [Amp. Scale: 0.5A/div.]
Figure 6.9 FFT spectrum for Current through Series Inductor L₁

Figure 6.10 shows the output voltage waveform of the converter at steady state. The converter is operated at 100 KHz at resonance frequency. A signal proportional to the rectifier output voltage is compared with the reference voltage. The fuzzy voltage controller processes the voltage error, its output changes the reference voltage of comparator in the pulse generating circuit. This is turn varies the duration of the pulses being applied to the inverter switches to maintain the voltage at the required value. At zero error, the output voltage of the rectifier is at the reference voltage. The control characteristics are observed to closely match the simulation value and the output voltage is seen to be nearly independent of load.
Figure 6.10 Output voltage (CH1: Output Capacitor Voltage [Volt. Scale: 50 V/div.], (CH2: Steady State error for output Voltage 2V, [Volt. Scale: 1 V/div.])

Figure 6.10, CH2 shows the steady state error of the rectifier voltage. It is found that the steady state error voltage is nearly 1V. From the response it can be observed that the peak overshoot is reduced to a greater extent with fuzzy logic controller. Figure 6.11 shows the harmonic analysis of the output voltage. It can be seen that the THD of the output voltage is decreased with the proposed controller. It is observed from the results that the peak overshoot in the output voltage is 1.2 % and the total harmonic distortion is 9% (excepts for a small increase owing to the decrease in circuit drops from RLE load).
The spectrum of the output signal is shown in Figure 6.11. From figures 6.5-6.11, it can be inferred that the performance of the controller has significantly increased. One can conclude that the controller is capable of operating under load-independent operation, again it can be seen that the output follows the reference with good accuracy and better dynamic performances. The LCL-T SPRC is verified by simulation and experimental studies. It is proved from the performance Table 6.1 the experimental results show the control characteristics are observed to closely match the theoretical values and the output voltage is seen to be nearly independent of load.
Table 6.1: Performance measures of Theoretical & Simulink Results for LCL-T SPRC fed with RLE Load

<table>
<thead>
<tr>
<th>Performance measures</th>
<th>Simulation Studies</th>
<th>Experimental Studies</th>
</tr>
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<tbody>
<tr>
<td>Load Voltage in Volts</td>
<td>99.8</td>
<td>94</td>
</tr>
<tr>
<td>Load Current in Amps</td>
<td>2.4</td>
<td>2.25</td>
</tr>
<tr>
<td>Settling Time in millisecond</td>
<td>0.01</td>
<td>1</td>
</tr>
<tr>
<td>% Over Shoot</td>
<td>1</td>
<td>2.1</td>
</tr>
<tr>
<td>Steady state error</td>
<td>0.001</td>
<td>2</td>
</tr>
<tr>
<td>THD %</td>
<td>7.89</td>
<td>9.81</td>
</tr>
</tbody>
</table>

The comparison charts are shown in figure 6.12 and 6.13. The input power variations with output power are plotted and shows in figure 6.12. It is observed that the power drawn decays steeply for lower load and as the load increases the power drawn gradually decreases and remains constant at greater loads. It is also seen that the proposed new control strategy has less load Sensitivity. The results obtained indicate that the FLC is an effective approach for DC-DC converter output voltage regulation. The plots of efficiency as a function of the output power are shown in figure 6.13. It concluded from the plot the LCL-T SPRC is better efficiency by using FLC.
As clearly shown in the above figure 6.12 the control characteristics are observed to closely match the theoretical curve and the output power is seen to be nearly independent of load. The conversion efficiency of the prototype is measured by varying the pulse to the inverter to vary the output power under different loading conditions at 100 V input dc voltage. The full load conversion efficiency of the prototype is measured to be 0.76 and it remains above 0.80 for 100-300 W output power. Out of total 40W power loss in the prototype operating at 300W, a major portion (~20W) is estimated to occur in the MOSFETs and diodes. The rest of losses can be attributed largely to the core and winding loss in transformer and resonant inductor.
CONCLUSION

It can be concluded from the above results that the output follows the reference with good accuracy and converter shown a good tracking performance of the controller. It is found that the FLC was eliminating the overshoot, rise time and high frequency noise suppression. It can be concluded that the fuzzy logic controller was capable of load-independent operation and it can be seen that the converter has better dynamic performance. The LCL-T SPRC was verified by simulation and experimental studies.