CHAPTER 2

PRELIMINARIES AND BACKGROUND

Parallel Processing refers to the concept of speeding–up the execution of a program by dividing the program into multiple fragments that can execute simultaneously, each on its own processor. A program being executed across \( n \) processors might execute \( n \) times faster than it would on a single processor.

It is known that one way for processors to communicate data is to use a shared memory and shared variables. However, this is unrealistic for large number of processors. A more realistic assumption is that each processor has its own private memory and data communication takes place using message passing via an Interconnection Networks (IN).

INs originated from the design of high performance parallel computers. When need felt for more bandwidth that has put them to use in network switches and to connect peripherals to a computer. INs is a major factor that differentiates modern multiprocessor architectures and is categorized according to a number of criteria such as topology, routing strategy, and switching technique. IN is building up of switching elements; topology is the pattern in which the individual switches are connected to other elements, like processors, memories and other switches.

2.1 Interconnection Networks

"Interconnection Networks should be designed to transfer the maximum amount of information within the least amount of time (and cost, power constraints) so as not to bottleneck the system".

INs has a long development history [11–18]. The Circuit switched networks has been used in telephony. In 1950s, the interconnection of computers and cellular automata as few prototypes was developed until 1960 it awaited full use. Solomon in 1962 developed multicomputer network. Staran with its flip network, C.mmp with a crossbar and Illiac–IV
with a wider 2–D network received attention in early 1970s. This period also saw several indirect network used in vector and array processors to connect multiple processors to multiple memory banks. This problem was developed in several variants of multi–stage interconnection networks (MIN). The BBN Butterfly in 1982 was one of the first multiprocessors to use as an indirect network. The binary e–cube or hypercube network was proposed in 1978 and implemented in the Caltech Cosmic Cube in 1981. In the early 1980s, the academic focus was on mathematical properties of these networks and became increasingly separated from the practical problems of interconnecting real systems.

The last decade was the golden period for INs research driven by the demanding communication problems of multicomputer enabled by the ability to construct single–chip Very Large Scale Integration (VLSI) routers. The researchers have made a series of breakthroughs that have revolutionized the digital communication systems. The Torus Routing Chip, in 1985, was one unique achievement. The first of a series of single–chip routing components introduced wormhole routing and virtual channels used for deadlock avoidance. The whole family of chips laid the framework for analysis of routing, flow–control, deadlock and livelock issues in modern direct networks. A flurry of research followed with new theories of deadlock and livelock, new adaptive routing algorithms, and new methods for performance analysis. The research progressed in collective communication and network architectures on a regular basis. By the early 1990s, low–dimensional direct networks had largely replaced the indirect networks of the 1970s and the hypercubes of the 1980s could be found in Cray, Intel, Mercury, and some other machines. The applicability of INs in digital communication systems with the appearance of Myrinet was adopted in 1995. The point–to–point multiple networks technology replaced the use of buses, which were running into a limited performance due to electrical limits and were used in the barrier network in the Cray T3E, as an economical alternative to dedicated wiring. However, the interconnection network technology had certain barriers on design and various researchers and engineers have performed analysis of these networks [15,17,18].

2.1.1 Multi–stage Interconnection Networks

As the acceptance and subsequent use of multiprocessor systems increased, the reliability, availability, performability, and performance characteristics of the networks that interconnect processors to processors, processors to memories, and memories to memories are receiving
increased attention. A brief survey of INs and a survey of the fault–tolerant attributes of MINs are reported in [11,13]. A MIN in particular is an IN consisting of a cascade of switching stages, each containing switching elements (SE). MINs are widely used for broadband switching technology and for multiprocessor systems. Besides this, MINs offer an enthusiastic way of implementing switches used in data communication networks. With the performance requirement of the switches exceeding several terabits/sec and teraflops/sec, it becomes imperative to make them dynamic and fault–tolerant [3,4].

Based on the paths availability the MINs traditionally have been divided into three classes:

1. **Blocking.** In this, there is a unique path between every input/output pair, thus minimizing the number of switches and stages.

2. **Nonblocking.** Any input port can be connected to any free output port without affecting the existing connections.

3. **Rearrangeable.** Any input port can be connected to any free output port. However, the existing connections may require rearrangement of paths.

The typical modern day application of the MINs includes fault–tolerant packet switches, designing multicast, broadcast router fabrics while Systems–on–Chip (SoC) and Networks–on–Chip (NoC) are hottest research topics in current trends [3]. Normally the following aspects are always considered while designing the fault–tolerant MINs: the topology chosen, the routing algorithm used, and the flow control mechanism adhered. The topology helps in selecting the characteristics of the present chip technology in order to get the higher bandwidth, throughput, processing power, processor utilization, and probability of acceptance from the MIN based applications, at an optimum hardware cost. Various researchers have already done sufficient work on regular MINs and irregular topologies were out of limelight. Therefore, it has been decided to work on irregular fault–tolerant MINs dominantly and comparing the same with regular networks based on stable matching.
2.1.2 Network Topology

2.1.2.1 Centralized Switched (Indirect) Networks

In Crossbar network, shown in Figure (2.1), the crosspoint switch complexity increases quadratically with the number of crossbar input/output ports = \( N \), i.e., grows as \( O(N^2) \) and has the property of being non-blocking.

In MINs, the crossbar is split into several stages consisting of smaller crossbars and the complexity grows as \( O(N \log N) \), where \( N \) is the number of end nodes. The Inter–stage connections are represented by a set of permutation functions. Figure (2.2) is an omega network, with 8 sources and 8 destinations communicating with each other using a MIN. The routing in the said network is done on the basis of perfect shuffle–exchange. Further, using Figure (2.3) a 16 port, 4 stage Omega network have been shown.

**Figure 2.1. Crossbar Network.**

**Figure 2.2. An Omega Network.**
MINs interconnect $N$ input/output ports using $k \times k$ switches, $\log_k N$ switch stages, each with $N/k$ switches and $N/\left(k \log_k N\right)$ total number of switches. As the MINs size increases the cost also increases and the reduction in MINs, switch cost comes at the price of performance. The Network has the property of being blocking and the contention is more likely to occur on network links moreover the paths from different sources to different destinations share one or more links. Figure 2.4(a–b) shows the circuits with non–blocking and blocking topology.
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