Chapter-1

Introduction

The telecommunication has been started with the development of electric telegraph by *William Cooke and Charles Wheatstone* that became commercial in 1838 [1]. This technology was rapidly replaced by *Samuel Morse*, with the introduction of the ‘Morse code’ first introduced in 1844, which reduced the communication into dots and dashes, and listening to the receiver [2]. In 1906, *Lee De Forest* introduced the three-element vacuum tube detector, opening the future to vacuum tubes for electronic applications as in the radio. The cellular phones are no doubt the most popular wireless communication system currently in use. Such a system can be divided into the user part (handset) and the infrastructure part (base stations). The user part consists of a transmitter and a receiver commonly known as transceiver system [3, 4].

1.1. Transceiver Systems

A sample heterodyne radio-frequency (RF) transceiver front-end system is shown in Fig. 1.1. In this architecture, the received RF signals are first passed through a band-pass filter, and then switched to a low noise amplifier (LNA). Due to its gain, the LNA essentially sets the signal to noise ratio for the receiver chain. The amplified signals are filtered for improved image rejection and down-converted to an intermediate frequency (IF) with a mixer. The signals at IF are then filtered for channel selection and shifted in frequency to baseband by a second mixer [5-7]. The transmission process is complementary to the reception process. During transmission, the signals at baseband are up-converted to the RF carrier using an IF stage. The power amplifier (PA) is used to drive the antenna. A transceiver (T/R) switch is used to connect/disconnect the antenna for transmit and receive processes. The direct down-conversion or homodyne architecture mixes the incoming RF signals with the carrier frequency to generate signals directly at baseband. Similarly, the signals are directly up-converted to the RF carrier using only one mixing step during transmission. The integrated circuit design industry is increasingly improving the direct down-conversion architectures to facilitate further integration by reducing the number of components required. This architecture uses standard CMOS technology and includes a LNA and PA on the same piece of Silicon.
Highly integrated transceiver solutions for the 802.11b, g standards have also been presented by Chien [8] and Kluge [9]. Amongst these blocks of Fig. 1.1, the transceiver switch stands out as a candidate for on-chip integration because the MOSFET device is optimized to operate as a switch. In early days the radio transceiver switches have been designed using PIN diode and FET, which consume more power. As the modern portable devices demands less power consumption switches, therefore, the PIN diodes and FETs are gradually replaced by the MOSFETs such as n-type MOSFET and p-type MOSFET [11, 12]. The MOSFET analog switches use the MOSFET channel as a low ON-resistance switch to pass analog signals at switch-ON condition and as high impedance at switch-OFF condition. The signals flow in both directions across a MOSFET switch. The source is a negative side for n-type MOSFET or more positive side for p-type MOSFET. All of these switches are limited on what signals they can pass or stop by their gate source voltage, gate drain voltage and source drain voltages; exceeding the voltage, current, or power limits will potentially damage the switch.

A traditional MOS switch has better performances but only for a single operating frequency. For multiple operating frequencies, high signal distortions are observed, which results in an unrecognizable information signal at the receiver end [13, 14]. The CMOS switch uses one n-type MOSFET and one p-type MOSFET to counteract the limitations of the single-type switch. To turn the switch ON, the gate of the p-type MOSFET is driven to the low potential and the gate of the n-type MOSFET is driven to the high potential. For voltages between $V_{DD} - V_m$ and Gnd−$V_{Ip}$, both MOSFETs conduct the signal, for voltages less than Gnd−$V_{Ip}$, the n-type MOSFET conducts alone and for voltages greater than $V_{DD} - V_m$, the p-type MOSFET conducts alone.

![Diagram](image)

Fig. 1.1. Simple RF transceiver architecture [10].
The RF/microwave switching elements using Si-CMOS technology are being investigated and presented as an alternative to the traditional PIN diode and GaAs MESFET devices. Si-CMOS RF switching elements are attractive because of their potential application in all Si monolithic CMOS solutions for completely integrated baseband and RF functions in low cost wireless, mobile satellite and personal communications systems. RF switches can be used at several places in RF front-ends. In a transceiver switch, a Double-Pole Single-Throw (DPST) arrangement of switches multiplexes the use of the antenna between the PA and LNA. Transceiver switches must have a high linearity to ensure that the high power signals (~2 W) at the output of the PA are transmitted to the antenna with minimum distortion. This linearity requirement presents a serious challenge in integrating transceiver switches into on-chip designs especially as the supply voltage in standard CMOS continues to decrease.

In addition to the transceiver switch application mentioned above, RF switches could be used to select capacitors, Fig. 1.2, for example, tuning of a voltage controlled oscillator (VCO). In this application, the challenge is to obtain a low ON-state resistance and a low OFF-state capacitance. In a given technology, the ON-state resistance and OFF-state capacitance are inversely related to each other. Since the resistance-capacitance product in a modern CMOS technology is not as low as desired [15, 16].

In the receiver part of a handset, low noise RF transistors are used to amplify the incoming signals. As in any LNA, the use of low or minimum noise figure transistors is desired. The noise requirements for the RF devices for this application are, however, not as stringent as those for satellite communications. In wireless communications, the receiver experiences the noise of the whole environment, which is interference dominated, whereas in satellite communications the signal comes from the sky with less background noise [17].

Fig. 1.2. Switching application in RF circuits as switching capacitors [16].
Consequently, for wireless communications, the noise produced intrinsically in the RF devices is somewhat negligible comparing to that from the noisy environment. Another requirement for the handset is the reduction of power consumption. At present, a supply voltage of 3 V has been established as a standard. To deliver a high output power combined with a high efficiency at a limited supply voltage of 3 V, RF power transistors possessing a large ON-current and a low ON-resistance are required in the transmit section of the handset.

The dominant power RF transistor used in base stations of wireless communications systems with operating frequencies up to 2.5 GHz is the Si lateral diffused (LD) MOSFET, which in the last several years has replaced all other competing Si and GaAs transistors [18]. Si-LDMOSFETs combine the advantages of moderate cost, high reliability and extremely high output power.

1.2. RF Switches

In the antenna selection system, signals from a subset of the antennas are processed at any time by the limited bandwidth of RF, which is available for the receiver. Hence, the transmitter needs to send pilots multiple times to enable the receiver to estimate the channel state of all the antennas and select the best subset. In the radio transceiver of the advanced communication systems, multiple antenna system is used to replace the traditional single antenna circuitry to improve the transmission capability and reliability. With the multiple antennas, data transfer rate can be increased by the same factor. For example, if we have three antennas as a1, a2, a3 used in the transceiver, then data transfer rate will increased by ‘3’ as it is number of antenna used. For such communication system, antenna selection and switch mechanism is essential to circumvent the uses of several RF chains, associated with the various antennas. The desired switching system must have a simple and low cost structure which also confined all the improvement of multiple-input, multiple-output (MIMO) systems [19, 20].

A traditional n-MOS Single-Pole Double-Throw (SPDT) switch has good performance but only for a single operating frequency. For multiple operating frequencies, high signal distortions are easily observed, which results in an unrecognizable information signal at the receiver end. To be able to transmitting or receiving information through the multiple antennas systems, known as MIMO systems, it becomes necessary to design a new RF switch that is capable of operating with
multiple antennas and frequencies as well as minimizing signal distortions and power consumption [21, 22]. For this purpose, we have proposed a model of Double-Pole Four-Throw (DP4T) RF CMOS switch and achieved a better performance with respect to drain current, switching speed and the voltages as compared to the Single-Pole Double-Throw (SPDT) [23], Double-Pole Double-Throw (DPDT) [24], and Single-Pole Four-Throw (SP4T) [25] switches. The device structures with different layouts and widths are studied to understand the effect of device geometry. This proposed switch is low in cost and capable of selecting data streams to or from the two antennas for transmitting or receiving processes, respectively.

We start with a basic CMOS inverter switch and go upto Double-Pole Four-Throw Double-Gate (DP4T DG) RF CMOS switch. It is designed with low insertion loss and low control voltage. The advantages of this proposed CMOS inverter switch is its minimal distortion and negligible voltage fluctuation, and does not require large resistance at the receiving end. It showed a better performance than DPDT in insertion loss, compression point, and control voltage. In addition, DP4T switches can be easily implemented into MIMO systems to increase diversity and system capacity due to the multiple antenna usage. Finally, we have designed a novel Cylindrical Surrounding Double-Gate (CSDG) MOSEFT.

Huang [25] fabricated a SPDT transceiver switch [26] for 3.0 V for a 0.5-µm CMOS process. This analysis shows that substrate resistances and source/drain to body capacitances must be lowered to decrease insertion loss. This switch exhibits a 0.7 dB insertion loss, 17 dBm compression point (P1 dB), and 42 dB isolation at 928 MHz. The switch has adequate insertion loss, isolation, P1, and IP3 for 900 MHz. The ISM band applications requiring a moderate peak transmitter power level (~15 dBm). To avoid the uses of multiple RF chain associated with the multiple antennas (used to replace traditional single antennas circuitry in the radio transceiver system in order to improve the transmission capability and reliability), RF switch is most essential component. Mekanand and Eungdamorang [27] have proposed the DP4T RF CMOS switch at frequencies 2.4 GHz and 5.0 GHz exhibits an insertion loss of 0.75 dB and 0.86 dB, respectively with compression point of 31.86 dBm and realizes the minimal distortion, negligible voltage fluctuation, and low power supply of only 1.2 V, which is used in wireless local area network (WLAN) and other advanced wireless communication systems. They also discussed the advantages of switch using a CMOS, instead of a single
n-MOS switch in the dynamic range. This dynamic range in the ON-state is significantly increased, which allows a full signal swing. Moldovan et al. [28] have demonstrated the analytically compact undoped DG MOSFET model and forecast the effect of volume inversion on the intrinsic capacitances and shows that the transition from volume inversion regime to the double-gate behavior. This result shows that the intrinsic capacitances are larger as well as limit the high speed (delay time) behavior of the DG MOSFETs under volume inversion regime. Lee et al. [29] have presented a novel architecture for the DPDT, DP4T, and 4P4T RF switches with simple control logics and high power handling capabilities, which require only one, two and three control lines, respectively. The developed DPDT switch demonstrates 1.0 dB of insertion loss, 19 dB of isolation, and 31 dBm of input $P_1$ dB, 34.5 dBm of input $P_1$ dB in 3/0 V operation at 5.8 GHz. The DP4T and 4P4T switches exhibit 1.8 dB, 2.8 dB insertion loss, and 23/37 dB, 20/35/55 dB of isolation, respectively, and 31 dBm of input $P_1$ dB, 35 dBm of input $P_1$ dB in 3/0 V operation at 5.8 GHz.

Woerlee et al. [30] have presented the impact of scaling on the analog performance of MOS devices at radio-frequencies and explored the trends in the RF performance of nominal gate length of n-MOS devices from 350-nm to 50-nm CMOS technologies. The RF performance metrics such as the cut-off frequency, maximum oscillation frequency, power gain, noise figure, linearity, and 1/f noise were explored in the analysis [31]. The minimum gate length of n-type MOSFET devices as 350-nm, 250-nm, and 180-nm CMOS technologies were studied.

Lee [32] has presented the standard digital CMOS process which offers number of ways to improve the characteristics of on-chip passive elements. In particular, it is possible to reduce significantly the severity of substrate loss. It is clear from [33] that the scaling trends properly exploited and combined with new insights into the device and oscillator noise enables the CMOS IC technology to perform at GHz frequencies to make it attractive for application specific once thought the sole province of more exotic technologies.

These advantages include high integration capabilities and excellent electrostatic discharge (ESD) robustness. Some RF switches do not require external DC blocking capacitors and have the control logic fully integrated. With CMOS compatible logic levels, the need for external level shifters is eliminated, as there are no any external components are required. So, the RF switches enable the really tiny board designs.
1.3. RF MOSFETs

RF MOSFETs are the MOSFETs that are designed to handle high power RF signals from devices such as stereo amplifiers, radio transmitters, and television monitors. These transistors are turned ON and turned OFF by input voltages and function as miniature electronic switches. Like other semiconductor devices, RF MOSFETs are made of materials such as Silicon (Si) or Germanium (Ge) and doped with impurities to induce changes in electrical properties. Voltage is applied between the gate and source terminals, modulating the current between the source and drain. Typically, a thin layer of oxide insulation is used to prevent current from flowing between the gate and a conductive channel in the semiconductor substrate [34].

Aside from cellular phones, several other RF systems with operating frequencies below 20 GHz are potential fields for the application of RF MOSFETs as well. For example, Bluetooth, in which the requirements of transistors RF performance are quite moderate, is predestined for RF MOSFETs [35]. For other applications below 20 GHz but with more stringent requirements concerning RF performance, the combination of SiGe HBTs and CMOS (SiGe BiCMOS) is currently a heavily discussed possibility in industries [36, 37]. The RF MOSFETs also seem to fulfill most of the performance requirements for civil RF systems with operating frequencies up to 6 GHz [38]. The RF CMOS transistors are combination of n-channel MOSFET and p-channel MOSFET. With both types of devices, the polarity of the electric field that controls the current in the channel is determined by the majority of carriers in the channel. The selection of RF MOSFETs requires an analysis of performance specifications, such as:

1) Drain-source breakdown voltage is the maximum drain to source voltage before breakdown with the gate grounded.

2) Power gain in dB is a measure of power amplification, is the ratio of output power to input power.

3) Noise-figure in dB is a measure of the amount of noise added during normal operation, is the ratio of the signal to noise ratio at the input and the signal to noise ratio at the output.

4) Power dissipation in W or mW is a measure of total power consumption.

Some other performance specifications for RF MOSFETs include the maximum drain saturation, common-source forward transconductance, operating frequency, and output power. The devices that operate in depletion mode can increase or decrease their
channels by an appropriate gate voltage. By contrast, devices that operate in enhancement mode can only increase their channels by an appropriate gate voltage. Some bipolar RF MOSFETs are suitable for automotive, commercial, or general industrial applications. RF MOSFETs vary in terms of operating mode, packaging, and packing methods.

1.4. Issues of RF MOSFET Modeling

In a MOSFET, the number of free carriers available in the channel is mostly controlled by the field induced from the gate voltage, but a change in the body potential can also affect the number of channel carriers. At low frequencies, the impedance of the junction capacitance is so large that the substrate impedance may not be seen from the drain terminal, and a MOSFET can be modeled as a three-terminal device [39]. This three-terminal device can be treated as a two-port network, where four complex numbers are sufficient to characterize the device. On the other hand, nine complex numbers are required to characterize a three-port network, such as a four-terminal device. Even if the three-port measurements are possible, many bias combinations for the ac characteristics will need to be considered, and the measurements and parameter extractions become impractical and time consuming. In spite of these problems, intensive efforts have been devoted to RF MOS modeling and parameter extraction.

A traditional n-MOS switch uses n-MOS as transistors in its main architecture, and requires a control voltage of 5.0 V and a large resistance at the receivers and antennas to detect the signal. A CMOS IC switch is an integrated circuit using FETs to achieve switching between multiple paths. Because of its high value of control voltage, it is not suitable for modern portable devices which demand smaller power consumption.

The aggressive scaling of MOSFET has led to the fabrication of high performance MOSFETs with a cutoff frequency more than 150 GHz [40]. As a result of this development, the CMOS is a strong candidate for RF wireless communications in GHz frequency range. Accurate device models are, however, needed to design the advanced analogue RF circuits and in this regard, various researcher proposed some parameters for cell design as used for RF switch circuits [21-25, 41]. CMOS is nowadays a real choice for RF circuitry due to its fast devices and low cost, which is due to the simple process. Large cellular systems can now be processed on a single chip containing most of the transceiver blocks at RF and baseband. Previously, to achieve the performance of GaAs
switches, the CMOS based RF switches had to be manufactured on dedicated and more expensive sapphire wafers. The new Infineon’s RF switches combined the benefits of CMOS with outstanding RF performance. The switches have RF performance traits such as low insertion loss, low harmonic distortion, good isolation and high power levels. The RF switches also have the inherent CMOS advantages including high integration capabilities, cost effectiveness, and excellent electrostatic discharge (ESD) robustness.

Continuous scaling of CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a severe part for RF applications in the GHz frequency range. With the scaling of device dimensions and increase in the short channel effects (SCE), multiple-gate transistors have been investigated to obtain an improved gate control characterization [42-44]. Due to these advantages, there has been growing interest in modeling of RF CMOS which is especially striking for various applications because it allows integration of both digital and analog functionality on the same die, increasing performance at the same time as keeping system sizes reserved [45-48]. An excellent improvement in the frequency response of Si-CMOS devices has explored their application in the microwave/millimeter wave regime of the electromagnetic spectrum for various wireless communication systems such as high capacity wireless local area network, short range high data rate, wireless personal area networks, and collision avoidance radar for automobiles.

Enormous progress has been made to scale the transistors to ever smaller dimensions to obtain faster transistors, as well as to lower the effective costs per transistor in terms of transistors per unit area. Several circuit parameters have high performance and have been designed and optimized for the generalized application [49-51]. For the investigation of circuit-level degradation a CMOS inverter is analyzed. A major advantage of CMOS technology is the ability to combine complementary transistors, n-channel and p-channel, on a single substrate.

Recently, the CMOS transistor uses the technique of Silicon-on-insulator (SOI), which is very attractive because of the high speed performance, low power consumption, its scalability and effective potential [52, 53]. As compared to the bulk Silicon substrate, the architecture of SOI MOSFET is more flexible due to several parameters such as thicknesses of film and buried oxide, substrate doping, and back gate bias which is used for optimization and scaling. The short channel effect, junction capacitances, and doping fluctuation are mitigated in ultra-thin SOI films [54, 55]. The main advantage of SOI
compared to bulk Silicon is its compatibility with the use of high resistivity substrates to reduce substrate coupling and RF losses [46]. Saha [57] has solved a problem of critical issue with the continued scaling of MOSFET devices towards their ultimate dimensions near 10 nm regime, and defined the process variability, induced device performance variability has become a critical issue in the design of very large scale integrated (VLSI) circuits using advanced CMOS technologies.

Manku [58] has discussed the design issues and the microwave and RF properties of CMOS devices and a qualitative understanding of the microwave characteristics of MOS transistors is provided. This design is helpful for integrated circuit design to create better front-end RF CMOS circuits and presented the network properties of CMOS devices, frequency response, microwave noise properties and scaling rule. Srivastava et. al. [59] have designed a model for a capacitor device using MOS layers with an oxide thickness of 528 Å (measured optically), and measured the material parameters from the curve drawn between capacitance versus voltage and capacitance versus frequency through the Visual Engineering Environment Programming (VEE Pro) software. In this research, to find good result Srivastava et. al. [59] varied the voltage with smaller increments and performs the measurements.

Litwin [55] presented a model for gate resistance ($R_g$) component in silicided polysilicon gate MOSFETs and discussed the high frequency properties depend critically on $R_g$. These results show that the contact resistance between silicide and polysilicon, built into the gate of a typical MOSFET, is of the same magnitude as the silicide sheet resistance. Srivastava et. al. [60, 61] have presented a model for a capacitor device, oxide thickness of 510 Å, measured the oxide thickness by the Stanford University Process Engineering Model Version 0-83, commonly known as SUPREM simulator and then proved that the thickness by using other method with the LCR meter and VEE Pro software are same. Its accuracy depends on the quality of models, parameters and numerical techniques it employ and also verify the result by measurement of capacitance at different voltages using LCR meter. Based on this oxide thickness measurement of a MOS capacitor, one can measure the device parameters, mainly the substrate dopant concentration.

Ye and Cao [62] have realized that the random variations have been regarded as one of the major barriers on CMOS scaling and proposed a compact 3-D model and perform the atomistic simulations to investigate the fundamental variations in a scaled CMOS
device, including random dopant fluctuation (RDF), line edge roughness (LER), and oxide thickness fluctuation (OTF). These models are scalable with device specifications, enabling quantitative analysis of circuit performance variability in future technology nodes. Caverly et. al. [63] have fabricated some cells using standard processes of 2.0-μm, 1.2-μm and 0.8-μm CMOS integrated circuit with no post-processing performed. The results indicate that 2.0 μm CMOS can be used successfully up to approximately 0.25 GHz with 0.8 μm cells useful up to approximately 1 GHz. Srivastava et. al. [64] have investigated the design parameters of RF CMOS cells which are suitable for switch in the wireless telecommunication systems and this results for the development of a cell library which includes the basics of the circuit elements required for the radio frequency sub-systems of the integrated circuits such as voltage-current (V-I) characteristics at low voltages, contact resistance which is present in the switches and the potential barrier with contacts available in the devices.

Rapid integrated system designs are the use of cell libraries for various system functions [65, 66]. In digital system design, these standard cells are both at the logic primitive level as well as higher levels of circuit functionality. For baseband analog systems, standard cell libraries are less frequently used. In the design of a CMOS RF cell library, the cells must be designed to be flexible in terms of drive requirements, bandwidth and circuit loading. For RF applications, the widespread drive requirements for off-chip loads are based on 50 Ω impedances. This impedance is a good compromise between lowest loss and highest power handling for a given cable size. Also, this impedance caught on for RF transmission rather than the well established 75 Ω that had been used for video transmission. A factor governing the bandwidth of the RF cells is the nodal capacitance to ground, primarily the drain and source sidewall capacitances [67, 68]. Since these cells are to be used with digital and baseband analog systems, control by on-chip digital and analog signals is another factor in the design [69].

The library consists of cells design, using standard Micro-Cap 2.0-μm and 0.8-μm CMOS processes. For the technologies studied, these control voltages varied between 0.0 V and 2.1 V, with the supply voltage of 1.2 V is of interest for low power consumption portable system applications. The cells have been designed for the purpose of radio frequency communication switch devices and high power RF MOSFET targets VHF applications. Transistors designs for the purpose of library elements are usually planned with multiple gate fingers to reduce the capacitances of sidewall. This increases
the contact resistance and reduces the barrier height. The properties for RF CMOS switch design for the application in communication [70] and designed results are presented in the Chapter 2 and have been designed with and optimized for the particular application. Higher drain current can be easily achieved by using higher number of gate-finger which is also analyzed.

The 5.0 GHz upper frequency is important because it includes several commercial communications bands. Although the 2.0 μm cells had a lower operating frequency range than the smaller process geometries, this technology is still useful for several applications such as the processing of RF signals in the 250 MHz range. The design goals were met for all the cell library elements such as RF control elements, single ended class-A amplifier, RF isolator, and Gilbert cell mixer circuit. In cell libraries of the RF MOSFET, designed cells should have elasticity for working frequency range, driving capability, and loading of devices or circuits. For RF applications, generally we used off-chip load impedance, which is of 50 Ω [71, 72]. RF MOSFET has feature of best noise figure and gain, excellent cross-modulation, ESD robustness protected via on-chip gate protection diode, 5th generation MOSFETs, for example BF5030W, BG5120K fulfill the stringent technical requirement from the digital tuners, and as well support low power 3 V designs, automotive quality [73].

The performance of a transceiver switch is characterized by several parameters in transmits and receives modes such as insertion loss, isolation, return loss, linearity, power, ESD reliability, ON-resistance and capacitances [74, 75]. Optimizing the performance of a MOSFET as an analog switch requires a number of trades-off. If the width to length ratio is increased to reduce $R_{ON}$, the parasitic capacitance of the gate oxide will increase proportionately resulting in lower bandwidth. There are many factors that affect $R_{ON}$ such as temperature, input voltage, supply voltage, and gate length. The $R_{ON}$ is application specific. For low signal, high speed applications, small $R_{ON}$ is required to maintain the integrity of the input signal throughout the device. If the use is for audio, a low $R_{ON}$ may not be as important due to the lower frequencies and power of the signal.

If a MOSFET is being used for a power application as the source to drain voltage increases a larger source to drain breakdown voltage is required, therefore increasing the value of $R_{ON}$. In order to design a switch or any type of MOSFET device, a complete understanding of the application is required. In the p-MOS gate region, an increase in the
parasitic capacitance is a concern at high frequencies. In this situation, the gate oxide becomes an issue especially at high frequencies. The source to substrate capacitance, the drain to substrate capacitance, and the source-to-drain Miller capacitance all have an effect on $R_{ON}$. As the frequency of the input signal increases, these capacitances can increase insertion loss and decrease off isolation. With $R_{ON}$ being non-linear and a strong function of voltage and temperature, an analog switch should not be used in any critical resistive voltage divider path in a circuit. The ESD performance of the switch is usually measured using the human body model (HBM) method. This method essentially measures the robustness of the part when subjected to a static discharge arising from human contact. In applying this model, a 200 pF capacitor is charged to a certain voltage and then discharged through the device under test (DUT).

The DUT breaks down and ceases to function as the voltage on the capacitor exceeds a certain threshold. This breakdown voltage is used as a measure of the ESD reliability of the DUT. Most of the GaAs RF components are rated at 500 V HBM. Other practical requirements of the transceiver switch include robustness with respect to antenna mismatch. Also, control voltage levels used to toggle the state of the switch must be available in the system. The turn ON and turn OFF times typically must be less than about 10 ns to enable rapid transition between $T_x$ and $R_x$ modes, although specific values depend on the application [76].

1.5. Organization of the Thesis

This thesis aims to understand the limitations of existing RF switches and to investigate new ways of designing RF switches with improved performance in conventional Silicon integrated circuit technology using double-gate (DG) MOSFET. The switch discussed in this thesis is a DP4T switch. The organization of the thesis is as follows:

Chapter 2 concerns with the DP4T switch and CMOS inverter. The SPDT is the fundamental switch that links between antenna and the analog front-end section but due to the single operating frequency, this type of switch has a limited data transfer rate. Therefore, we proposed a DP4T CMOS switch designed with inverter technology.

Chapter 3 presents the benefit of DG MOSFET as compared to SG MOSFET. A symmetrical DG MOSFET have been modeled and simulated including the basics of the circuit elements parameter required for the RF sub-systems of the integrated circuits
such as drain current, output voltage, threshold voltage, capacitances, resistances at switch ON condition, oxide thickness, resistance of poly-silicon, number of bulk capacitors, and power or voltage gain.

Chapter 4 focuses on modeling of DP4T switch using DG MOSFET technology. High frequency phenomena such as capacitive, drain current effects in the substrate are modeled and characterized in detail using simulations. It includes the basics of the circuit elements parameter required for the radio frequency sub-systems of the integrated circuits such as threshold voltage, resistances, capacitances, insertion loss, isolation, compression point and switching speed.

Chapter 5 proposes the basic concept of a CSDG MOSFET. In the DG MOSFET, the gates are only on the two sides. We have widened the gate on all-around the device and design like a cylinder. So, we extend this work for the CSDG MOSFET. Using the optimized models, the design, and simulation results of an integrated transceiver switch is presented.

Finally, we conclude the thesis and recommend the future scope of the work in Chapter 6.