Chapter-6

Conclusions and Future Scope

6.1. Conclusions

After modeling of the symmetrical DG MOSFET, we have drawn the layout and simulate with the parameters available in the MOSFET. It includes the basics of the circuit elements parameter required for the radio-frequency sub-systems of the integrated circuits such as drain current, output voltage, threshold voltage, capacitances, resistances at switch ON-condition, oxide thickness, resistance of polysilicon, number of bulk capacitors, and power or voltage gain. For the purpose of RF/microwave switch, we have explored the methods to minimize control voltage, resistance for the switching condition and capacitances for isolation. A DP4T CMOS inverter switch has been designed with low insertion loss and low control voltage. A DP4T RF CMOS switch design using independently controlled double-gate has been discussed and the impact on the power consumption with respect to ON-resistance and current, propagation delay, leakage behavior as well as area of the device is presented, which shows that the numbers of transistor are reduced with the application of DG MOSFET and also the area can be significantly reduced for logic gates, therefore, the logic density per area increases. Favorable condition for low power circuit is that, where both transistor gates are on the same potential contribution even a reduced amount of leakage current. The proposed DP4T RF CMOS switch design with double-gate transistors modifies the conventional analog switch circuit design to operate with digital signals to achieve isolation buffering for bidirectional signals and high density packing of multiple buffer switches operating under single enable control in a single package.

In the DG MOSFET, the bulk voltage is zero, so we achieved the higher drain current. We have reported the attenuation of 0.005 dB to 0.016 dB for 45-nm technology compared to the attenuation of 0.020 dB to 0.070 dB for 0.8-μm technology. Off-isolation and switching speed are significantly improved in the proposed DP4T DG RF CMOS switch over the already existing CMOS switch. Moreover, the flat-band capacitance and power dissipation becomes half and threshold voltage as well as flat-band voltage is reduced as flat-band capacitance becomes half for the proposed DP4T DG RF CMOS switch. The half power dissipation has been discussed for the
proposed DP4T DG RF CMOS switch and compared the results with the already existing CMOS switches. Ultra thin body SOI FETs suggests a very thin Silicon body to achieve better control of the channel by the gate and hence, reduces the leakage and short channel effects. By the use of the intrinsic or lightly doped body, in the DG MOSFET, reduction in the threshold voltage occurs due to random dopant fluctuations, which enhances the mobility of the careers in the channel region and therefore increment in ON-current occurs. Using the designed capacitive model of the DP4T DG RF CMOS switch, the equivalent circuit of this model for the switch, and simulated S-parameters are presented. For the purpose of RF switch, we have achieved the process to minimize the ON-resistance and maximize the parasitic capacitance and minimize the control voltage to control the isolation and switching speed for the switch ON condition with DP4T DG RF CMOS switch. Since the operating frequencies of the RF switches are in the range of few MHz to 60 GHz, therefore, it is useful for modern broadband wireless communication systems. The proposed DP4T DG RF CMOS switch results the peak output currents around 0.387 mA and switching speed of 36 ps. A device structure with a double-gate contact shows a significant improvement in currents and switching speed as compared to the single-gate structure.

For increasing the gate voltage, the drain current increases, hence the contact resistance decreases which increases the cut-off frequency. Therefore, for the purpose of RF switch, where control voltage should be low and then current flow will be less and in terms of contact resistance, it will increases with increase in number of gate-fingers. So, in the application of RF switch, we have tried to increase the gate-finger. From the simulated result of DG MOSFET, we conclude that (for the DG MOSFET, bulk voltage is zero), highest drain current can be easily achieved by using higher gate-fingers. As at higher gate-fingers, it also enhances the mobility of the careers in the channel region as compared to the lower gate-fingers due to intrinsic or lightly doping and therefore increment in drain current occurs at higher gate-fingers.

We have analyzed the designing parameters of a CSDG MOSFET. The proposed CSDG MOSFET device is operating at the microwave frequency regime of the spectrum. For the purpose of RF or microwave switch, we achieved the process to minimize control voltage, capacitances for isolation and the resistance for the switching condition and increased energy storage of a device. From the discussions in previous chapters we have achieved a better CSDG MOSFET as compared with CSSG MOSFET.
A CSDG MOSFET has been designed and we simulated the parameters available in this model, by using the PSpICE and ADS. It includes the basics of the circuit elements parameter required for the radio frequency sub-systems of the integrated circuits such as drain current, output voltage, threshold voltage, capacitances, resistances at switch ON condition, oxide thickness, resistance of polysilicon, energy stored, cross talk, number of bulk capacitors, and power or voltage gain. For the RF/microwave switch, we have achieved the process to minimize the control voltage, capacitances for isolation and the resistance for the switching condition and increased energy storage of a device. The mobile charge density is calculated by using the analytical expressions obtained from modeling the surface potential as well as the difference of potentials at the surface and at the center of the Silicon doped layer. The analytical expressions for the charge characteristics are presented as the function of Silicon layer impurity concentration, gate dielectric and Silicon layer thickness with the variable mobility.

6.2. Future Scope

Beyond the analyzed parameters in this work, the proposed CSDG MOSFET has potential challenges such as the fabrication of this kind of devices by a tricky process. In the presented work, we apparently restrict our comparative analysis of the different devices to an applied high drain biasing. As a consequence, the comparisons have been made, particularly, in regard to the RF performance and saturation regime, the most important of which are transit frequency, \( f_T \) (sub threshold swing and OFF-current), which is not covered in this work that is imperative for the wireless applications. Another decisive factor for microwave application is the hot carriers effect, which affect the device degradation for high power and high frequency applications, which can also be taken into account in the future works. In general, the physical oxide thickness is determined by Ellipsometer, but its accuracy cannot be guaranteed for those of very thin oxides.

As a consequence of the power-supply voltage being reduced much less proportionally to the channel length, the lateral electric field will be increase in the device. Carriers which move from the source to the drain in such a turned-ON transistor can get enough energy to cause impact ionization that generates electron-hole pairs in Silicon and surmount the interfacial energy barrier. The energy of the hot carriers depends mainly on the electric field in the pinch-off region. The carriers injected into a
gate dielectric induce device degradation such as threshold voltage \( V_{th} \) shift due to occupied traps in the oxide and reduced drain current \( I_{ds} \). Hot carriers can also generate traps at the Silicon-oxide interface leading to subthreshold swing deterioration and stress-induced drain leakage. Therefore, hot carrier injection degradation significantly reduces the transistor lifetime. The n-type MOSFET is more sensitive to hot carrier injection than the p-type MOSFET transistor, since electrons become hotter than holes due to their higher mobility and energy barrier is lower for electrons compared to holes at the interface. However, to solve this issue, drain engineering is used to alleviate the peak of the lateral electric field located close to the drain edge by modifying the drain doping profile through introduction of source/drain extension implants by a lower dose.

Another approach is using high resolution transmission electron microscopy analysis. This method is more accurate, but still suffers from high cost and low throughput. In addition, the thickness measured with these methods is physical thickness. It cannot be employed to determine the equivalent oxide thickness of the high dielectric constant (high-k) materials, proposed for future ULSI CMOS applications, because dielectric constants of these materials are different to that of oxide.

We can extend this work with a replacement of SiO\(_2\) with HfO\(_2\) as a high dielectric material. Hafnium-dioxide (HfO\(_2\)), is a high dielectric, low absorption material usable for coatings in UV (~250 nm) to IR (~10 \( \mu \)m) regions, its adhesion is superb to metals such as Aluminum and Silver. In the presented work, CMOS with pure SiO\(_2\) is adopted for DP4T DG MOSFET switch to detect the signals to/from transceivers and the performance of this DP4T DG RF CMOS switch at 45-nm technology was demonstrated. In the future work, performance of HfO\(_2\) for switch as effective \( R_{ON} \), attenuation, flat-band capacitance, average dynamic power, and working efficiency at high temperature can be investigated. In the DP4T switch, effective resistance \( R_{ON} \) should be less and it is inversely proportional to intrinsic trans-conductance (which is higher in HfO\(_2\) compare to SiO\(_2\)), so it is better to use HfO\(_2\) for a DP4T switch. Also, the attenuation is directly proportional to \( R_{ON} \), so it can be improved by using the HfO\(_2\).