The PAL equations for the Network Interface Card are:

\[ CS = !(!AEN \& !A9NANDA8 \& !A7 \& !A6 \& !A5 \& !A4 \& !AO) \]

The Chip Select (CS) signal decodes the address 300H.

\[ LDPORT = !(!AEN \& !A9NANDA8 \& !A7 \& !A6 \& !A5 \& !A4 \& !AO \& !IOWR) \]

The LDPORT decodes the address 301H and it is active only during I/O write cycles.)
The BUSEN signal is enabled if a DMA is taking place or I/O ports 300H to 30FH are being accessed.

\[
\text{BUSEN} = \overline{\text{DACK1}} \& \overline{\text{DACK3}} \& \{\overline{\text{AEN}} \& \overline{\text{A9}} \& \overline{\text{A8}} \& \overline{\text{A7}} \& \overline{\text{A6}} \& \overline{\text{A5}} \& \overline{\text{A4}}\}.
\]

DREQ1 = \( \overline{\text{REQ0}} \& \overline{\text{DACK1}} \) \# \{ \overline{\text{REQ0}} \& \overline{\text{DREQ1}} \} \# \text{RESET}

DREQ3 = \( \overline{\text{REQ1}} \& \overline{\text{DACK3}} \) \# \{ \overline{\text{REQ1}} \& \overline{\text{DREQ3}} \} \# \text{RESET}

The DREQ1, DREQ3 signals are used insure that the request to the DMA controller is never deactivated before the acknowledge is received.