Chapter 6

DESIGN & ANALYSIS OF HIGH PERFORMANCE DIFFERENTIAL CAPACITANCE READ OUT CIRCUIT

6.1 Introduction

Navigational grade accelerometer requires stability and resolution of the order of micro g. In this chapter we attempt to describe the design of a high sensitive/performance differential capacitance pick-off circuit for the micromachined acceleration sensors. Efforts are made to take care of thermal noise, bias drift and thermal effects.

The circuit conventionally used for navigational grade traditional accelerometer is based on Blumlein Bridge which employs a center tapped transformer. This circuit will maintain accurate balanced symmetrical signals, which will not affect the sensor performance. The Blumlein Bridge circuit is immune to supply drift and temperature variation. It cannot be implemented in CMOS process. The present design discussed here is capable to meet the high resolution and stability requirement for navigational grade accelerometer and can be fabricated as CMOS ASIC.

From equation (3.18) the differential capacitance $C_2 - C_1$ is

$$\Delta C = \frac{2\varepsilon A x}{d_0^2 - x^2}$$  \hspace{1cm} (6.1)

where $x$ is the displacement of the proof mass from rest position and $d_0$ is the initial gap between the plates of capacitances $C_2$ and $C_1$, when there is no acceleration and $\varepsilon$ is the permittivity of the medium. Measuring $\Delta C$, displacement $x$ can be found by solving the above nonlinear equation.

6.2 Capacitive Sensor Interface

Capacitive transduction have many advantages. In most micro machining technologies, minimal additional processing is needed. It is having very good sensitivity and the transduction mechanism is insensitive to temperature. Parasitic stray capacitances present on the circuits is taken care in the design.
6.3 Capacitive position sense circuits

The purpose of the sense electronics is to detect and amplify the minute capacitance changes resulting from small displacement changes. A simple circuit for this purpose is shown in Fig 6.1. The sense capacitors C1 & C2 form a simple voltage divider and CP1 and CP2 represent the wiring parasitics. The sense output Vs is fed to a unity gain buffer to avoid the signal attenuation due to parasitic capacitance CP1.

![Capacitive position measurement circuit](image)

The voltage at the sense output

$$V_s = V_x \cdot \frac{2\Delta C}{2C_0 + CP1} \quad (6.2)$$

where $V_x$ & -$V_x$ are the in phase and out of phase excitation signal +/- 5V with a frequency ($f_{clk}$), $C_0$ is the capacitance value of C1 & C2 when there is no acceleration. CP1 represents wiring parasitic capacitance between the sense output with respect to accelerometer body, CP2 represents the capacitance between the output Vout and the sense output Vs. $\Delta C$ is the difference in capacitances between C1 & C2. The resistor $R_{dc}$ sets the potential at the node Vs to a value close to zero. The value of the $R_{dc}$ is chosen such that $i_{dc}$$<$input signal current. This translates $R_{dc} \gg \frac{1}{2\Pi C_0 f_{clk}}$

where $f_{clk}$ is frequency of the input excitation signal Vx. In this design $C_0$ is taken as 40 pf & $f_{clk}$ is chosen as 100 kHz.
Thermal noise from the buffer limits the minimum detectable capacitance.

For 1 microg resolution (ie 1.31 aF) and ±5 Volts $V_x$, $V_s$ will be 131 nV. Extreme care is taken in selecting the $R_d$ and the input buffer OpAmp to keep the noise sources below this value. Thermal noise from the buffer and the resistance $R_d$ limits the performance. By using the chopper stabilization method, the device operation frequency is moved from the flicker noise range to thermal noise range, thus enhancing the signal-to-noise ratio and improving the resolution of the circuit. Reversing the polarity of the excitation voltage $V_x$ at frequency $f_{clk}$ results in the amplitude $V_s$ being proportional to $\Delta C$. Typical chopping frequency 100 kHz is being used for the design. The signal is recovered by using phase sensitive demodulation method.

### 6.4 Circuit Design

The functional block diagram of the design is given in Fig 6.2 and the detailed circuit diagram is given in Fig 6.3 [26].

6. 2 Functional Block schematics of the circuit
Fig. 6. 3 Capacitive pick-off circuit
The first block is the capacitance to voltage converter and it converts the capacitance variation $\Delta C$ to voltage (eqn 6.2). The maximum $\Delta C$ considered is 30 pf. The maximum value of parasitic capacitances $C_3$ & $C_{P2}$ considered is 10 pf. The value of $R_{dc}$ should be higher than $\frac{1}{2\pi C_o f_{clk}}$. A lower value of $R_{dc}$ is preferable for the design, since the thermal noise of the resistor will affect the resolution of the capacitance sensing. By considering the value of $C_0$ as 40 pf and $f_{clk}$ of 100 kHz, the value $R_{dc}$ should be higher than 40 K ohms. $R_{dc}$ has been chosen as 100 k ohms. The frequency of $f_{clk}$ is chosen by considering the slew rate and the gain bandwidth product of the input buffer $U_1$ and the switching characteristics of the CMOS switches (CD TLC 4066) used for the demodulator. The reference clock amplitude has been selected as $\pm 5 \text{V}$ based on the input buffer supply voltage.

The input buffer $U1A$ & the phase sensitive demodulator differential amplifier $U2A$ in fig 6.3 have been selected based on the following parameters.

- Very low input voltage noise and current noise.
- High slew rate.
- Low input bias current.
- High gain bandwidth product.

By considering all the above points TLO 82 has been selected for the $U1A$ & $U2A$. TLO 82 is having very low current noise of 0.01 pA/Hz$^{1/2}$, voltage noise of 16 nV/Hz$^{1/2}$, input bias current of 50 pA, slewrate of 13V/µS and the gain bandwidth product of 4MHz.

The phase sensitive demodulator is based on the OpAmp TLO 82. The function of the demodulator is to convert the signal information from the chopping frequency 100 kHz. The filter has two functions, filter the 100 kHz excitation signal and to limit the amplifier response to 200 Hz. Simple RC single pole Butterworth filter has been designed. The final scaling amplifier has been designed to operate with a gain of 10.62 dB. The gain of the amplifier is decided, based on the output swing $\pm 4.5 \text{V}$ for a $\Delta C$ maximum of 30 pf. Proven industry standard low bias drift and bias drift stability, OpAmp OP 07 is selected. Apart from the characteristics of the device, model availability in the PSPICE is also considered for the device selection.
6.5 Circuit simulation

The circuit is shown in Fig 6.3. The supply voltage is limited to ±5 Volt, since most of the OpAmp & analog switches for the standard cell library for the CMOS processes is available for ±5V operation.

The input excitation signals V4 & V5 are generated in opposite phases (100 kHz ±5V). The R6 & C5 is used as a 200 Hz low pass filter for limiting the bandwidth. Using Microsim PSPICE, the circuit has been simulated.

6.6 Simulation Results

1. The final amplifier gain is 10.62 db for an output voltage limit of ±4.44 Volts for 30 pf delta C input.

2. The temperature has been varied from 25 deg C to 55 deg C. The output-offset temperature sensitivity is 1.41 micro volt /°C.

3. The output referred noise is 132 nV max for the entire 0-200 Hz bandwidth. This corresponds to equivalent of 0.89 aF (0.56 micro g), the circuit can resolve such a very low capacitance variation.

4. The sensitivity study on the excitation signal has been studied, for the 10 % frequency variation, the output variation of 8.7 mV is observed. The Excitation amplitude is also varied by 10 % and the change in output variation is 0.083%.

5. The maximum observed output bias voltage is 79 microvolts at 25 deg C. The same can be further adjusted by trimming the output amplifier offset.

6.7 Conclusion

The designed circuit can be implemented in CMOS technology and can be easily integrated into the silicon micromachined accelerometer which will minimize the stray capacitance and improve the noise figure.