CHAPTER 5

GENERALIZED SSHSM METHODS FOR HIGHER LEVEL INVERTERS

5.1 INTRODUCTION

This chapter presents generalized formulation of SSHSM techniques that are suitable for N-level inverter. All proposed modulations are extended to operate with higher level inverter and its performance is presented. Let N be the number of levels of the inverter and K be the number of converter cells, therefore, K= (N-1)/2. A generalized SSHSM controller consists of N-level MSPWM generation module, N-level base MSPWM circulation module and independent HMC for all inverter cells.

N-level MSPWM generation module is used to generate FFPWM, SSP and K number of MSPWM. SSP and FFPWM pulses are same for all inverter cells in each phase. MSPWM is based on the type of modulation and carrier signals used. The MSPWM modulation pulses for SSHSM methods are APOD, SCSM, CBSVM and PSC. The main advantage of MSPWM is easy to achieve relatively, and its complexity is almost no increase as the levels increasing. The generalized base PWM circulation schemes embedded with higher-level SSHSM modulations are for to maintain symmetrical loading of the inverter cells and help DC-link capacitor voltage balancing. The same effective switching action for each FBI in a phase leg is achieved with this scheme.

The proposed HMC for each inverter cell is applicable for any MSPWM technique and used for developing the SSHSM pulse generation.

The generalized formulation of a combinational logic that suits for each inverter cell given by

$$\begin{aligned} S_{u1} &= A\,B\,Z + \overline{A}\,B \\ S_{u2} &= \overline{A}\,B\,Z + \overline{A}\,\overline{B} \\ S_{u3} &= \overline{A}\,\overline{B}\,Z + A\,\overline{B} \\ S_{u4} &= \overline{A}\,B\,Z + A\,B \end{aligned} \tag{5.1}$$

where Z is MSPWM for K^{th} inverter cell. An independent HMC is used to combine a SSP, FFPWM and its corresponding MSPWM for developing SSHSM pulses in K^{th} inverter cell. Similarly, SSHSM pulses developed for all inverter modules of a CMI. Totally, 4K gate pulses per phase developed to operate N-level inverter.

In order to show the feasibility of the proposed modulations for higher-level inverter operation, the spectral analyses has been performed by using MATLAB/Simulink software and it is presented. The frequency of modulation and carrier waves are 50 Hz and 1500 Hz respectively and the inverter is operated in a linear modulation region with M=0.85. The load resistance and inductance are 10Ω and 15mH respectively, and the DC bus voltage is set at 200V. The proposed SSHSM techniques are theoretically analyzed for seven and nine-level inverters, then generalized for N-level inverter, and validated by simulation results.

5.2 GENERALIZED HYBRID ALTERNATE PHASE OPPOSITE DISPOSITION MODULATION

The scheme of N-level HAPOD technique is shown in Figure 5.1. In order to implement the HAPOD for N-level inverter, K numbers of base APOD pulses are needed. APOD pulses are generated by comparison of modulation signal with (N-1)/2 triangular carriers independently. The

modulation index for N-level APOD is given by $M=A_m/KA_c$. The amplitude of the modulation signal (A_m) is modified based on the inverter level, therefore A_m= (N-1) M A_c/2, where A_c is the amplitude of the carrier signal. The DC bias off-set difference between carriers is $2A_c$ and it is shown in Figure 5.1. The FFPWM and SSP pulses are same in each phase and it should be synchronized with phase reference signals.

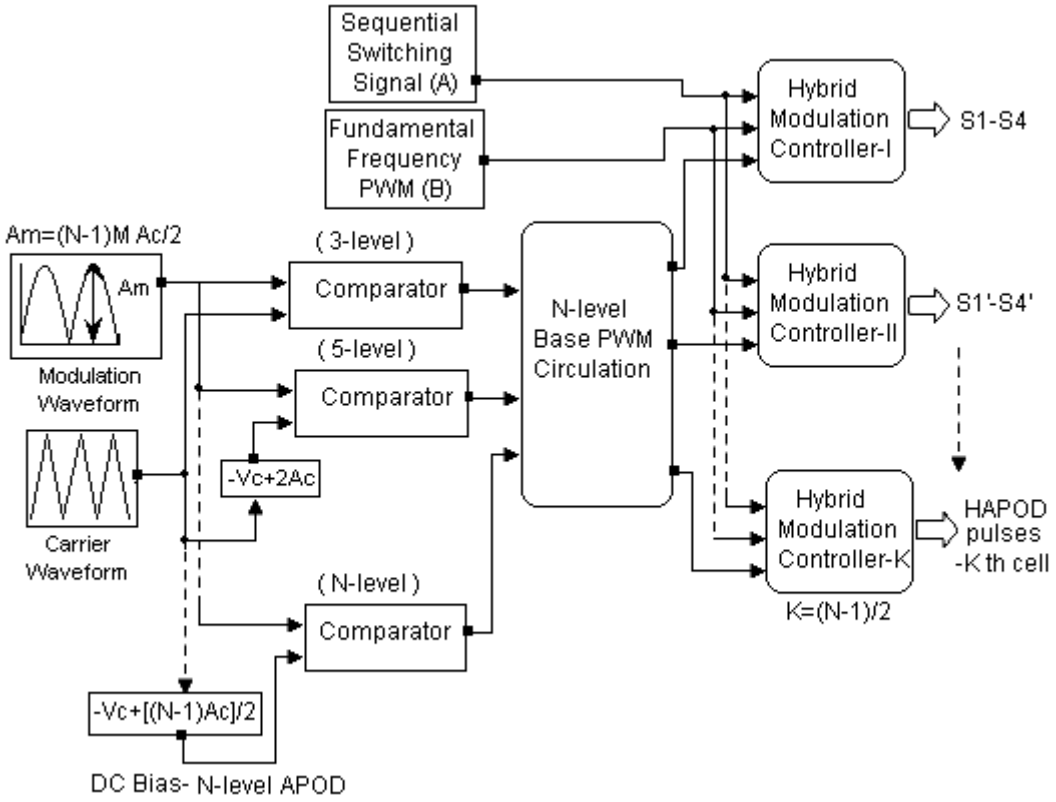
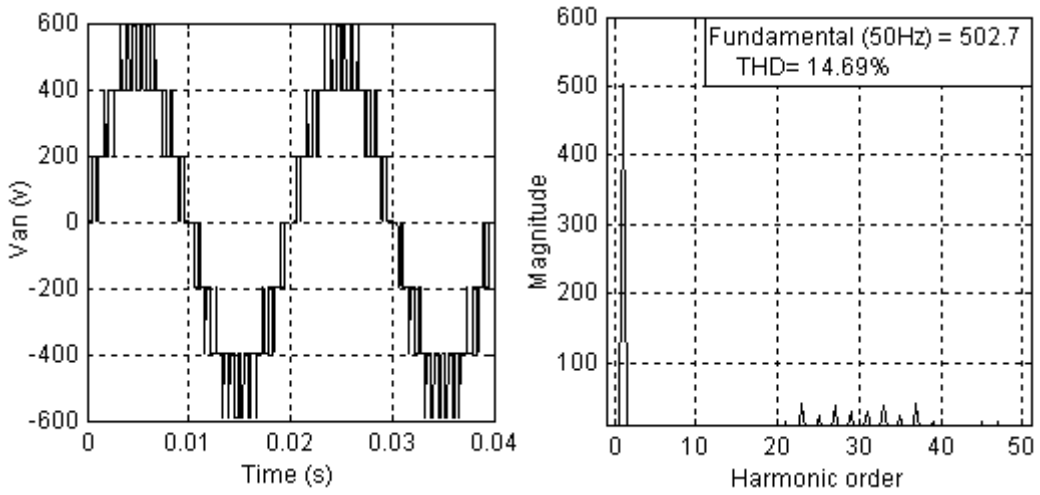


Figure 5.1 Scheme of N-level sequential switching HAPOD modulation

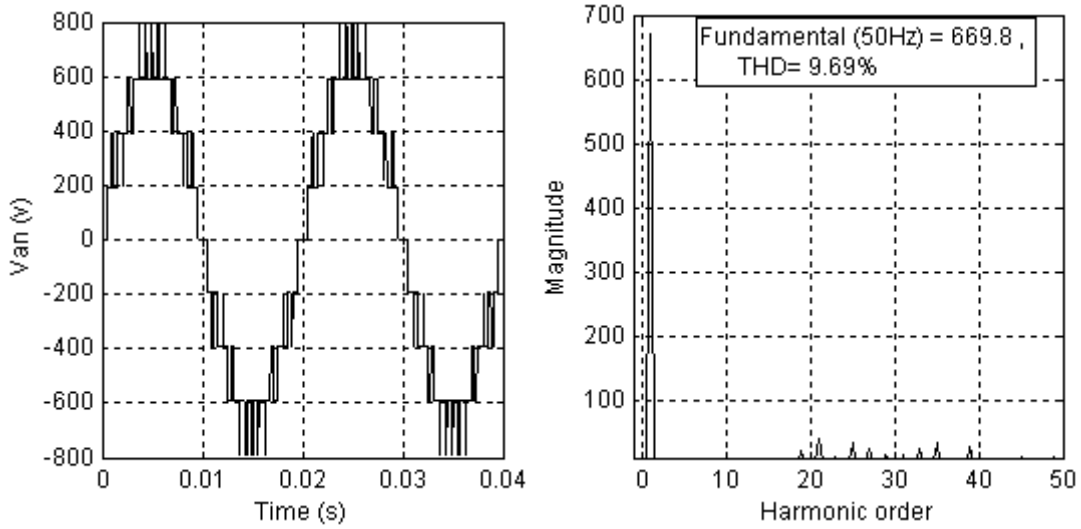
HMC for each inverter cell is used to combine FFPWM, SPP and its corresponding APOD pulses for developing sequential switching HAPOD pulses. The IGBT switches in each cell are operated with HAPOD; it is a combination of FFPWM and APOD pulses, so that it produces the resultant switching pattern which is same as APOD. Therefore, the inverter output is having APOD harmonic performance and considerable reduction of switching

loss due to reduced switching frequency is an advantage with this proposed modulation.



(a) (b)

Figure 5.2 Simulation results of seven-level HAPOD modulation: (a) Phase voltage waveform (b) Spectrum of phase voltage



(a) (b)

Figure 5.3 Simulation results of nine-level HAPOD modulation: (a) Phase voltage waveform (b) Spectrum of phase voltage

The seven-level output voltages can be clearly identified in linear modulation region as shown in Figure 5.2(a), a low harmonic distortion can be noted in Figure 5.2(b). Then, the nine-level HAPOD operation is performed; its output voltage waveform is shown in Figure 5.3(a). The THD is 14.69% for seven-level inverter, where as, it is reduced to 9.69% for nine-level operation. The side band harmonics are centered on 1.5 kHz; its harmonic amplitudes are reduced considerably for higher-level inverter operation.

5.3 GENERALIZED HYBRID SINGLE CARRIER SINUSODIAL MODULATION

The scheme of N-level HSCSM technique is shown in Figure 5.4. For N-level HSCSM, (N-1)/2 of SCSMs are developed as base modulation pulses. SCSM are defined by the comparison of unipolar modulation signals with single carrier. For N-level SCSM, K number of modulating signals are used with DC bias difference of each signal is –Ac. The amplitude of the modulation signal are A_m= (N-1) M A_c/2. SSP and FFPWM are same for all inverter cells in each phase leg; it should be synchronized with first modulation signal. N-level base PWM circulation module is used for SCSM circulation for every switching period to get resultant HSCSM circulation among the inverter modules. An independent HMC is used to combine a SSP, FFPWM and its corresponding SCSM for developing HSCSM pulses in K^{th} inverter cell.

The mathematical model of N-level SCSM is required for on-line digital implementation. It is derived from the point of intersection between single carrier and the sampled modulation signals. The modulation signals can be described as

$$S_1(t) = A_m \sin [\ \omega t\ + \frac{\pi}{P}] \qquad (5.2)$$

$$S_2(t) = A_m \sin [\ \omega t\ + \frac{\pi}{P}] - A_c \tag{5.3}$$

where angular frequency $\omega = \frac{2\pi}{P}$.

The straight-line equation for the carrier wave can be expressed as

$$C(t) = -2\ A_c\ f_c\ t + h\ A_c\ ,\ h=1,\ 2,\ 3\ldots \tag{5.4}$$

A generalized equation to generate the i^{th} SCSPWM pulses for any inverter level is given by

$$\alpha_u(i) = \frac{1}{2f_c}[(2i + u - 2) - \frac{A_m}{A_c}\sin(\omega\ (i-1) + \frac{\pi}{P})] \tag{5.5}$$

where i represent a position of each modulated pulses (i=1, 2, 3….P) and u=1, 2... K represents which inverter cell is being referred to.

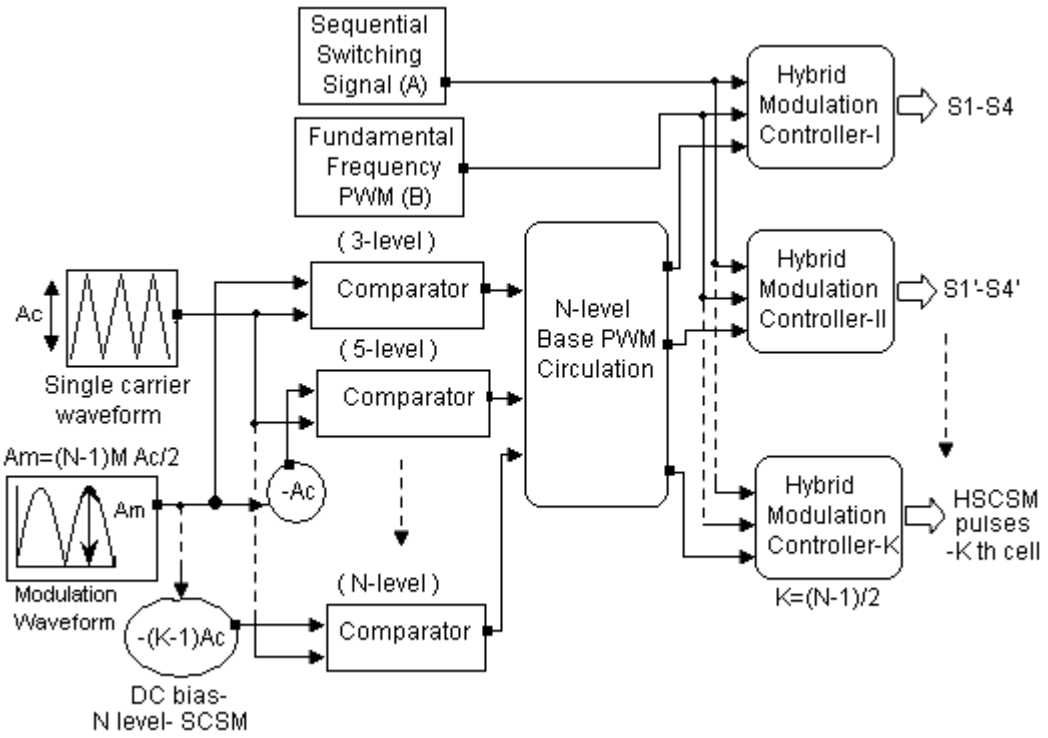
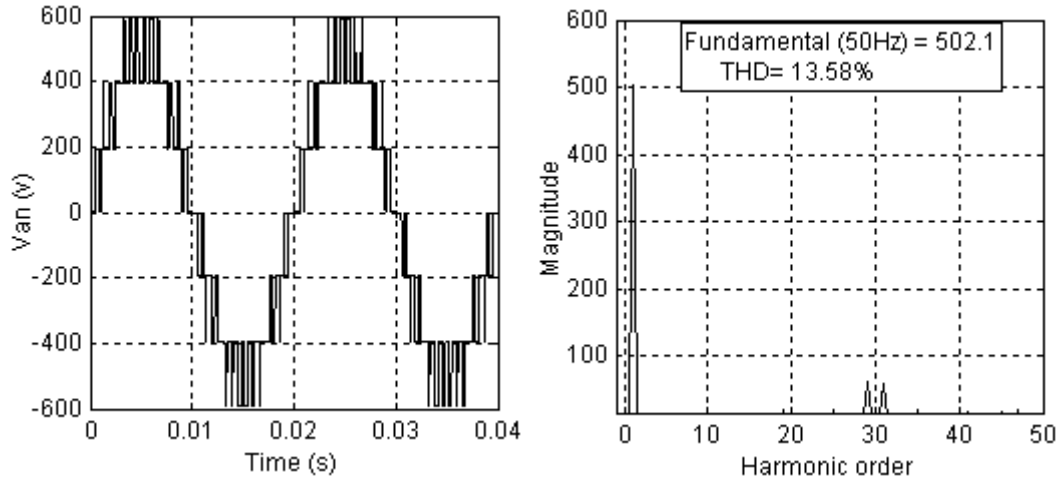
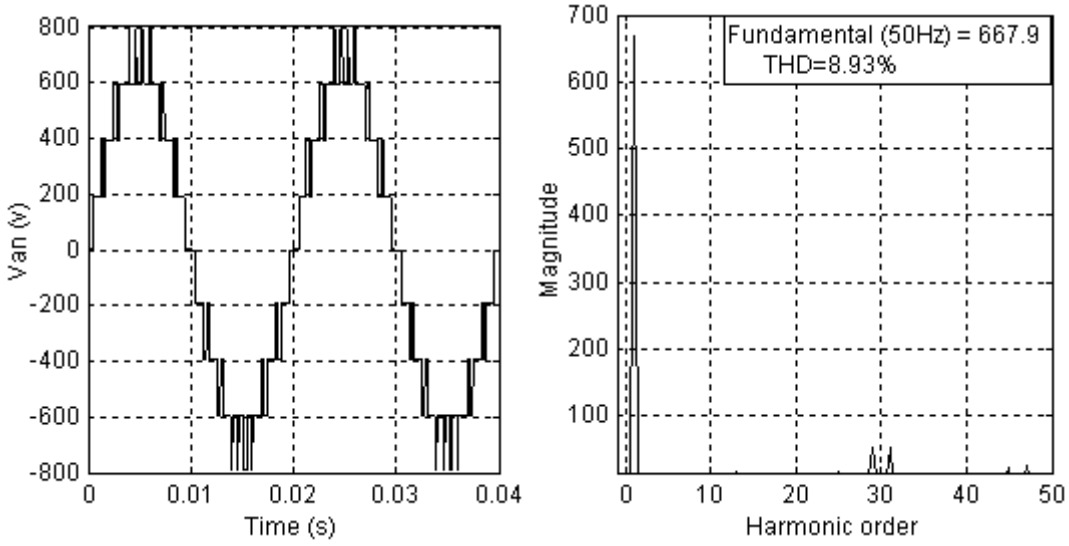


Figure 5.4 Scheme of N-level sequential switching HSCSM



(a) (b)

Figure 5.5 Simulation results of seven-level HSCSM: (a) Phase voltage waveform (b) Spectrum of phase voltage



(a) (b)

Figure 5.6 Simulation results of nine-level HSCSM: (a) phase voltage waveform (b) Spectrum of phase voltage

The switched voltage waveform with its harmonic spectrum for seven-level HSCSM is shown in Figure 5.5. It is noted that the fundamental voltage is pre-defined for seven and nine-level inverter operation. The

significant harmonics are 29, and 31, which are high frequency, with the RMS values under 6% of the fundamental term. In addition, the magnitudes of harmonics are getting down when the inverter level increases. The WTHD values for seven and nine-level operation are 1.19%, and 1.09% respectively. This inverter operates with odd frequency ratio; produces even side band harmonics and for even frequency ratio, produces odd side band harmonics. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all.

5.4 GENERALIZED HYBRID CARRIER BASED SPACE VECTOR MODULATION

The generalized formulation of HCBSVM needs the (N-1)/2 CBSVM pulses. The scheme of N-level HCBSVM technique is shown in Figure 5.7. N-level CBSVM, uses (N-1)/2 carrier waveforms of equal magnitude, frequency and phase, into contiguous bands that fully occupy the linear modulation range. Three phase modified reference waveforms are then superimposed over the carrier sets, and the intersection points determine the level that the phase leg must switch to. A simple base CBSVM scheme can be used for higher level HCBSVM generation. This technique does not involve any sector identification and reduces the computation time considerably, when compared to conventional SVM for higher order inverters.

To generalize the HCBSVM concept, the algorithm for an N-level inverter is as follows:

(i) Based on the inverter level, the number of HMC is defined as K=N-1/2.

(ii) Modify the peak amplitude of the phase reference voltages V_a, V_b, and V_c based on the modulation index (M). The

amplitude of the phase references (A_m) are modified based on the inverter level, therefore A_m= (N-1) M A_c/2, where A_c is the amplitude of the carrier signal.

(iii) Identify the instantaneous values of the three phase reference voltages V_a, V_b, V_c and determine the values of off-set voltages V_{off} and V_{off}'. The offset voltage computation is based on a modulus function depending on the DC-link voltage, number of levels and the phase voltage amplitudes. This modulo offset ensures that the middle two space vectors of the switching sequences are centered in each switching period. The offset voltages for multilevel operation can be defined as:

$$V_{off} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \tag{5.6}$$

$$V_k' = (V_k + V_{off} + V_{dc}) \bmod \left(\frac{2\,V_{dc}}{N-1}\right), \; k = a,b,c \tag{5.7}$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a', V_b', V_c') + \min(V_a', V_b', V_c')}{2} \tag{5.8}$$

(iv) The modified sinusoidal references are obtained by

$$V_k' = V_k + V_{off} + V_{off}' \tag{5.9}$$

(v) The modified sinusoidal modulating signals are compared with each PD carriers separately, to define the switching pulses of CBSVM. The DC bias off-set difference between carriers is A_c and it is shown in Figure 5.7. The carrier amplitudes are defined to designate the carrier regions in which reference phase voltages lie during the sampling interval under consideration.

(vi) A common SSP and FFPWM pulses for each phase should be used in synchronization with the phase references.

(vii) An independent HMC for each inverter cell is used to combine SSP, FFPWM and the corresponding CBSVM for HCBSVM generation.

(viii) Similarly, HCBSVM pulses are developed for all inverter modules for an N -level inverter.

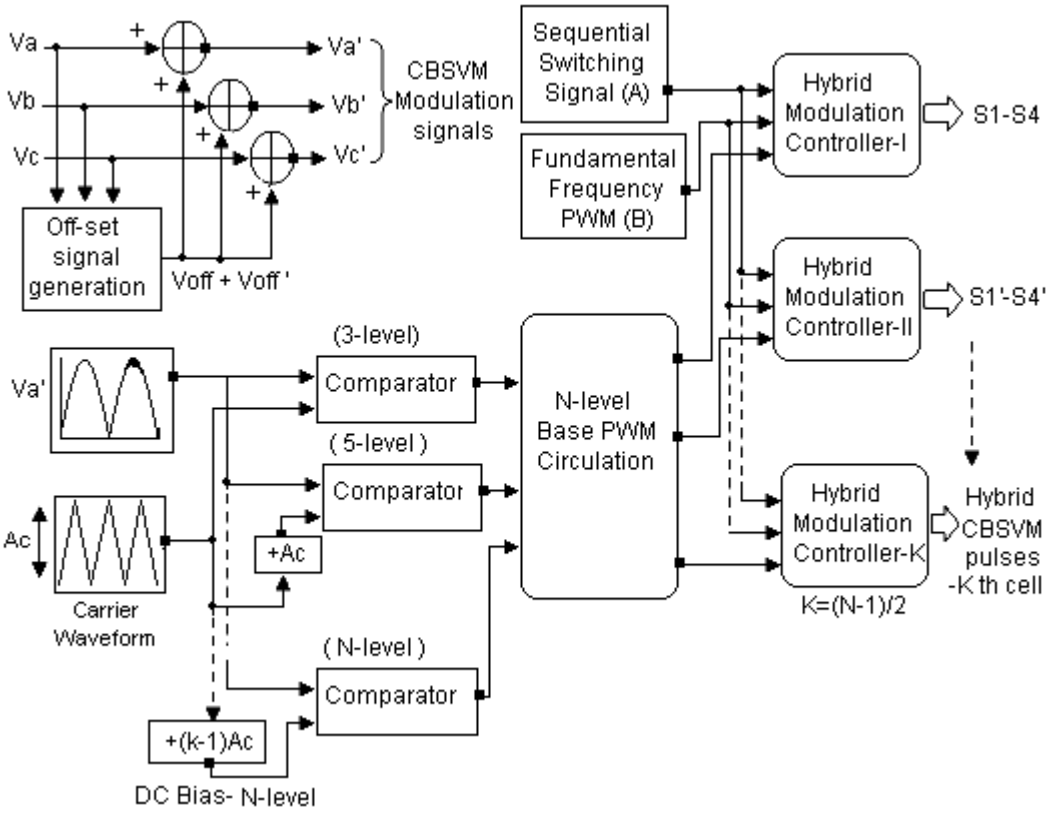
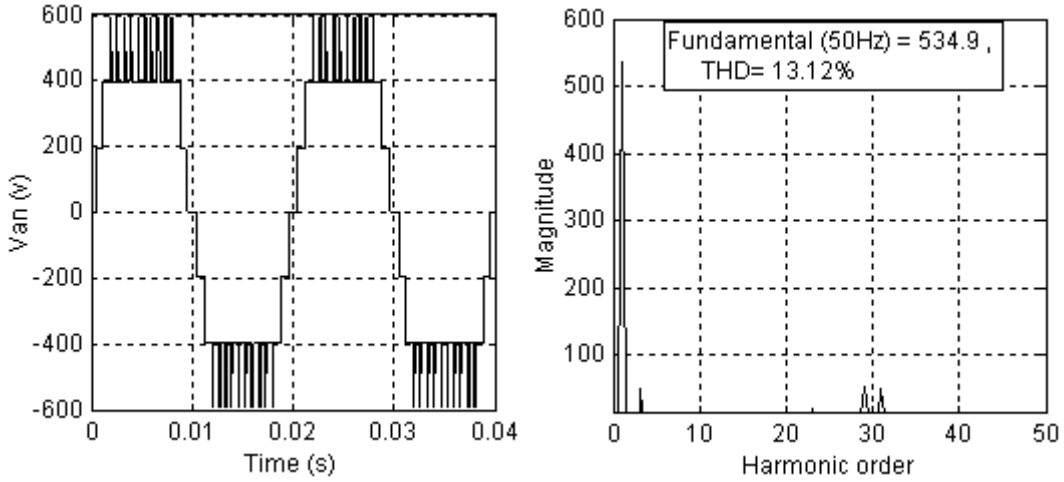


Figure 5.7 Scheme of N-level sequential switching HCBSVM

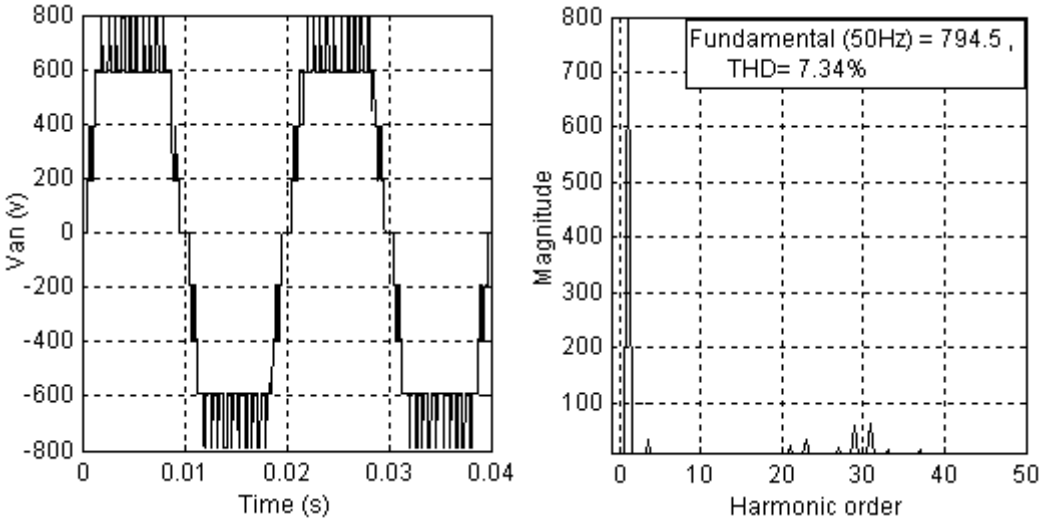
The phase voltage waveforms with its spectrum for seven-level HCBSVM operation are shown in Figure 5.8. The phase voltage WTHD is 1.12%, which is less than five-level operation, and no individual harmonic component has a magnitude greater than 6% of the fundamental. In HCBSVM modulation, only generates carrier sideband harmonics in the phase voltage,

the dominant harmonics are adjacent to carrier frequency. From the spectrum shown in Figure 5.8 (b), it is commented that some base band harmonics are due to adding offset values for CBSVM, which are cancelled in the line voltage.



(a) (b)

Figure 5.8 Simulation results of seven-level HCBSVM: (a) Phase voltage waveform (b) Spectrum of phase voltage.



(a) (b)

Figure 5.9 Simulation results of nine-level HCBSVM: (a) Phase voltage waveform (b) Spectrum of phase voltage

The nine-level HCBSVM operation is presented in Figure 5.9, this harmonic performance is better than the seven-level and the predefined fundamental voltage is obtained. This generalized HCBSVM algorithm is very simple, computationally efficient and has linear voltage transfer characteristics throughout the modulation range extending up to over-modulation mode.

5.5 GENERALIZED HYBRID PHASE SHIFTED CARRIER MODULATION

The formulation of N-level HPSC consists of N-level base PSC modulator and (N-1)/2 HMC. The principle of generalized HPSC modulation is illustrated in Figure 5.10. The N-level PSC technique consists of (N-1)/2 carriers with the frequency $f_c' = f_c/(N-1)$, where f_c is the switching frequency of the resulting PWM waveform. The carriers are phase shifted by $2\pi / (N-1)$ incrementally.

For N-level PSC modulation, K number of inverter cells in one phase with their carriers shifted by an angle of 360º/2K are compared with respect to the same reference signal in order to obtain 2K+1 level line to neutral output voltage. FFPWM and SSP pulses are same for all inverter cells in each phase. An independent HMC is used to combine a SSP, FFPWM and the corresponding PSC pulses to develop HPSC pulses for K^{th} converter cell.

Base PWM circulation can be omitted in this modulation because it has the feature of inherent balanced power distribution among the cells. Using HPSC, the harmonic spectrum of the inverter output voltage contains switching components at 2K times the frequency of the carrier, its integral multiples and the side bands shifted from these in the multiples of the fundamental frequency.

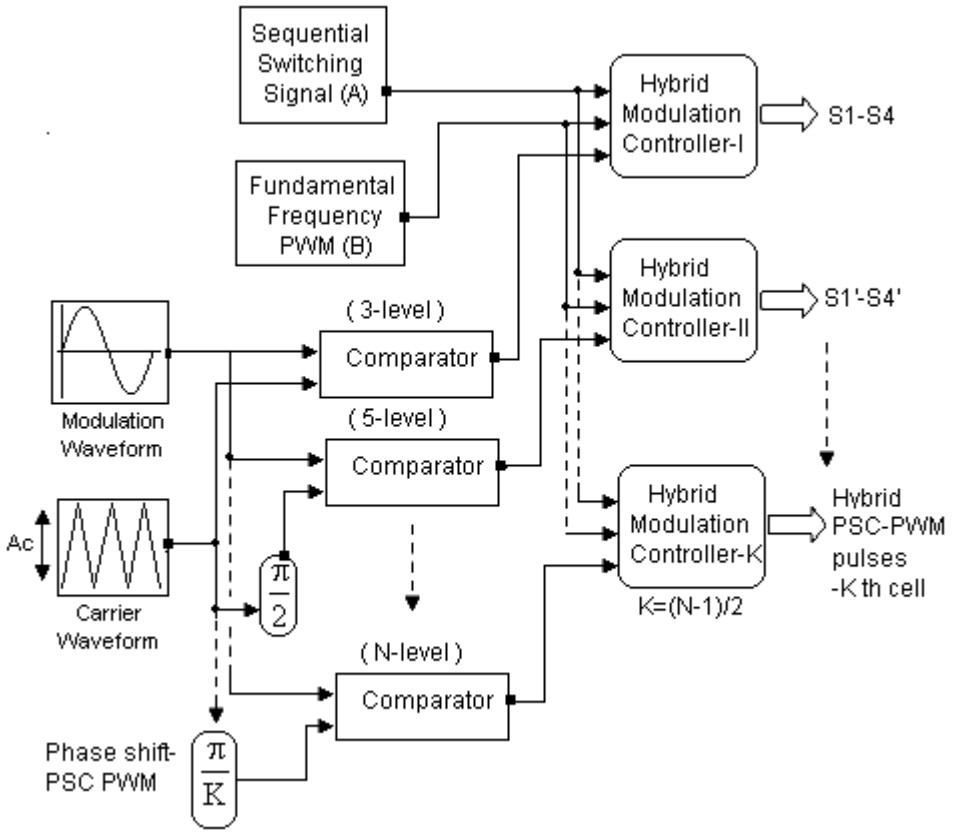
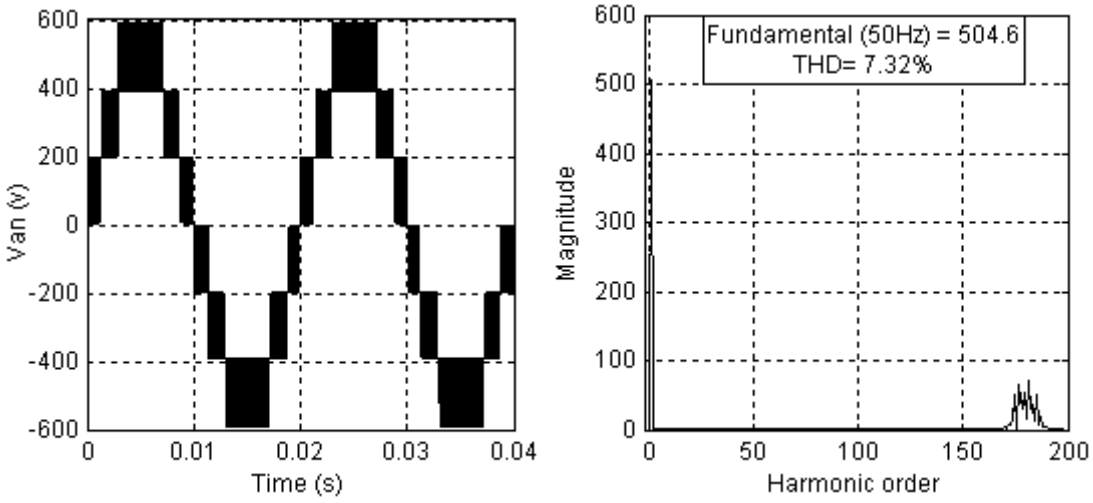


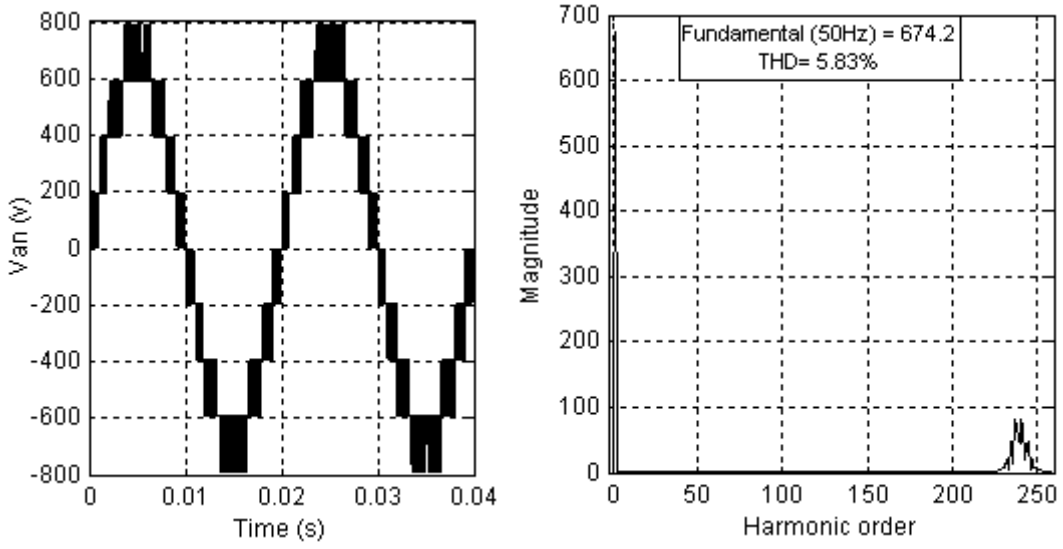
Figure 5.10 Scheme of N-level sequential switching HPSC modulation

The magnitude of switching harmonics in the PWM output is also proportionally reduced by a factor 1/2K. These two conditions considerably reduce the ripples in the switching function, and this allows the smooth modulation of the switching function for MI with a carrier signal of small amplitude. Figure 5.11 is the frequency spectrum of seven-level inverter output voltage, it is shown that the harmonics appear only as sidebands centered on the frequency of $6f_c$ and its multiples. Therefore, the output voltage has very high equivalent switching frequency, which simplifies the size of output filter. Also, it can be seen that the low frequency harmonics are simply absent. For nine-level HPSC operation, the output voltage and its spectrum are shown in Figure 5.12. In this spectrum, the side band harmonics are shifted to $8f_c$ and its WTHD is very low (0.22%).



(a) (b)

Figure 5.11 Simulation results of seven-level HPSC modulation (a) Phase voltage waveform (b) Spectrum of phase voltage



(a) (b)

Figure 5.12 Simulation results of nine-level HPSC modulation (a) Phase voltage waveform (b) Spectrum of phase voltage

5.6 COMPARATIVE PERFORMANCE ANALYSIS

To prove that the comparison levels joined in the new modulation strategies assure high efficiency of CMI, Figure 5.13 present the power loss reduction by the SSHSM modulation schemes at various inverter level operations. Power losses of the four SSHSM schemes reduce in turn. It appears that HPSC modulation is potentially attractive for high power applications because of their lower switching frequency. When the inverter level increases, number of commutations saved per cycle is reduced. Therefore, switching loss reduction is also decreased. Table 5.1 presents the harmonic measures of voltage waveforms with SSHSM methods in the higher level inverter operations. The harmonic factor valves are considerably reduced in nine-level inverter than seven-level operation.

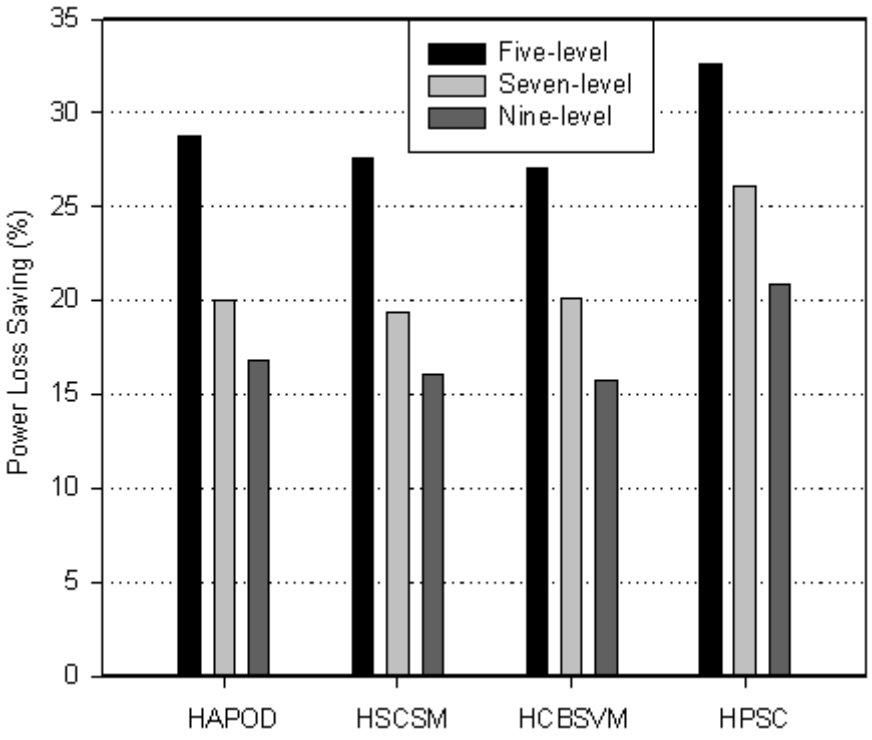


Figure 5.13 Power loss savings at higher level inverters with SSHSM schemes

Table 5.1 Harmonic performance of higher-level CMI with SSHSM schemes

PWM Type	Inverter level	THD (%)	WTHD (%)	WTHD0 (%)	Significant harmonics (harmonic order)	Magnitude of low order harmonics (% of fundamental)
HAPOD	Seven	14.69	1.26	1.13	23,27,29,31,33	4.08
	Nine	9.69	1.15	1.09	27, 29, 33, 35	2.89
HSCSM	Seven	13.58	1.19	1.08	29,31,35	6.81
	Nine	8.93	1.09	1.01	29,31,35	4.97
HCBSVM	Seven	13.12	1.12	1.02	23,27,31,33	5.06
	Nine	7.34	0.97	0.94	23,27,31,33	3.15
HPSC	Seven	7.01	0.26	0.21	173,181,189	2.16
	Nine	5.80	0.22	0.20	231,237,243	1.83

As a result, power loss reduction with superior harmonic performance is achieved with all proposed modulations, for seven-level and higher level CMI operation, which improves the performance of the converter.