CHAPTER 6

Fabrication & Characterization of Photonic Integrated Devices

Introduction
Materials for Optical Waveguides
Microfabrication Process Steps & Techniques for Photonic Integrated Devices
Fabrication of Directional Coupler, TMI Coupler and MMI Coupler
Characterization and Experimental Results
Conclusion
6.1. Introduction

The current chapter-6 deals with the fabrication processes steps and adopted techniques for realization of compact photonic integrated device components such as directional coupler (DC), two mode interference (TMI) coupler and multimode interference (MMI) coupler. In reference to the index of refraction, choice of material selection is a requisite necessity and this depends mainly on the function to be performed by the device. Although there are a number of candidate materials such as Ti: LiNbO₃ [1]-[3], GaAsInP/InP [4][5], SiON/SiO₂[6][7], GeO₂-SiO₂/SiO₂[8][9], SOI [10][11], polymer [12]-[14] etc. for development of compact photonic components; Silicon shows the property of opaque in the visible spectrum whereas transparent at the infrared wavelengths incorporates its application in optical transmission to guide light [7][15]. As discussed in chapter-2 and designed in previous chapters, for the fabrication of designed device components Silicon Oxynitride (SiOₓNᵧ) has been chosen as the core material surrounded by Silica (SiO₂) cladding layer for the following advantages [7][15]-[16]:

- SiOₓNᵧ is intrinsically compatible with the silicon processing technology.
- It shows a combination of chemical inertness, the low chemical permeability of silicon nitride and the excellent dielectric interface properties of silicon dioxide.
- The most important feature of this material is the variation of refractive index with changes in composition, or more precisely with the ratio of oxygen and nitrogen atoms. This feature enables one to tailor the refractive index and thereby customize the design of waveguides.
- Further, the luminescent properties of SiOₓNᵧ might lead to the future integration of electro optic devices with passive waveguides.

6.2. Fabrication Process and Techniques for Integrated Devices

Fig-6.1(a)-(c) shows the flow chart of adopted fabrication process steps and techniques which are discussed in detail along with process parameters in the
Subsequent sections.

**Fig-6.1(a):** Detail scheme for fabrication of channel waveguide structure
Fig-6.1(b): Detail scheme for fabrication of channel waveguide structure
Fig-6.1(c): Detail scheme for fabrication of channel waveguide structure

In this research effort the process of fabrication begins with the deposition of lower (cladding) layer of SiO$_2$, grown by high-pressure thermal oxidation- Dry-Wet-Dry Oxidization, and Plasma Enhanced Chemical Vapor Deposition (PECVD). The detail deposition process is discussed later in this chapter. The silicon oxynitride (SiON) film as a core layer is deposited using silane (SiH$_4$) and nitrous oxide (N$_2$O) precursor gases in the PECVD reactor which is also discussed in details later on. Previous works [17]-[21] have optimized low loss SiO$_x$N$_y$ films with index contrast ($\Delta n$) $<$5%-7% and above which the loss increases rapidly. Although the high index contrast materials based waveguide devices reduces device dimension, these material shows poor transmission properties in the high index range. Because of the high refractive index difference ($n=2$ for Si$_3$N$_4$, vs $n=1.45$ for SiO$_2$), the core layer need to be relatively thin to ensure single-mode operation. Thermal oxidation is performed using a quartz-tube electric furnace to heat Si wafers in a flowing oxygen atmosphere [20]-[22]. To grow a thick SiO$_2$ layer, the oxidation rate can be enhanced by using steam or steam-added oxygen atmospheres (Wet oxidation). The refractive index of
the SiO₂ layer exhibits slight dependence on the atmosphere. The thickness of the underlying oxide buffer layer must be large enough to ensure that the optical mode remains well confined in the core (Silicon Oxynitride) layers and does not leak into the high-index silicon substrate. Previous works on waveguides based geometry have been reported with propagation losses as low as 0.2 dB/cm [17]. The refractive index and the thickness of the films were measured using Ellipsometer and Profilometer. To understand the material behavior of deposited films, composition analysis are also carried out using high resolution FTIR spectroscopy. Table-3.2 shows the design parameters of DC, TMI coupler and MMI coupler as details are discussed in chapter-3. The designed DC, TMI coupler and MMI coupler with these waveguide parameters are then fabricated and experimentally tested using SiON as the waveguide core material with SiO₂ cladding layer. The detail each fabrication process steps and experimental results are discussed in the proceeding sections.

**Table-6.1: Design parameters of DC, TMI coupler and MMI coupler**

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Directional Coupler</th>
<th>MMI Coupler</th>
<th>TMI Coupler</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core waveguide width (a), μm</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Core waveguide Thickness (b), μm</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Index Contrast (Δn)</td>
<td>5%</td>
<td>5%</td>
<td>5%</td>
</tr>
<tr>
<td>Core RI (n₁), Δn=5%</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Cladding RI (n₂)</td>
<td>1.45</td>
<td>1.45</td>
<td>1.45</td>
</tr>
<tr>
<td>Coupling Gap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cladding RI (n₃)</td>
<td>1.45</td>
<td>1.4945</td>
<td>----</td>
</tr>
<tr>
<td>Coupling gap (h), μm</td>
<td>0.5</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>Wavelength (λ), μm</td>
<td>1.55</td>
<td>1.55</td>
<td>1.55</td>
</tr>
<tr>
<td>Beat Length (Lₑ), μm</td>
<td>91</td>
<td>80</td>
<td>45</td>
</tr>
</tbody>
</table>
6.2.1 Preparation of Wafer for Fabrication

Wafer specifications: Si wafer

Type: P-type
Orientation: <100>
Thickness: 525 ± 0.25 µm
Diameter: 100 mm
Resistivity: 1-15 ohms-cm
Surface: one side polished

Wafer Cleaning Process: The RCA clean is a standard set of wafer cleaning steps which need to be performed before high temp processing steps (such as oxidation, diffusion, CVD etc.) of silicon wafers in fabrication process. Werner Kern developed the basic procedure in 1965 while working for RCA, the Radio Corporation of America. It involves the following:

1. Removal of the organic contaminants (Organic Clean)
2. Removal of thin oxide layer (Oxide Strip)
3. Removal of ionic contamination (Ionic Clean)

The wafers are prepared by soaking them in DI water. The first step RCA-1 (also called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of NH₂OH (ammonium hydroxide) + H₂O₂ (hydrogen peroxide) + H₂O (water) at 75 or 80 ºC typically for 10 minutes. This treatment results in the formation of a thin silicon dioxide layer (about 10 Angstrom) on the silicon surface, along with a certain degree of metallic contamination (notably Iron) that shall be removed in subsequent steps. This is followed by transferring the wafers into a DI water bath.

The second step is a short immersion in a 1:50 solution of HF + H₂O at 25 ºC, in order to remove the thin oxide layer and some fraction of ionic contaminants.

The third and last step RCA-2 (also called SC-2) is performed with a 1:1:6 solutions of HCl + H₂O₂ + H₂O at 75 or 80 ºC. This treatment effectively removes
the remaining traces of metallic (ionic) contaminants. The details cleaning process steps approached are as follows:

The cleaning processes are carried out in the Chemical Wet bench as shown in Fig.-6.2.

**RCA (WET BENCH)**

![Fig-6.2. Chemical Wet Bench](image)

The RCA (Radio Corporation of America) is having 2 process steps as discussed above: **RCA-1 and RCA-2.**

**RCA-1:** (DI water: $\text{H}_2\text{O}_2$: $\text{NH}_4\text{OH}=5:1:1$)

- DI water =200 ml
- $\text{H}_2\text{O}_2$ = 40 ml
- $\text{NH}_4\text{OH}$ =40 ml

In case, if we don’t have Ammonium Hydroxide, we can also use ammonium solution.

- Temperature of the solution = 75-80° C
- RCA-1 function: Remove Organic residues
• Quartz beaker is mandatory.
• Magnetic stirrer: rotate uniformly and mix the solution and also maintain the temperature 75-80° C.
• Wafer holder: used to hold the wafer.
• Exhaust to be on, while performing RCA Cleaning.

Fig-6.3: RCA-1 Cleaning Process

RCA-1 Cleaning Procedure:
RCA-1 cleaning removes the surface contaminants like dust, grease etc. The process steps are:

Step-1: Take 200 ml DI water into quartz beaker then add 40 ml H₂O₂ and 40 ml NH₃OH to DI water. Once the solution is prepared, keep it on a hot plate and set temperature to 250° C. The temperature of the solution is maintained at 75- 80° C.

Step 2: A magnetic Stirrer put in the solution so that it uniformly rotate and mix the solution.

Step-3: Once solution gets heated up to 80° C, load silicon wafer into wafer holder and immerse into heated RAC-1 solution for 10 minutes. After 10 minutes of
cleaning take out wafers from the solution and rinse with DI water thoroughly for 1 minute, so that it can be cool down.

**Step-4:** After doing RCA-1, all beakers should be washed with DI water. Acid waste and DI water to be disposed in drain.

**RCA-2:** (DI water: H₂O₂: HCL=6:1:1)
- DI =240 ml
- H₂O₂ = 40 ml
- HCL =40 ml

- Temperature of the solution = 75-80° C
- RCA-2 function : Remove metallic residues
- Quartz beaker is mandatory.
- Magnetic stirrer: rotate uniformly and mix the solution and also maintain the temperature 75-80° C.
- Wafer holder: used to hold the wafers.
- Exhaust to be on, while performing RCA Cleaning.

![Fig-6.4: RCA-2 Cleaning Process](image_url)
RCA-2 Cleaning Procedure:

The RCA-2 cleaning removes the metallic contaminants from the wafer. The cleaning process steps are:

**Step-1:** Take 240 ml DI water into quartz beaker. Add 40 ml $\text{H}_2\text{O}_2$ and 40 ml HCl to DI water. Once the solution is prepared, keep it on a hot plate and set temperature to 250° C. The solution will be needed to be heated 75- 80° C.

**Step-2:** Magnetic Stirrer put in the solution so that it uniformly rotates and mix the solution.

**Step-3:** Once solution gets heated up to 80° C, load silicon wafer into wafer holder and immerse into heated RAC-2 solution for 10 minutes. After 10 minutes of cleaning take out wafers from the solution and rinse with DI water thoroughly for 1 minute, so that it can be cool down.

**Step-4:** After doing RCA-2, all beakers should be washed with DI water. Acid waste and DI water to be disposed in drain.

After RCA-1 and RCA-2 cleaning process, next process step is:

**HF (hydrofluoric acid solution) DIP:** (DI water: HF=10:1)

DI water = 100 ml
HF= 1 ml

- This process takes about 5 to 7 minutes to complete.
- Never use a glass beaker with HF since HF attacks glass, always use plastic beaker.

**Procedure:**

Take 100 ml of DI water using measuring cylinder and pour into polypropylene beaker and then 1 ml of HF in a polypropylene measuring cylinder and add to DI water and mix thoroughly using Teflon rod. Then dip RCA-2 cleaned silicon wafer
into dilute HF solution for 15 seconds and finally rinse with DI water for 1 min. Next, wafers should be blow dry with Nitrogen and store in a wafer box.

Fig-6.5: (a) HF solution dipped Wafer  
Fig-6.5(b): Blow dry with Nitrogen

Now the wafers are ready for thermal wet oxidation process.

6.2.2 Deposition of Silica (SiO₂) Layer as Lower Cladding

In thermal oxidation, silicon wafers are oxidized in furnaces at about 1000° C. The furnaces consist of a quartz tube in which the wafers are placed on a carrier made of quartz glass. For heating there are several heating zones and for chemical supply multiple pipes. Quartz glass has a very high melting point (above 1500° C) and thus is applicable for high temperature processes. To avoid cracks or warping, the quartz tube is heated slowly (e.g. +10° C per minute). The tempering of the tube can be done very accurate via individual heating zones. Depending on the gases different oxidations occur (a thermal oxidation has to take place on a bare silicon surface). Fig-6.7 shows the schematic diagram of Wet Oxidation Furnace/Tempress Furnace used for dry-wet-dry oxidation.
The thermal oxidation can be divided into the dry and wet oxidation:

The dry oxidation takes place under pure oxygen atmosphere. The silicon and oxide reacts to form silicon dioxide (SiO₂):

$Si + O_2 \rightarrow SiO_2$

In wet thermal oxidation, the oxygen is led through a bubbler vessel filled with heated water (about $\sim$95°C), so that in addition to oxygen water is present in the quartz tube as steam. The oxidation is given by:

$Si + 2H_2O \rightarrow SiO_2 + 2H_2$

This process is done by $90^0$ C to $1000^0$ C. The characteristics of wet thermal oxidation are:

i. Fast growth rate even on low temperatures

ii. Less quality than dry oxides

This dry process is done at 1000 to $1200^0$ C actually. To create a very thin and stable oxide the process can be done at even lower temperatures of about $800^0$ C. Characteristic of the dry oxidation:

i. Slow growth of oxide

ii. High density

iii. High breakdown voltage
In the beginning, the oxygen and silicon react to form silicon dioxide. Now the oxide layer at the surface has to be surpassed by other oxygen atoms which have to diffuse through the dioxide layer to react with the silicon crystal beneath. For this reason the growth rate primarily depends on the reaction time of oxygen and silicon, while at a certain thickness the oxidation rate is mainly determined by the velocity of diffusion of the oxygen through the silicon dioxide. With increasing thickness of the dioxide the growth rate decreases. Since the layer is amorphous, not all bonds in the silicon dioxide are intact. Partial there are dangling bonds (free electrons and holes) at the interface of silicon and SiO₂, and therefore there is a slightly positively charged zone at the interface. Since these charges affect the integrated circuit in a negative manner, therefore in general these charges are reduced with a higher temperature during oxidation or by using the wet oxidation which causes only a light charge.

**Details Oxidation Procedure:**

**A. Growth of SiO₂ of 1 μm thickness: Dry-Wet-Dry**

Material: SiO₂

Thickness: 2-3 μm (for >1 μm PECVD is preferred)

At the first, switch-on the mains of thermal wet oxidation furnace to grow 1 μm oxide layer on the top of the cleaned silicon wafer. Through Digital temperature controller the furnace is ramp up and executes the temperature.
1. Display mode
2. Program mode
3. Execute mode

**Fig-6.8: Digital temperature controller**

Thermal oxidation is carried out for growing SiO$_2$ layer on the cleaned Si surfaces. SiO$_2$ layer of thickness~1 µm is grown in the first step of oxidation using dry-wet- dry oxidation sequence.

The steps for thermal oxidation are as follows.

**Step-A:** Set the oxidation furnace temperature to $1100^\circ$ C and purge the furnace with pure N$_2$ gas.

**N$_2$ Flow rate** - 1 liter/min for 15 min.

**Step-B:** Load wafers in oxidation furnace in a N$_2$ ambient (N$_2$ is used only during loading and unloading of wafers in oxidation furnace).

**Step-C: Carry out dry oxidation for 10 min.**

Drive the O$_2$ into the furnace. Dry oxidation is to get the uniform layer of thickness and good interface between Si and Oxide.

**O$_2$ Flow rate** - 1 liter/min.
Fig-6.9: (i) Oxidation Furnace, (ii) Front view of the furnace chamber (iii) Back view along with bubbler and gas (Installed at CeNSE, IISc.)

Step-D: Carry out Wet oxidation for 3 hours.

Heat the water up to 97° C and connect to the furnace. Pass the O₂ through bubbler. The oxygen carries water vapours along with it to the wafer surface enabling wet oxidation to take place.

Fig.-6.10: Bubbler

Step-E: Carry out dry oxidation for 10 min.

Hence a 1 μm of SiO₂ is grown by the above process. At the end of this duration, the ambient gas is again switched to N₂ and wafers are unloaded.
Colour of 1 μm oxide - green violet.
The dry-wet-dry sequence used in the process helps achieve a good quality Si-SiO₂ interface (enabled by dry oxidation) and at the same time a faster oxidation rate is achieved (due to wet oxidation).

**Note:** Initially 25-35 min will take to set the furnace temperature 1100° C and water heater to 97° C.

**Timings:**
- Loading of wafers: 1: 10 p.m
- Dry oxidation: 1:20 p.m to 1:30 p.m
- Wet Oxidation: 1:30 p.m to 5:10 p.m
- Dry Oxidation: 5:10 p.m to 5:20 p.m
- Unloading of wafers: 5:40 p.m

**Thickness Measurement of Deposited SiO₂ Layer:**
The thickness of the growth SiO₂ layer on the top of a Si-wafer by using
thermal oxidation technique is measured with the help of Ellipsometer Thickness Measurement System (Model: XLS100 from J.A. Woollam Co. Inc). Fig-6.12(a) shows the photograph of the system whereas Fig.-6.12(b) shows the schematic diagram. The measured result indicating the thickness of deposited SiO₂ lower cladding layer of ~1 μm (10455.19 Å) is shown in Fig.-6.13.

Further on the top of thermally grown SiO₂ layer of thickness ~1 μm, another layer of SiO₂ of thickness ~2 μm is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique.

Fig.-6.12(a): Ellipsometer Measurement System (Model: XLS100) (Installed at CeNSE, IISc., Bangalore)

Fig.-6.12(b): Schematic of Ellipsometer
Fig. 6.13: Measured thickness of SiO₂ layer ~1 μm deposited using thermal oxidation
B. Deposition of Silica (SiO₂) Layer using PECVD Method

The basic reaction for the formation of the silica (SiO₂) using SiH₄ and N₂O precursor gases in PECVD is as follows:

\[
\text{SiH}_4 \ (\text{gas}) + 4 \text{ N}_2\text{O} = \text{SiO}_2 \ (\text{solid}) + 2 \text{ H}_2\text{O} \ (\text{gas}) + 4 \text{ N}_2 \ (\text{gas})
\]

![PECVD system (Oxford PlasmaLabSystem100)](image)

**Fig-6.14: PECVD system (Oxford PlasmaLabSystem100)**

(Installed at CeNSE, IISc.)

Fig-6.14 shows the schematic view of the PECVD system (PlasmaLabSystem100) from Oxford Instrument System which is used for deposition of SiO₂ lower cladding layer of thickness ~2 μm with the following process parameters.

**Process parameters used:**

- RF power @ 13.56 MHz : 20 W
- Pump pressure : 1000 mTorr
- Silane (SiH₄) flow rate : 8.5 sccm
- N₂O flow rate : 710 sccm
N\textsubscript{2} flow rate  : 161 sccm  
Substrate temperature : 350\textdegree{}C  
Deposition rate : 1 \mu m/25 min  

The details of PECVD system is discussed in the proceeding section-6.2.3. The thickness and refractive index of the deposited SiO\textsubscript{2} layer is measured using ellipsometer. Fig.-6.15 shows the process parameters of SiO\textsubscript{2} deposition using PECVD system whereas the measured thickness of SiO\textsubscript{2} layer (~3 \mu m) is shown in Fig.-6.16.

\textbf{Fig-6.15:} Process parameters for deposition of SiO\textsubscript{2} layer using PECVD
Fig.-6.16: Measured thickness of SiO$_2$ layer ~2 μm deposited using PECVD
6.2.3 Deposition of Silicon Oxynitride (SiON) as Guiding Layer

Material : SiON  
Thickness : 1.5 μm

Among the variety of techniques available for silicon oxynitride production, plasma enhanced chemical vapour deposition (PECVD) technique is one of the most widely utilized due to the relative high deposition rates and low deposition temperatures [6][7]. On the other hand, for optical applications, besides the tunability of the refractive index of the materials involved, thick films (3–5 μm) with lower internal stress are essential. Plasma Enhanced Chemical Vapor Deposition (PECVD) for silicon oxynitride (SiON) layers results in a flexible material for optical waveguides. Deposition of silicon oxide and oxynitride by PECVD is identified as quite attractive technology for development of compact optical devices as films fabricated by this process easily matches the refractive index profile by changing the process parameters. In the PECVD process, the precursors used and the deposition parameters strongly influence the optical properties and quality of the deposited films. For the most part of PECVD processes for waveguide fabrication, nitrous oxide (N₂O) and silane (SiH₄) are used as main precursors for fabrication of pure silica. The basic reaction for the formation of SiON is given below,

\[
\text{SiH}_4 + \text{N}_2\text{O} + \text{NH}_3 \rightarrow \text{SiO}_x\text{N}_y\text{H}_z \text{ (solid)} + \text{H}_2\text{O (gas)} + \text{N}_2 \text{ (gas)} \\
\quad \rightarrow \text{SiO}_x\text{N}_y \text{ (solid)} + \text{H}_2\text{O (gas)} + \text{HCl (gas)} \text{ (after annealing)}
\]
Process Parameters used:

- Si-Substrate temperature: $350^\circ$ C
- RF power @ 13.56MHz: 20 W
- Pressure: 1000 mTorr
- SiH$_4$ flow rate: 10 sccm
- NH$_3$ flow rate: 10 sccm
- N$_2$O flow rate: 200 sccm
- N$_2$ flow rate: 500 sccm
- Deposition rate: 1 $\mu$m/20 min

Fig.-6.17: PECVD technology (courtesy: Oxford Instrument System)

The silicon oxynitride films are deposited by using plasma enhanced chemical vapor deposition (PECVD) system (PlasmaLabSystem100) of Oxford Instruments System as shown in Fig-6.14 and Fig-6.17. The precursor gases are fed through a shower head which evenly distributes the gas mixture over the substrate holder; exhaust gases are pumped out from the bottom of the reactor. The plasma is created
between the shower head and the substrate holder and hence the substrate is in direct contact with the plasma. This system can be operated at two different frequencies: 13.56 MHz and 100 kHz. The system can be programmed to switch back and forth between the two frequencies automatically during a deposition run. Fig.-6.18 shows the process parameters with precursor gases used for SiON deposition by PECVD whereas the measured thickness of SiON layer obtained by using Ellipsometer is shown in Fig.-6.19. The refractive index and thickness of the deposited films were measured using a Model 2010 prism coupler from Metricon Corporation and Ellipsometer respectively. It uses a 632.8 nm He-Ne laser with a rutile prism to couple the beam into the film. All the measurements were done at TE polarization mode using a single film on substrate algorithm.

**Fig-6.18:** Process parameters for deposition of SiON layer using PECVD
Fig. 6.19: Measured thickness of SiON layer ~1.5 μm deposited using PECVD
Fig.-6.20: Refractive index variation of SiON films as a function of N$_2$O and NH$_3$

It is seen that different factors such as flow rates of gases, pressure, power, temperature etc. affect both the deposition rates and refractive index of the deposited SiON films. Fig.-6.20 shows the refractive index relation with the N$_2$O gas flow rates for 3 different NH$_3$ gas flow levels. The refractive index of deposited SiON films can be modified successively between 1.55 and 1.495, which is the range of interest for waveguide application. Higher refractive indices up to 1.912 are probable by exploiting a lower N$_2$O/SiH$_4$ ratio or using a greater NH$_3$ flow rate. But high refractive index is not suitable to waveguide application. A common tendency discovered is that the refractive index decreases when flow rate of N$_2$O increases owing to nitrogen's weaker chemical reactivity compared to oxygen [19]-[20]. This occurs because oxygen atoms are more reactive than nitrogen atoms and large amount of oxygen with small amount of nitrogen will be incorporated into the silicon oxynitride film, resulting in refractive index closer to that of stoichiometric SiO$_2$. At lower N$_2$O flow rate and in the absence of ammonia, a large index film was produced because of the higher silicon abundance (silicon rich films). Besides, as the flow rate
of ammonia gas was increased, the refractive index was enhanced due to the increase in nitrogen as well as hydrogen contents.

6.2.4 Preparation of Mask

The LaserWriter System is a useful tool for transfer of designed patterns on a Cr mask plate or directly on the substrate. The system transforms a laser beam into a controlled writing tool for photolithographic mask fabrication or for direct in-situ processing on planar substrates.

![LaserWriter System](image)

**Fig.-6.21**: Microtech LW 405A Laser Writer used for Mask Preparation
(Installed at CeNSE, IISc.)

The Laser Writer [Model: Microtech LW 405A] is used for preparation of 4 inch Cr-Mask plate. The mask layout of the design patterns is prepared using L-Edit software and optiBPM software before writing to the mask plate. The LaserWriter is driven by a MICROTECH proprietary data format - LDF, LaserDraw Format -obtained by
automatic translation from a number of industry standard languages accepted by the LaserWriter, such as CIF, DXF, and GDSII. Fig-6.22 shows the photograph of prepared mask.

**Fig.-6.22:** Patterned Mask for Photolithography

### 6.2.5 Annealing

The PECVD deposited SiON layer contains certain amount of O-H bonds, N-H bonds, and Si-H bonds that are known to be main cause of optical absorption at 1.38 μm, 1.48 μm and 1.51 μm respectively. In order to eliminate these bonds, the deposited SiON layer has been annealed at 800°-1000° C for 3 hrs with N₂ ambient using the First Nano drive-in furnace. For higher annealing temperatures (>1000° C), a large number of cracks occurred in the deposited SiON film. Fig-6.23 shows the First Nano’s EasyTube® 6000 Horizontal Furnace System installed at CeNSE, IISc., Bangalore. The FTIR spectroscopy of SiON deposited film after annealing and
before annealing is carried out which is shown in Fig.-6.24. This FTIR spectroscopy is carried out at SAIF, Tezpur University.

**Fig.-6.23:** First Nano Drive-in Furnace (Installed at CeNSE, IISc.)

![FTIR analysis of SiON layer](image)

**Fig.-6.24:** FTIR analysis of SiON layer (1: Si-O-H, 2: -Si-H, 3: -N-H_2 and 4: Si-O-H, -Si-H bonds)

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6.2.6 Transfer of Pattern on Guiding Layer

After cleaning the mask plate (prepared using Laser Writer as discussed in section-6.2.4) using acetone and IPA, the standard photolithography is performed for the transfer of designed patterns on the top of SiON core layer using EVG 620 double sided mask aligner set-up. The details process steps are discussed as follows:

6.2.6.1 Spin Coating of Photoresist

Process Parameters:

Positive photoresist (PR) : AZ315B
Developer : MF26A
Thickness of photo resist : 1-1.2 μm (4000 RPM)
Exposure : 85 mJ/cm²
Standard NUV : 350-450 nm
Lamp power : 350 W-500 W

The positive photoresist (AZ315B) is coated on sample with spinner coater at 4000 rpm for 40 second. An exposure with UV light is given for 1.5 sec, after pre-baking of sample at 125°C for 1 min. The photoresist (PR) is developed in developer for 60 sec and then the sample is kept in oven for post baking at 125°C for 1 min in order to make further hardening of the exposed portion of photoresist.

![Image](image.png)

**Fig-6.25:** Photoresist on the sample (a) before spinning (b) after spinning
6.2.6.2 Photolithography

Photolithography is the standard process to transfer a pattern that has been designed with computer-aided-engineering (CAE) software packages, on to a certain material (mask plate). The process steps involved in photolithography are resist coating, exposure, development, lift-off and etching etc. In the photolithographic process, a photoresist layer is spin-coated on to the material to be patterned. Next, the photoresist layer is exposed to ultraviolet (UV) light through the mask. This step is done in a mask aligner, in which mask and wafer are aligned with each other before the subsequent exposure step is performed. A mask with the desired pattern is created which is a glass plate with a patterned opaque layer (typically chromium) on the surface. Resist is coated on the waveguide substrate by a spinner. It is essential that the resist film coating is thin and as uniform and as free of pinholes as possible. The baking of the resist films has been done in an oven after coating to vaporize the solvent completely and to enhance adhesion to the substrate. Depending on the mask aligner generation, mask and substrate are brought in contact or close proximity (contact and proximity printing) or the image of the mask is projected (projection printing) on to the photoresist-coated substrate. Fig-6.27 shows the photograph of EVG Mask Alligner Photolithography Set-up installed at CeNSE, IISc., which is used for transfer of patterns to sample.
Fig-6.27: EVG 620 Mask Aligner Photolithography Set-up (CeNSE, IISc.)

Fig.-6.28 shows the basic steps of photolithography (positive) whereas the basic differences of positive and negative photolithography are shown in Fig.-6.29.

**A. Exposure**

- UV Radiation
- Mask
- Photoresist
- SiON
- SiO₂
- Si Wafer

**B. Development**

- Photoresist
- SiON
- SiO₂
- Si Wafer

**C. After development**

- Photoresist
- SiON
- SiO₂
- Si Wafer

Fig.-6.28: Photolithography steps
Depending on whether positive or negative photoresist was used, the exposed or the unexposed photoresist areas, respectively, are removed during the resist development process. The remaining photoresist acts as a protective mask during the subsequent etching process, which transfers the pattern onto the underlying material. Alternatively, the patterned photoresist can be used as a mask for a subsequent ion implantation. After the etching or ion implantation step, the remaining photoresist is removed, and the next layer can be deposited and patterned.

**Fig.-6.29(a):** Positive Photolithography

**Fig.-6.29(b):** Positive Photolithography (www.me.ccny.cuny.edu)
6.2.6.2.1 Mask Cleaning

The mask pattern made on the chromium (Cr) plate is cleaned using piranha solution (a mixer of H₂O₂ + H₂SO₄) before used in mask aligner system.

6.2.6.2.2 Alignment and Exposure

Before giving the exposure to the sample, proper alignment should be taken care off for the well matching of the alignment marks at the mask plate. The mask pattern was aligned upon wafer before transfer of the same using EVG-620 alignment set up as shown in Fig- 6.27. After soft baking (at 125°C for 30 sec), the mask pattern is transferred on wafer via exposure of UV light where they were aligned on the mask. The exposure time is optimized, during the experiment (~1.5 seconds) after the several iterations were made. Proper UV exposure time is essential to deliver light with the proper intensity, directionality, spectral characteristics and uniformity across the wafer.

6.2.6.2.3 Development and Post Baking

The photoresist (AZ315B) is developed in developer solution (MF26A) for 60 sec and then the sample is kept in oven for post baking at 125°C for 1 min in order to make further hardening of the exposed portion of photoresist.

6.2.6.3 Metallization

Material : Chrome (Cr) metal
Thickness: 150 nm-200 nm
Method : RF Sputtering/Thermal evaporation vacuum coating unit
Process Parameters:

RF power: 100 W
Ar flow rate: 200 sccm
O$_2$ flow rate: 20 sccm

The so-called *lift-off technique* is used to structure a thin-film material, which would be difficult to etch. Here, the thin-film material is deposited on top of the patterned photoresist layer. In order to avoid a continuous film, the thickness of the deposited film must be less than the resist thickness. In this regards, a chromium (Cr) metal layer of 150 nm thicknesses is deposited over the patterned wafer with the guiding layer using RF Sputtering unit. The total time taken for the deposition of chrome layer (thickness 150 nm) is $\sim$ 2-3 hrs, whereas deposition rate is 1.25 nm/sec. The photograph of RF sputtering unit is shown in Fig.-6.30 whereas Fig.-6.31 shows the window of process parameters respectively.

![RF Sputtering Unit](image)

**Fig.-6.30:** RF sputtering unit (Installed at CeNSE, IISc.)
Fig-6.31: Process parameters used for Cr metallization

6.2.6.4 Lift-off Technique

The lift off technique is widely used for the patterning of relatively thin waveguide cores. After metal deposition on photoresist content surface of the wafer, it was kept in boiled acetone for 3 minutes. The metal was lift from the places where the photo resist was present because photo resist is soluble in acetone. By removing the underneath photoresist, the thin-film material on top is also removed by ‘lifting it off’, leaving a structured thin film on the substrate.

After the lift-off, the structures are verified with the help of optical microscope
(shown in Fig.-6.32) before approaching to the further fabrication process. Fig-6.33 (a)-(c) shows the microphotograph of successful example structures whereas a few break/damage example structures are shown in Fig-6.34(a)-(c) respectively.

**Fig-6.32:** Optical Microscope (Model: Leika DFC290 at CeNSE, IISc.)

![Optical Microscope](image)

**Fig-6.33:** Microphotograph of successful lift-off structures (a) DC, (b) TMI coupler and (c) MMI coupler

![Microphotographs](image)

**Fig-6.34:** Microphotograph of failed lift-off structures (a) DC, (b) TMI coupler and (c) MMI coupler
6.2.6.5 Reactive Ion Etching

Reactive Ion Etching (RIE) is a dry etching technique which is used to selectively etch thin films in various device structures. The etching characteristic - selectivity, etch profile, etch rate, uniformity, reproducibility - can be controlled very precisely in the reactive ion etching. It involves a combination of both Physical Etching as well as Chemical Etching. Selection of an appropriate recipe (combination) of gases is an important issue. Typically the etch rates are slow and can be controlled by regulating parameters like the Electrode Bias, applied RF Power, Chamber pressure and flow rate of gases chosen in the recipe. RIE is capable of providing highly anisotropic profiles with reasonable selectivity. It is also possible to add custom recipes to etch new materials which are extremely useful for research purposes.

![Reactive Ion Etching of SiON](image)

Material to be etch : SiON
Thickness : 1-2 \textmu m
Method : F –based

**Process Parameters:**
- RF power : 50 W (Lower electrode)
- ICP power : 2500 W (Top)
- Chamber Pressure : 5 mTorr
- SF\textsubscript{6} flow rate : 9 sccm
- CHF\textsubscript{3} flow rate : 40 sccm
- Etch rate : 366 nm/min
- Etch duration : 6 minutes (for depth 2.2 \textmu m)
For the RIE process, the etch rates of the SiO$_x$N$_y$ films were determined first. The films were first etched separately and the etch rate of each film was determined. Following this, the patterned wafers were etched with an assigned time for the correct depth. Several issues were important for the etching processes: the side-wall anisotropy, side-wall roughness and grass formation. For the side-wall anisotropy, a mixture of tri-fluoromethane (CHF$_3$) and argon (Ar) were used as the process gas. With the above parameter specifications, the anisotropy and roughness were found to be within the limits of tolerance. In an RIE system, reactive ions are generated in plasma and are accelerated towards the surface to be etched, thus providing directional etching characteristics.

The basic reaction for the RIE of SiON can be written:

$$4CHF_3 + 2O_2 + 3SiON \rightarrow SiF_4 + CO_2 + 2H_2O + N_2$$

Fig.-6.35 shows the photograph of RIE system whereas the etch depth measurement result is shown in Fig.-6.37 obtained by using Dektak Set-up which is shown in Fig.-6.36 respectively.

Fig-6.35: RIE Set-up, F based (PlasmaLabSys-Oxford Instrument System), CeNSE
Fig.-6.36: Dektak Set-up for step height measurement (CeNSE, IISc.)

Fig-6.37: Step height measurement after RIE of SiON layer using Dektak system (depth~1.71 μm)
6.2.6.6 Wet Etching/RIE of Metallization (Cr) layer

Material to be etched : Cr
Thickness : 150 nm
Etchant used : H₂O:H₂O₂

Table-6.2: List of available etchants for wet etching

<table>
<thead>
<tr>
<th>Concentrations</th>
<th>Etchants</th>
<th>Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:3:12</td>
<td>KMnO₄: NaOH:H₂O</td>
<td></td>
</tr>
<tr>
<td>3:1</td>
<td>H₂O:H₂O₂</td>
<td></td>
</tr>
<tr>
<td>Concentrated and dilute</td>
<td>HCl</td>
<td></td>
</tr>
<tr>
<td>3:1</td>
<td>HCl:H₂O₂</td>
<td></td>
</tr>
<tr>
<td>2:1</td>
<td>FeCl₂: HCl</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cyantek CR-7s (Perchloric based)</td>
<td>7 min/μm</td>
</tr>
<tr>
<td>1:1</td>
<td>HCl: glycerine</td>
<td>12 min/μm after depassivation</td>
</tr>
<tr>
<td>1:3</td>
<td>[50g NaOH+100 ml H₂O]: [30g K₃Fe(CN)₆+100 ml H₂O]</td>
<td></td>
</tr>
</tbody>
</table>

6.2.7 Deposition of Top Cladding

Deposition of Upper Cladding (SiO₂)

Material to be deposit : SiO₂
Thickness : 2-3 μm
Method : PECVD
The basic reaction for the formation of the silica (SiO₂) can be written as follows:

\[ SiH₄ \text{ (gas)} + 4N₂O = SiO₂ \text{ (solid)} + 2H₂O \text{ (gas)} + 4N₂ \text{ (gas)} \]

The top cladding layer of SiO₂ is deposited using PECVD set-up (as shown in Fig.-6.14) with the following process parameters and a layer of thickness ~3 μm is achieved which takes around ~2 hrs for deposition process.

**Process parameters used:**
- RF power @ 13.56 MHz : 20 W
- Pump pressure : 1000 mTorr
- Silane (SiH₄) flow rate : 8.5 sccm
- N₂O flow rate : 710 sccm
- N₂ flow rate : 161 sccm
- Substrate temperature : 350°C
- Deposition rate : 1 μm/25 min

### 6.3. Fabrication of DC,TMI Coupler and MMI Coupler

As discussed in the chapter-3, the designed PID components—conventional directional coupler, two-mode interference coupler and multimode interference coupler are realized using the above mentioned fabrication techniques and process steps. Fabrication is carried out with the design parameter (for Δn=5%, n₁=1.5, n₂=1.45 and for Δn=3%, n₁=1.8, n₂=1.45, a=b=1.5 μm) as discussed in chapter-3 with SiON waveguide core surrounded by SiO₂ cladding layer. The flow chart of fabrication process steps is shown in the Fig.-6.39 whereas Fig.-6.38(a)-(c) shows the SEM images of fabricated device components, (a) Directional Coupler (DC), (b) Two Mode Interference (TMI) coupler and (c) Multimode Interference (MMI) coupler respectively. The measured experimental results are discussed in the proceeding sections.
Fig-6.38: SEM images of fabricated (a) Directional Coupler (DC), (b) Two Mode Interference (TMI) coupler and (c) Multimode Interference (MMI) coupler

Fig-6.39: Flow chart of fabrication process steps

6.4. Experimental Set-up and Measurements

After the fabrication of the designed structures (as discussed in previous
sections of the current chapter) of conventional directional coupler, two-mode interference coupler and multimode interference coupler with silicon oxynitride as the core material surrounded by silica cladding layer, the optical power loss measurement is execute for performance evaluation of the developed device components. After the dicing and polishing of waveguide end faces, optical loss characterization is done by end fire coupling method.

![Diagram of a Power loss measurement set-up](image)

**Fig-6.40:** Schematic block diagram of a Power loss measurement set-up

Fig-6.40 shows the schematic block representation of the experimental set-up that is used for measurement of power loss whereas the photograph of the developed measurement set-up in the laboratory is shown in Fig-6.41. Helium Neon laser (He-Ne) is used as a source of light which is focused by using a focusing lens (10X and 20X) into an optical fiber with a polarizer that enable us to choose TE or TM polarized light. The transmitted light through the testing devices to the other end is measured using power sensor (Ge doped/Model: FieldMax II-VIS from Coherent Inc.) attached to the Powermeter (Model: FieldMax II-TOP from Coherent Inc.). The complete set-up is kept on the top of vibration free optical bread board of size (1 m x
1 m x 1 m). The measured experimental results are discussed later in this current chapter. For measurement of beam spot at the end waveguides, the powermeter with power sensor is replaced in the above set-up with a CCD camera. The measured field spots are also discussed later on.

![Image](image.png)

**Fig-6.41:** Power loss measurement set-up

### 6.5. Experimental Results and Characterization

The fabricated device components are studied for power loss characteristics with the help of developed power loss measurements set-up and also determined the power imbalance with respect to the width tolerances. The measured experimental results are compared with the results obtained (as in the chapter-3) by simple effective index method which is discussed in details as follows.

#### 6.5.1 Coupling Characteristics of Directional Coupler with Δn=5 %

Fig-6.42 shows the normalized coupled power versus beat length with experimental measured results for DC of coupling gap h~0.5 μm, n₂=1.45, Δn=5 % and λ=1.55 μm. The black squares of the plot indicate the measured experimental results. From the plot, it is seen that the experimental measured results for the output
powers at the output access waveguides (cross and bar states) are matching well with the results obtained by using SEIM. The inset images in the figure shows the SEM photograph of the fabricated conventional directional coupler of beat length ~91.2 μm and the 3 dB coupler of beat length ~45.4 μm respectively. The beam spot is taken at the cross output access waveguide at beat length ~91.2 μm whereas the second image shows the beam spot at the bar state.

Fig-6.42: Normalized coupled power versus beat length with experimental measured results for DC of coupling gap h~0.5 μm, n₂=1.45, Δn=5% and λ=1.55 μm.

6.5.2 Coupling Characteristics of TMI Coupler with Δn=5%

Fig-6.43 shows the normalized coupled power versus beat length with experimental measured results for conventional TMI coupler. It is found that the beat length of the fabricated TMI coupler with Δn=5 % with h=0 μm, n₂=1.45, Δn=5 % are obtained as cross state ~45.1 μm whereas 3 dB coupler of beatlength ~22.6 μm respectively which are close to the results obtained by simple effective index method (SEIM) and beam propagation method (BPM). The black squares indicate the measured experimental results.
Fig-6.43: Normalized coupled power versus beat length with $\Delta n=5\%$ for two mode interference (TMI) coupler with coupling gap $h \sim 0 \, \mu m$, $2a=3 \, \mu m$.

6.5.3 Coupling Characteristics of MMI Coupler with $\Delta n=5\%$

Fig-6.44: Normalized coupled power versus beat length with $\Delta n=5\%$ for multimode interference (MMI) coupler with coupling gap $h \sim 4 \, \mu m$.
Fig.6.44 shows the normalized coupled power versus beat length with experimental measured results for conventional MMI coupler. It is found that the beat length of the fabricated MMI coupler with $\Delta n=5\%$ with $h=4$ $\mu$m, $n_2=1.45$, $\Delta n=5\%$ are obtained as cross state $\sim 79.9$ $\mu$m whereas 3 dB coupler of beatlength $\sim 40.1$ $\mu$m respectively which are close to the results obtained by simple effective index method (SEIM) and beam propagation method (BPM) as details are discussed in chapter-3. The black squares of the plot indicate the measured experimental results.

6.5.4 Power Imbalance Characteristics DC, TMI Coupler and MMI Coupler

Fig.6.45: Power Imbalance characteristics versus width tolerances ($\delta w$) for conventional directional coupler ($h\sim 0.5$ $\mu$m), conventional TMI coupler ($h\sim 0$ $\mu$m) and conventional MMI coupler ($h\sim 4.0$ $\mu$m), with index contrast $\sim 5 \%$, cladding index$\sim 1.45$, $a=1.5$ $\mu$m, $b=1.5$ $\mu$m and $\lambda\sim 1.55$ $\mu$m respectively.

Fig.6.45 shows plot for power imbalance $[=10 \log_{10} (P_3/P_4)]$ versus fabrication tolerances ($\pm \delta w$) of conventional directional coupler ($h\sim 0.5$ $\mu$m), conventional TMI
coupler (h~0 μm) and conventional MMI coupler (h~4.0 μm) with index contrast ~5%, cladding index~1.45, a=1.5 μm, b=1.5 μm and λ~1.55 μm respectively. It is seen that the power imbalance increases with ±δw=0 μm symmetrically for both the structures and the increase of power imbalance for directional coupler is slightly more than that of conventional MMI coupler and TMI coupler. The cross, dot and square signs shows the respective experimental values which are closed to that of the theoretical results obtained by simple effective index method (SEIM) based on sinusoidal modes. The rate of increase of power imbalance (dB) with respect to width tolerance for conventional DC, TMI and MMI couplers are approximately obtained as \( \frac{\partial}{\partial \delta w} \) [Power Imbalance (dB)]~0.15 dB/μm, 0.18 dB/μm and 0.13 dB/μm respectively. It is also required to study the dependence of power imbalance on wavelength for conventional MMI coupler and tooth shaped grating assisted MMI coupler. Finally, an overall comparison of experimental results with the results obtained by simple effective index method (SEIM) is summarized in the Table-6.3.

Table-6.3: Comparison of SEIM results with fabricated results

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Coupling Length (L_d), μm</th>
<th>SEIM Result</th>
<th>Experimental results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Cross</td>
<td>3 dB</td>
</tr>
<tr>
<td>Directional Coupler</td>
<td>91 μm</td>
<td>45.1 μm</td>
<td>91.2 μm</td>
</tr>
<tr>
<td>TMI Coupler</td>
<td>45 μm</td>
<td>22.3 μm</td>
<td>45.1 μm</td>
</tr>
<tr>
<td>MMI Coupler</td>
<td>80 μm</td>
<td>39.9 μm</td>
<td>79.9 μm</td>
</tr>
</tbody>
</table>

It is found that the tolerances between experimental results with SEIM based theoretical results are within ~10%.
6.6. Conclusion

In this chapter the design device components such as directional coupler, two mode interference coupler and multimode interference coupler are studied experimentally and compare the measured results with the results obtained by using simple effective index method (SEIM) based on sinusoidal modes. The adopted fabrication process steps and techniques along with process parameters are also discussed in details. The fabrication process and most of the characterizations are carried out under INUP at the Center of Excellence in Nano Science and Engineering (CeNSE), Indian Institute of Science (IISc.), Bangalore. The experimental measurement (power loss) and FTIR analysis are carried out at Tezpur University. From these studies, it is found that the beat length of DC, TMI coupler and MMI coupler are ~ 91.2 µm, 45.1 µm and 79.9 µm respectively which are almost closed to that obtained theoretically as discussed in chapter-3. The deviations of experimental results are within 10% tolerance.

References


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