7.1 Introduction to High-k Dielectrics

The imminent need for higher speed at reduced cost has forced us to reduce the dimensions thereby integrating a higher number of transistors on chip. Scaling has come in the form of reducing the thickness of gate dielectrics in MOS technology. SiO₂ being the widely used gate dielectric so far has its own advantages and limitations.

**Advantages of SiO₂ as Gate Dielectrics**

- Thermal growth is possible with excellent thickness control and uniformity
- Stable interface with Silicon substrate with minimum interface defects
- Excellent thermal and chemical stability
- Large band gap of 9 eV
- High breakdown fields of the order of 13 MeV cm⁻¹.

**Limitations of SiO₂ as Gate Dielectrics**

- The thickness limit of SiO₂ for scaling is about 7 Å below which the full band gap of the insulator may not be formed
- Below 3 nm charge carriers can flow through gate dielectric by tunneling process which increases exponentially with reducing thickness
- Large increase in leakage current as thickness is reduced
- \( V_G(\text{max}) \) decreases as the oxide thickness decreases.

These limitations has left us with no option other than finding an alternative material for gate dielectrics which can overcome the limitations of SiO₂ as well as go in par with the advantages. Although optimization using nitride/oxynitride gate stacks were under pursue to lower the leakage current, still a need for better high-k materials persisted in order to solve the issues such as negative bias temperature instability and mobility lowering [1,2]. With implementation of high-k, essentially the gate leakage current was
reduced by several orders, but other issues such as thermal stability, interface layer control, increased interface charges and poly depletion still persists posing various degrees of challenges that require more R&D to overcome [3].

7.1.1 Why High-κ?

The need for a high permittivity (high-κ) material for future nano-electronic devices is very clear. High-κ dielectric materials have attracted much attention since physically thicker dielectric films are strongly required to create a very thin equivalent oxide thickness for sub-0.1 μm complementary metal–oxide–semiconductor technology.

It is well known that a MOS structure behaves like a capacitor and the value of capacitance ‘C’ is given by

\[ C = \frac{A\varepsilon_r\varepsilon_0}{t_{ox}} \]

where,

\[ \varepsilon_r = k = 3.9 \text{ (SiO}_2\text{)} \]

\[ \varepsilon_0 = \text{Permittivity of free space} = 8.85 \times 10^{-12} \text{ Fm}^{-1}. \]

The only feasible method to increase the capacitance is by decreasing the thickness of the dielectric. But when SiO₂ reaches its limit an alternate way of increasing the capacitance is by using materials with high \( \varepsilon_r \) or high \( k \).

For example, 1 nm thick SiO₂ can be replaced by 5.1 nm ZrO₂ (\( \varepsilon_r \approx 20 \)). The Equivalent Oxide Thickness of any dielectric material is calculated with respect to SiO₂ using the formula

\[ \frac{t_{eq}}{\varepsilon_r(\text{SiO}_2)} = \frac{t_{highK}}{\varepsilon_r(\text{highK})} \]

Some of the properties preferred from alternative dielectrics are briefed below

- Good thermal stability in contact with Si preventing the formation of interfacial SiOₓ and silicide layers
- Low density of intrinsic defects at the interface (\(< 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}\))
- Large band gap to reduce the leakage current
• Compatibility with CMOS processing.

A few dielectrics with its k values are listed in Table 7.1.

Table 7.1: List of few High-k dielectrics

<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al$_2$O$_3$</td>
<td>9-11</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>14-25</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>15-26</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>25-26</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>50-80</td>
</tr>
</tbody>
</table>

TiO$_2$ having a high $\varepsilon_r$ value is still not preferred as it strongly reacts with Silicon. Another consideration is that band gap tends to decrease with increasing dielectric constant. Therefore medium k oxides with relatively wide band gap are currently focused as a replacement for SiO$_2$.

7.1.2 Areas of Concern for Alternative Dielectrics

Thermo Dynamical Compatibility

The dielectric materials should be resistant to reactions and should produce low permittivity silicates, silica or conducting silicides during deposition or post deposition heat treatments. Structural match of oxide layer to silicon has to be taken care during epitaxial growth. Precise atomic registry across the Si/Gate oxide interface can help the system against nucleation of reaction products.

Process Flow Options

The high temperature backend processing step strongly limits the number of alternative metal oxides. The gate oxide must be able to survive the heat treatment without formation of low dielectric constant interface or metal silicides. Another replacement for the regular high temperature process is the Gate stack process flow which allows high
temperature dopant diffusion anneals before high k deposition. Subsequent anneals can be limited to 550 °C.

**Dielectric Properties**

Dielectrics can be of distinct microstructures-epitaxial film dielectrics, smooth and homogenous amorphous gate dielectrics. A defect free microstructure can be achieved through amorphous solids, but unfortunately non crystalline dielectrics are less common.

**Electronic Structure**

The bandgap of the dielectrics should be large such that electronic transitions between valence and conduction states are minimized. If the bandgap is low the material will not be resistive enough to provide charge storage over acceptable time periods.

**Defect Chemistry**

Above absolute zero, point defects are predicted and the type of defects depends on the crystal structure. These defects can act as trap sites which can influence the dielectric leakage current and transistor operation. Mg vacancies in MgO and Ti interstitials in TiO$_2$ are some of the examples for point defects observed in dielectrics.

**7.1.3 Interface Properties of Various High- k Materials with Silicon**

Regular process flow consists of high temperature process in oxygen atmosphere after the dielectric deposition/growth. SiO$_x$N$_y$ & SiO$_2$ films being inert, are very stable on silicon and, the oxygen diffusion during the post deposition high temperature process in oxygen atmosphere cause no chemical change. In contrast, the alternative oxides for high-k dielectrics are reactive in O$_2$ containing atmosphere and are less stable. Oxygen diffusion strongly reacts with three regions namely surface, bulk and interface.

**Interaction with bulk results in**

- Change in dielectric constant of high-k film
- Change in flat band voltage of the capacitor
- Change in threshold voltage of the transistor.
Interaction with High-k Si Interface

- Oxygen arrival at the high- k/Si interface forms SiO₂ layer and metal silicates leading to high k-SiO₂ and high k silicate stacks which lowers the overall dielectric constant.
- Oxygen arrival triggers the Si interstitials and are transported across high k films which changes the film composition.

Interaction with Gate Metal - High- k Interface

- Si interstitials migrated across the high k interacts with the gate metal electrodes and forms metal silicides at the dielectric - metal electrode interface changing the Fermi level and the electrical conductivity.
- A low capacitance layer is formed in series with high k dielectric.

7.1.4 Defects Related Issues on High-k Dielectrics

An ideal insulator should have less leakage current and a low loss tangent. The leakage current has two components. One comes from tunneling when oxide thickness is very small and the second one is the defect related channel which involves dislocations, grain boundaries or point defects.

The specific problems caused by the defects include

- Initiation of degradation
- Charge trapping
- Creation of fixed charge which causes carrier scatter in Si substrate.

The defects also cause the dielectric properties to vary as they move within the dielectric leading to failure of the devices. Non-Stoichiometry in the films which results from defects or charge carriers gives rise to charge transport or dielectric loss. Such defects cause conduction along grain boundaries or dislocations, resistance degradation etc. Vacancies are generated in the films and the bulk samples due to growth, deposition and doping process. Post deposition anneal of the films is an intrinsic part of any growth cycle and involves oxygen and nitrogen diffusion through the oxide and the possible formation of interstitial oxygen or nitrogen species. Oxygen diffuses into films in atomic
form and once incorporated, the oxygen can act as an electron trap, changing its charge state and therefore its properties and interactions with the oxide and other defects.

Oxygen vacancies in silica have been implicated as possible electron and hole traps responsible for oxide charging and degradation. Charged oxygen vacancies in hafnia films can also be generated from electron and hole trapping from silicon. These cause the displacement of Hf ions. Oxygen vacancies in monoclinic hafnia formed in three and four coordinated oxygen sites are called V3 and V4 respectively. The possible defect level of V3 is found to be 9.36 eV and that of V4 to be 9.34 eV. Oxygen incorporation which forms oxygen interstitials are also observed at +1.6 eV for atomic oxygen and +4.2 eV for molecular oxygen [4-6].

7.1.5 Band Offset and Band Alignment

When two semiconductors with different band gaps are joined, the conduction and valence bands cannot both be aligned. Band offset may exist in the conduction band, the valence band or both. To replace SiO₂ with a high-k dielectric, one of many requirements is that both valence and conduction band offsets of the material (with respect to the silicon band edges) need to be greater than 1 eV. Garfunkel et. al. [9] reports the energy gap (E₉), the valence band offset (ΔEv ) and the conduction band offset (ΔEc) of different materials as given in the Table 7.2

<table>
<thead>
<tr>
<th>Material</th>
<th>E₉</th>
<th>ΔEv</th>
<th>ΔEc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO₂</td>
<td>8.9</td>
<td>4.5</td>
<td>3.3</td>
</tr>
<tr>
<td>HfO₂</td>
<td>5.7</td>
<td>2.7</td>
<td>1.9</td>
</tr>
<tr>
<td>Hf₀.₇Si₀.₃O₂</td>
<td>6.0</td>
<td>2.8</td>
<td>2.1</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>5.5</td>
<td>2.7</td>
<td>1.7</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>7.0</td>
<td>3.2</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Table 7.2: Band gap and Band offsets in various High-k materials
The high-k materials being currently investigated for integration into future IC technologies include Al₂O₃, HfO₂, ZrO₂, Y₂O₃ and Ta₂O₅ and/or the silicates and aluminates of some of these materials [11]-[21]. The dielectric constant (ε_{high-k}) is in the range of 10-40, approximately 3-10 times higher than that of SiO₂ (ε_{SiO₂} = 3.9) [15]. However, some of them have narrow bandgaps, which will lower the barrier height for tunneling. Since leakage current increases exponentially with decreasing film thickness and barrier height [22]-[23], this trade-off between dielectric constant and barrier height will determine the relative advantages that an alternative dielectric offers in terms of reduced leakage current. Initial data in the literature show that the net effect for high-k materials is a reduced leakage current; some high-k gate dielectrics exhibit up to ~5 orders of magnitude less leakage current than electrically equivalent SiO₂ [15], [24]-[25].

The Group IV metal oxide HfO₂ has been studied extensively for future commercial and space electronics [9], [12], [16], [18], [26]-[27] due to its high dielectric constant (~22) [28]-[29], relatively wide bandgap (~5.6 eV), sufficient band offset (> 1.4eV) [33], and thermal compatibility with Si-based processing [31]-[32]. It has also been reported by Sayan et.al.[10] that the valence and conduction band offsets for HfO₂ films were found to be 3.61 and 1.97 eV. These offsets are large enough to confirm HfO₂ to be a viable high-k candidate from a barrier height perspective [7-10].

### 7.2 Fabrication of HfO₂ based MOS Capacitors

HfO₂ based MOS capacitors were fabricated on p-type 1–10 ohm-cm resistivity, (100) orientation and ~300 μm thick silicon substrates. High purity HfO₂ (99.9% purity) 5-inch sputtering target was used to deposit the thin films in MRC rf-sputtering system. The wafers were cleaned by using standard piranha cleaning procedure for removing organic and inorganic contaminations.

The wafers were etched in dilute HF (1: 20), rinsed in DI water and dried in dry N₂ immediately before loading in the vacuum chamber. The vacuum chamber was evacuated to the background pressure of 1.2 × 10⁻⁶ Torr. The sputtering was done in high purity argon ambient gas with gas pressure maintained at 6 m Torr. Thin films of HfO₂ were deposited on silicon substrate at sputtering voltage 0.8 kV for 10 mins keeping film thickness 15–20 nm corresponding to equivalent oxide thickness of SiO₂ about 4.5 nm.
The as deposited films were thermally annealed at 700 °C in oxygen ambient for 30 min. The Aluminum thin films of about 700 nm were deposited on both side of the wafer, used as top electrode and back contact. The metal film was patterned using photolithography and metal etching. The MOS structures were finally annealed in forming gas at 450 °C. The film thickness was measured using Ambios step profiler. Figure 7.1 show the structure of HfO₂ based MOS capacitor. The flat band voltage ($V_{FB}$) calculated by comparing the C-V curve of un-irradiated device with ideal curve was -1.65 V. The doping concentration was calculated to be $4.29 \times 10^{15}$ cm$^{-3}$ by plotting $1/C^2$ vs $V$ for un-irradiated device.

![Figure 7.1: Structure of HfO₂ based MOS capacitor](image)

**7.3 Radiation Response of HfO₂ based MOS Capacitors**

In the present scenario, radiation effects community are entering a situation somewhat analogous to that of 30 years ago, early in silicon dioxide technology. An enormous amount of effort was required to develop conventional silicon dioxide-based radiation hard technologies. A similar effort may be required to adapt the new high-k systems for radiation hard applications. Despite the large amount of ongoing research into alternative dielectrics, very little work has been done to understand the radiation responses of these materials.

HfO₂ based MOS capacitors were irradiated by 50 MeV Li$^{3+}$ ions for various fluences ranging from $5 \times 10^{10}$ Li ions cm$^{-2}$ to $1 \times 10^{12}$ Li ions cm$^{-2}$ at Inter University Acceleration Center (IUAC), New Delhi. Samples were mounted on a metallic holder.
and placed in general purpose scattering chamber at a vacuum of $10^{-6}$ torr. The ions were beamed to fall on the front side of the device exactly at right angles. The scanning area was fixed at $1 \times 1$ cm$^2$ with a magnetic scanner to obtain uniform fluence over the devices. The beam current was maintained at 1 nA. The electrical characterization of the devices before and after irradiation was performed using a Keithley 4200-SCS integrated system with a 590CV analyzer and shielding probe station. The electrical properties of MOS devices were investigated at 1 MHz frequency at room temperature before and after Li$^{3+}$ ions irradiation. In this section, the radiation response of HfO$_2$ based MOS capacitors to 50 MeV Li$^{3+}$ ions are described in terms of changes in series resistance and interface state density and accumulation capacitance.

Figure 7.2 shows the high frequency (1 MHz) C-V characteristics of Virgin and Li ion irradiated MOS capacitors for various Li fluences viz. $5 \times 10^{10}$ ions cm$^{-2}$, $1 \times 10^{11}$ ions cm$^{-2}$, $5 \times 10^{11}$ Li ions cm$^{-2}$ and $1 \times 10^{12}$ ions cm$^{-2}$. The shift in the flat band voltage ($V_{FB}$) of the irradiated devices is extracted from C-V curves by comparing with the ideal curve. It is found that the $V_{FB}$ reduces with increasing fluence from -1.65 V for unirradiated devices to -0.96 V for device irradiated with $1 \times 10^{12}$ Li ions cm$^{-2}$. The doping concentration ($N_A$) was calculated by plotting $1/C^2$ vs. $V$ for both un-irradiated and irradiated devices from the experimental C-V plots and the values are reported in Table 7.3.

From Figure 7.2 it can be noticed that there is a large variation in the accumulation capacitance while no appreciable change has been observed in the inversion region. In principle, the change in capacitance may occur due to the changes in capacitor area, dielectric thickness, or dielectric constant. If the area and dielectric thickness are assumed to be constant, the changes in capacitance can be attributed to the change in the dielectric constant of the film. It has been reported that the dielectric constant of a material, defined as one plus the electric susceptibility ($1+\chi_e$), is directly proportional to the dipole moment of a material which can alter the dielectric constant [34]. Structural modifications of the dielectric films induced by irradiation leads to change in dielectric constant which in-turn affects the accumulation region. This sort of behaviour (change in accumulation capacitance) has also been reported by other researchers and the origin of
such a behaviour is still not understood [35]. The other factors contributing for the improvement in the accumulation capacitance has to be further investigated.

![Graph showing C-V characteristics](image)

**Figure 7.2:** High frequency C-V characteristics of Li-ion irradiated HfO₂ based MOS capacitors

**Table 7.3:** Calculated values of flat band voltage ($V_{fb}$) and doping concentration ($N_A$) for Li ion irradiated HfO₂ based MOS capacitors

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Fluence (ions cm⁻²)</th>
<th>$V_{fb}$ (Volts)</th>
<th>$N_A$ (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Un-irradiated</td>
<td>-1.65</td>
<td>$3.3 \times 10^{15}$</td>
</tr>
<tr>
<td>2</td>
<td>$5 \times 10^{10}$</td>
<td>-1.49</td>
<td>$2.9 \times 10^{15}$</td>
</tr>
<tr>
<td>3</td>
<td>$1 \times 10^{11}$</td>
<td>-1.28</td>
<td>$2.8 \times 10^{16}$</td>
</tr>
<tr>
<td>4</td>
<td>$5 \times 10^{11}$</td>
<td>-1.17</td>
<td>$3.4 \times 10^{16}$</td>
</tr>
<tr>
<td>5</td>
<td>$1 \times 10^{12}$</td>
<td>-0.96</td>
<td>$6.1 \times 10^{16}$</td>
</tr>
</tbody>
</table>

Figure 7.3 shows the changes in series resistance ($R_s$) of the HfO₂-based MOS devices before and after irradiation for various Li⁺⁺ ion fluencies. It is observed that the values of the series resistance ($R_s$) increase as the ion fluence increases.

175
The increase in series resistance of irradiated devices can be attributed to the dopant reduction in the silicon bulk caused due to ion irradiation. The dopant reduction effect of the order of one has also been observed for other radiation sources [36-37]. Irrespective
of the oxide material, the series resistance is dependent on the thickness of the oxide and the frequency at which the device is characterized [38-39]. The front and back contact probing during measurement, the resistance at the bulk of silicon and the non-uniform doping underneath the gate are some of the other factors which affect the series resistance of the device [40]. Figure 7.4 shows the variation in interface charge density ($D_{it}$) of HfO$_2$-based MOS capacitors for various Li ion fluences. The decrease in $D_{it}$ with increase Li ion fluences seems to be very interesting which can be attributed to the improvement in the interface properties of the device.

7.4 Conclusion

The radiation response of high-k dielectric HfO$_2$ based MOS capacitors is studied. The C-V characteristics of Al/HfO$_2$/Si MOS capacitor prepared by rf-sputtering deposition method were carried out at 1 MHz before and after 50 MeV Li$^{3+}$ ions irradiation. The changes in the series resistance $R_s$ and interface traps density ($D_{it}$) of the devices for various Lithium ions were calculated using the experimental C-V curves. The series resistance of MOS capacitors calculated at strong accumulation region was found to increase with ions fluence while the $D_{it}$ was found to decrease with ions fluence. The increase in accumulation capacitance and decrease in interface trap density after irradiation seems to be very interesting. The change in the electrical properties of the devices may be attributed to the change in physical properties of the HfO$_2$ thin films. Sufficient clarity could not be established at present for the change in dielectric properties of the film. Further investigation is required for better understanding of the factors which initiate the changes in the film dielectric properties and to correlate between the physical properties of the high-k films and the device performance in the radiation harsh environment.

References


