### LIST OF SYMBOLS, NOTATIONS AND ABBREVIATIONS

<table>
<thead>
<tr>
<th>Symbol/Notation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{blp}$</td>
<td>Long line capacitance of top up precharge</td>
</tr>
<tr>
<td>$C_{pc}$</td>
<td>Capacitance of precharge transistor</td>
</tr>
<tr>
<td>$C_{a}$</td>
<td>Capacitance of access transistor</td>
</tr>
<tr>
<td>$C_{ts}$</td>
<td>Capacitance of bidirectional transmission logic</td>
</tr>
<tr>
<td>$C_{wbl}$</td>
<td>Capacitance of long line wire</td>
</tr>
<tr>
<td>$R_{pu}$</td>
<td>Resistance of pull up transistor</td>
</tr>
<tr>
<td>$T_{pc}$</td>
<td>Time for precharge</td>
</tr>
<tr>
<td>$R_{bl}$</td>
<td>Resistance of long line wire</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Channel length modulation parameter</td>
</tr>
<tr>
<td>$W$</td>
<td>Aspect ratio of transistor</td>
</tr>
<tr>
<td>$L$</td>
<td>Long line voltage</td>
</tr>
<tr>
<td>$W_{a}$</td>
<td>Width of access transistor</td>
</tr>
<tr>
<td>$R_{Sh}$</td>
<td>Sheet resistance</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>Oxide layer capacitance per unit surface area</td>
</tr>
<tr>
<td>$W_{AE}$</td>
<td>Critical width of access transistor for energy cost function</td>
</tr>
<tr>
<td>$W_{AT}$</td>
<td>Critical width of access transistor for time cost function</td>
</tr>
<tr>
<td>$I_{pu}$</td>
<td>Current through pull up transistor</td>
</tr>
<tr>
<td>$V_{dsat}$</td>
<td>Saturation voltage</td>
</tr>
<tr>
<td>$E_p$</td>
<td>Energy dissipated in precharge</td>
</tr>
<tr>
<td>$P_{pc}$</td>
<td>Power dissipation in precharge</td>
</tr>
<tr>
<td>$R_{pc}$</td>
<td>Resistance of precharge transistor</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>Activity factor</td>
</tr>
<tr>
<td>$P_{pu}$</td>
<td>Static dissipation in precharge and pull up transistors</td>
</tr>
<tr>
<td>$I_{pu}$</td>
<td>Leakage current in pull up transistor</td>
</tr>
<tr>
<td>$I_{pc}$</td>
<td>Leakage current in precharge transistor</td>
</tr>
<tr>
<td>$Area_{pu}$</td>
<td>Area of top up precharge</td>
</tr>
<tr>
<td>$W_{pu}$</td>
<td>Width of pull up transistor</td>
</tr>
<tr>
<td>$W_{pc}$</td>
<td>Width of precharge transistor</td>
</tr>
<tr>
<td>$L$</td>
<td>Length of transistor</td>
</tr>
<tr>
<td>$C_{io}$</td>
<td>Capacitance of input/output logic</td>
</tr>
<tr>
<td>$I_{da}$</td>
<td>Drain current in access transistor</td>
</tr>
<tr>
<td>$T_{wcy}$</td>
<td>Write cycle time</td>
</tr>
<tr>
<td>$I_{nx}$</td>
<td>Leakage current in n transistor</td>
</tr>
<tr>
<td>$I_{px}$</td>
<td>Leakage current in p transistor</td>
</tr>
<tr>
<td>$I_{ax}$</td>
<td>Leakage current in access transistor</td>
</tr>
<tr>
<td>$R_a$</td>
<td>Resistances of access transistors of a cell</td>
</tr>
<tr>
<td>$R_n$</td>
<td>Resistances of pull down transistors of a cell</td>
</tr>
<tr>
<td>$C_{blw}$</td>
<td>Overall capacitive load on long line</td>
</tr>
<tr>
<td>$C_{bls}$</td>
<td>Capacitive load on read assist sense amplifier</td>
</tr>
</tbody>
</table>
$T_{phl}$ High to low transition time
$E_{sense}$ Energy dissipated in read assist sense amplifier
$P_{sense}$ Power dissipation in read assist sense amplifier
$P_{sow}$ Static dissipation in read assist sense amplifier
$Area_s$ Area on chip by read assist sense amplifier
$T_R$ Read time
$K_1$ Cost function for energy
$K_a$ Constant for access transistor
$K_n$ Constant for n transistor
$W_n$ Width of n transistor
$L_{bl}$ Length of long line
$W_{bl}$ Width of long line
$E_{fetched}$ Energy fetched
$E_{stored}$ Energy stored
$E_{dissipated}$ Energy dissipated
$V_e$ Proportionality constant
$\Delta V_{bl}$ Differential voltage swing of long line
$V_{Th}$ Threshold voltage at temperature $T^oK$
$V_T$ Threshold voltage at ambient temperature $T_{amb}^oK$
$C_{depl}$ Depletion capacitance
$V_{r0}$ Threshold voltage fixed for given technology
$S$ Slope factor
$10T$ 10-Transistor
$2-D$ 2-Dimensional
$6T$ 6-Transistor
$8T$ 8-Transistor
$ABD$ Absolute Difference
$A_{cell}$ Area of cell
$ASIC$ Application Specific Integrated Circuit
$BB$ Bulk Bias
$BCE$ Boundary Condition Estimator
$BDI$ Block Data Interpolation
$BHE$ Block Header Estimation
$BL(bl)/LL(ll)$ Bit Line/Long line
$BL'(BL_{BAR})/LL'(LLB)$ Complement of Bit Line/Long Line
$C$ Code book
$CAM$ Content Addressable Memory
$CC$ Curve Compensation
$C_i$ Code vector
$C_{ik}$ Pointed code book vector
$C_j$ Reference code vector at address j
$C_{min}$ Nearest match reference code vector
$CMOS$ Complementary Metal Oxide Semiconductor
$CR$ Charge Recycle
$CSI$ Cauchy-Schwarz Inequality
$CVR$ Code Vector Renderer
$D$ Distortion measure
$D(X_k, C_i)$ Distortion between input and reference code vector
$D_{ND}$ Distortion indicating negative polarity
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Distortion indicating positive polarity</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
</tr>
<tr>
<td>DRG</td>
<td>Data Retention Gated ground cache</td>
</tr>
<tr>
<td>DTA</td>
<td>Double Test Algorithm</td>
</tr>
<tr>
<td>EENNS</td>
<td>Equal Average Equal Variance Nearest Neighbor Search</td>
</tr>
<tr>
<td>ENNS</td>
<td>Equal-Average Nearest Neighbor Search</td>
</tr>
<tr>
<td>FCRC</td>
<td>Fast Convergence Reduced Complexity</td>
</tr>
<tr>
<td>fps</td>
<td>Frames Per Second</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>FSVQ</td>
<td>Full Search Vector Quantization</td>
</tr>
<tr>
<td>GW</td>
<td>Gold Washing</td>
</tr>
<tr>
<td>HBLSA</td>
<td>Hierarchical Bit Line and Local Sense Amplifier</td>
</tr>
<tr>
<td>h&lt;sub&gt;j&lt;/sub&gt;</td>
<td>Header reference code vector at address j</td>
</tr>
<tr>
<td>HVQ</td>
<td>Hierarchical Vector Quantization</td>
</tr>
<tr>
<td>I</td>
<td>Set of indices through which search is done</td>
</tr>
<tr>
<td>i&lt;sub&gt;cmin&lt;/sub&gt;</td>
<td>Index for C&lt;sub&gt;min&lt;/sub&gt;</td>
</tr>
<tr>
<td>i&lt;sub&gt;hj&lt;/sub&gt;</td>
<td>Address of each h&lt;sub&gt;j&lt;/sub&gt;, called group id</td>
</tr>
<tr>
<td>i&lt;sub&gt;k&lt;/sub&gt;</td>
<td>Index</td>
</tr>
<tr>
<td>IOBW</td>
<td>Input Output Bandwidth</td>
</tr>
<tr>
<td>IPP</td>
<td>Inner Partial Product</td>
</tr>
<tr>
<td>J</td>
<td>Count that indicates stage number</td>
</tr>
<tr>
<td>K</td>
<td>Temperature coefficient constant of 0.7 mV/K</td>
</tr>
<tr>
<td>LBG</td>
<td>Linde-Buzo-Gray</td>
</tr>
<tr>
<td>LE</td>
<td>Logic Element</td>
</tr>
<tr>
<td>LL(ll)</td>
<td>Long Line</td>
</tr>
<tr>
<td>LLB(llb)</td>
<td>Long Line Bar</td>
</tr>
<tr>
<td>M</td>
<td>Total number of stages in code book</td>
</tr>
<tr>
<td>MAC</td>
<td>Multiply-And-Add</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MPS</td>
<td>Mean Distance Ordered Partial Codebook Search</td>
</tr>
<tr>
<td>N</td>
<td>Total number of reference code vectors</td>
</tr>
<tr>
<td>N/A</td>
<td>Not applicable or not mentioned</td>
</tr>
<tr>
<td>N&lt;sub&gt;C&lt;/sub&gt;</td>
<td>Total number of partitions</td>
</tr>
<tr>
<td>N&lt;sub&gt;Cc&lt;/sub&gt;</td>
<td>Total number of code vectors in a partition</td>
</tr>
<tr>
<td>N&lt;sub&gt;Ci&lt;/sub&gt;</td>
<td>i&lt;sup&gt;th&lt;/sup&gt; partition</td>
</tr>
<tr>
<td>NMOS</td>
<td>N Channel MOSFET</td>
</tr>
<tr>
<td>OTNNS</td>
<td>Nearest Neighbor Search Algorithm Based on Orthonormal Transform</td>
</tr>
<tr>
<td>PCL</td>
<td>Partition Count Logic</td>
</tr>
<tr>
<td>P&lt;sub&gt;dcell&lt;/sub&gt;</td>
<td>Static dissipation in cell</td>
</tr>
<tr>
<td>P&lt;sub&gt;dcells&lt;/sub&gt;</td>
<td>Total power dissipation in cells</td>
</tr>
<tr>
<td>PDE</td>
<td>Partial Distortion Elimination</td>
</tr>
<tr>
<td>P&lt;sub&gt;dpc&lt;/sub&gt;</td>
<td>Power dissipation in top up precharge</td>
</tr>
<tr>
<td>PDS</td>
<td>Partial Distortion Search</td>
</tr>
<tr>
<td>PMOS</td>
<td>P Channel MOSFET</td>
</tr>
<tr>
<td>P&lt;sub&gt;scells&lt;/sub&gt;</td>
<td>Total static dissipation in cells</td>
</tr>
<tr>
<td>P&lt;sub&gt;total&lt;/sub&gt;</td>
<td>Total power dissipation</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RC</td>
<td>Recycle</td>
</tr>
<tr>
<td>RCDC</td>
<td>Reduced Complexity 2-D Convergence</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computer</td>
</tr>
</tbody>
</table>
SAC  Sense Amplifying Cell
SARC  Switched Amplifier Random Access Memory Cell
SBTR  Subthreshold
SBTR-BB  Subthreshold with Bulk Bias
SIMD  Single Instruction Multiple Data
SNM  Static Noise Margin
SOA  State of Art
SOM  Self Organizing Map
SPICE  Simulation Program With Integrated Circuit Emphasis
SRAM  Static Random Access Memory
SVGA  Segmented Virtual Ground Architecture
SVGND  Segmented Virtual Ground
SVT  Sub Vector Technique
TCVQ  Trellis Coded Vector Quantization
TG  Transmission Gate
TIE  Triangular Inequality Elimination
TMS  Threshold Modulated Separation of read & write
TOX  Oxide Layer Thickness
u_{hj}  Sub-vector derived from h_j
V_{dd}/V_{DD}  Supply voltage
V_{ddpc}/V_{DDPC}  Top up precharge supply voltage
V_{llbpp}  Peak to peak voltage on long line bar
V_{lpp}  Peak to peak voltage on long line
VLSI  Very large Scale Integration
VQ  Vector Quantization
w  Word length of I/O
X_i  Input code vector
X_k'  Reproduced code vector