4.1 Introduction

Design of fine grain elements and codebook is discussed earlier. Performance parameters of such VLSI circuits are speed, power/energy dissipation, throughput and area on chip. Since these parameters are interdependent, optimization for one parameter leads to penalty in terms of others. Optimization process becomes crucial when it is matter of codebook. Designs and optimization of supplies for fundamental fine grain elements of codebook have been explored earlier. This chapter deals with the development of cost functions for energy, time and power separately. Involvement of devices and passive element parasitics are different in these cost functions. Since codebook occupies large space on chip, power dissipation also becomes dominant, which has been emphasized. Section 4.2 deals with optimization of cost function for energy while 4.3 explores optimization of cost function for time. Similarly cost function for power and related optimization model are given in section 4.4. Results and conclusions are summarized in section 4.5.

4.2 Optimization of Cost Function for Energy

Energy function for a cell is given by

\[ K_1 = \int_0^T \left( \text{Power} \right) dt \]

\[ \therefore Time \approx T_R = \left[ \frac{K_a}{W_a} + \frac{K_n}{W_n} + R_{SH} \frac{L_{bl}}{W_{bl}} \right] C_{blw} \]

\[ C_{blw} = C_{pc} + \int_0^M \left[ C_a \right] dc + C_{c} + C_{io} + C_{cbl} \]

\[ Power = \frac{C_{blw} [V_{dd} - V_{ddpc}]^2}{T_R + T_{pc}} \]

where, \( K_a \) (\( K_n \)) is constant for access (pull down) transistor of a cell, \( R_{SH} \) is sheet resistance, \( L_{bl} \) (\( W_{bl} \)) is length (width) of long line, \( T_R \) (\( T_{pc} \)) is read (precharge) time.
Schematic exploring long line capacitor $C_{blw}$ and related current $i$ giving voltage swing $V_{bl}$ are shown in Fig. 4.1. Energy fetched from supply is given by

$$E_{fetched} = \int_{0}^{T} (V_{dd} \times i_{average}) dt$$

$$= C_{blw} V_{dd} \Delta V_{bl}$$

Energy stored in $C_{blw}$ is given by

$$E_{stored} = \frac{C_{blw} \Delta V_{bl}^2}{2}$$

Energy and power dissipated become

$$E_{dissipated} = \frac{C_{blw} \Delta V_{bl} [2V_{dd} - \Delta V_{bl}]}{2}$$

$$Power = \frac{C_{blw} \Delta V_{bl} [2V_{dd} - \Delta V_{bl}]}{T_{R} + T_{PC}}$$

Simplifying ahead,

$$K_1 = V_{dd} \left[ \frac{C_{blw} \Delta V_{bl}}{T_{R} + T_{PC}} \right] \left[ \frac{1.7 K_u}{W_a} + R_{bl} \right] \left[ M C_{ox} W_a L + C_{wbl} \right]$$

But

$$T_{PC} = \frac{Q}{I_{ch\ avg\ e}} = \frac{C_{blw} \Delta V_{bl}}{I_{ch\ avg\ e}}$$
and

\[ C_{blw} = MC_{ox}W_dL + C_{wbl} \]

where, \( R_{bl} \) is resistance of bit line/long line (LL), \( C_{ox} \) is oxide layer capacitance per unit area and \( L \) is length of transistor i.e. 250 nm.

Simplifying ahead

\[ K_1 = V_{dd} \Delta V_{bs} \left[ MC_{ox}W_dL + C_{wbl} \right] \left[ \frac{1.7K_a}{W_a} + \frac{R_{bl}}{1.7K_a + W_aR_{bl} + \Delta V_{bs} \rho_{pu}} \right] \]

Let

\[ V_{dd} \Delta V_{bs} = V_i \times V_i \quad \text{and} \quad \frac{V_{bs}}{\text{I Fog e}} = R_{pu} \]

Simplifying ahead

\[ K_1 = d \left[ V_aMC_{ox}W_dL(1.7K_a) + V_dMC_{ox}W_dLR_{bl}(W_a) + V_cC_{wbl}(1.7K_a) + V_cC_{wbl}W_dR_{bl} \right] \]

\[ \frac{1.7K_a + W_aR_{bl} + R_{pu}}{1.7K_a + W_aR_{bl} + \Delta V_{bs} \rho_{pu}} \]

Differentiating w.r.t. \( W_a \), equating to 0 and simplifying ahead, optimum resistance and width of access transistor are given by

\[ R_a = \left| \frac{R_{bl} + \rho_{pu}}{3.4} \right| \]

\[ W_a = \left| \frac{3.4K_a}{R_{bl} + \rho_{pu}} \right| \]

Codebook column is designed for the optimum width of an access transistor given by this equation. Widths, areas, perimeters of access transistors are varied and simulations of an overall column are carried out. Variation of power dissipation of column (except cells & top-up precharge) with width (\( W_a \)) of access transistor is shown in Fig. 4.2.

It is observed that dissipation goes almost minimum at critical width (\( W_{ae} \)) of 11 \( \mu \)m. Variation of top-up precharge power dissipation with width (\( W_a \)) of access transistor is shown in Fig. 4.3. Since it is not function of access device, remains unaffected. Similarly total cells power dissipation settles to almost minima at \( W_{ae} \) as shown in Fig. 4.4. Total column dissipation also remains stable around \( W_{ae} \) as shown in Fig. 4.5. Variations of LL and LLB voltages are shown in Fig. 4.6 and 4.7 respectively. Fig. 4.8 shows total cells leakage dissipation. Individual cell power and leakage power dissipations are shown in Fig. 4.9 and 4.10 respectively.
Fig. 4.2 Variation of power dissipation of column (except cells & top-up precharge) with width (\(W_a\)) of access device

Fig. 4.3 Variation of top-up precharge power dissipation with width (\(W_a\)) of access device

Fig. 4.4 Variation of total cells power dissipation with width (\(W_a\)) of access device
Fig. 4.5 Variation of total power dissipation of column with width ($W_a$) of access device

Fig. 4.6 Long line voltage swing $V_{LL_{pp}} \max$ w.r.t. width ($W_a$) of access device

Fig. 4.7 Long line bar voltage swing $V_{LL_{Bpp}} \max$ w.r.t. width ($W_a$) of access device
Fig. 4.8 Variation of total cells leakage power dissipation with width ($W_a$) of access device

Fig. 4.9 Variation of cell power dissipation with width ($W_a$) of access device

Fig. 4.10 Variation of cell leakage power dissipation with width ($W_a$) of access device
4.3 Optimization of Cost Function for Time

Factored design gives minimum dissipation whereas flat gives minimum delays. Access transistor plays an important role in these designs. Parameters of this device are modulated so as to achieve minimum latency which is indicated by the slopes of swings on long lines. Stress is given on read access time than write because codebook read operations are frequent than that of write.

Read time is given by

\[
T_r = \left[ \frac{K_a}{W_a} + \frac{K_n}{W_n} + R_{bl} \right] \left[ MC_{oa} W_a L + C_{wbl} \right]
\]

\[
= 1.7 K_a MC_{oa} L + 1.7 \frac{K_a}{W_a} C_{wbl} + R_{bl} MC_{oa} W_a L + R_{bl} C_{wbl}
\]

Differentiating w.r.t. \(W_a\), equating to zero and simplifying ahead,

\[
W_a = \frac{1.7 K_a C_{wbl}}{R_{bl} MC_{oa} L}
\] (4.2)

It is critical value of device width (\(W_{aT}\)). Putting all variables, it becomes 2 µm. This width is varied from 0.25 to 4 µm for experimentation. Other parameters such as area, perimeter etc. are varied accordingly. Widths of n and p transistors of storage cell are also changed to 6 and 0.25 µm respectively so that there will not be any read/write operation violation.

Fig. 4.11 shows variation of power dissipation of column w.r.t. width of access transistor. It is maximum of 147 µW at \(W_{aT}\) as penalty of time. Precharge dissipation increases gradually from 727.5 µW to 1685 µW with \(W_a\) as it is not part of optimization for time as shown in Fig. 4.12. Variation of total power dissipation except in a single cell is shown in Fig. 4.13. LL and LLB swings are indications of fast recovery of charges and hence latency. The crests observed are 255 mV and 187 mV in Fig. 4.14 and 4.15 respectively. Individual cell dynamic power and leakage power dissipations increase with device width as shown in Fig. 4.16 and Fig. 4.17. LL and LLB swings are shown in Fig. 4.18 and 4.19. The differential swing is 37 mV around \(W_{aT}\) as shown in Fig. 4.20. The differential swing is also 68 mV at \(W_{aT}\) as shown in Fig. 4.21.
Fig. 4.11 Variation of power dissipation of column (except cells and precharge) with width ($W_a$) of access device

Fig. 4.12 Variation of precharge power dissipation with width ($W_a$) of access device

Fig. 4.13 Variation of total power dissipation except dissipation in an active single cell with width ($W_a$) of access device
Fig. 4.14 Long line voltage swing max w.r.t. width ($W_a$) of access device

Fig. 4.15 Long line bar voltage swing max w.r.t. width ($W_a$) of access device

Fig. 4.16 Variation of cell power dissipation with width ($W_a$) of access device
Fig. 4.17 Variation of cell leakage power dissipation with width ($W_a$) of access device

Fig. 4.18 Long line voltage swing max w.r.t. width ($W_a$) of access device

Fig. 4.19 Long line bar voltage swing max w.r.t. width ($W_a$) of access device
Fig. 4.20 Differential swing ($|\Delta Swing|$) between long lines w.r.t. width ($W_a$) of access device

Fig. 4.21 Differential swing ($|\Delta Swing|$) between long lines w.r.t. width ($W_a$) of access device

**4.4 Optimization of Cost Function for Power**

Cost function for energy is already developed in the earlier section. However, the function only for power is considered here. If only long line swing is considered then power dissipation is given by

$$P = \Delta V_{bl} \left[ \frac{C_{bbl} \Delta V_{bl}}{T_k + T_{pc}} \right]$$

$$\therefore T_k + T_{pc} = C_{bbl} \left[ \frac{1.7 K_a}{W_a} + R_{bl} \frac{\Delta V_{bl}}{i} \right]$$
\[
\therefore P = \Delta V_{bl} \left[ \frac{\Delta V_{bl}}{1.7 K_a + R_{bl} + \frac{\Delta V_{bl}}{i}} \right]
\]

Differentiating w.r.t. \( \Delta V_{bl} \) and equating to zero, optimum value of \( \Delta V_{bl} \) is given by

\[
\Delta V_{bl} = 2i \left[ \frac{1.7 K_a}{W_a} + R_{bl} \right]
\]

If power is considered as

\[
P = \frac{C_{bb} \Delta V_{bl} [2V_{dd} - \Delta V_{bl}]}{T_R + T_{PC}}
\]

then putting \( T_R + T_{PC} \), power is given by

\[
P = \Delta V_{bl} \left[ \frac{2V_{dd} - \Delta V_{bl}}{1.7 K_a + R_{bl} + \frac{\Delta V_{bl}}{i}} \right] \tag{4.3}
\]

Let \( x = \frac{1.7 K_a}{W_a} + R_{bl} \), now differentiating w.r.t. \( \Delta V_{bl} \) and equating to zero,

\[
\Delta V_{bl} = i \left( \frac{1.7 K_a}{W_a} + R_{bl} \right) \left[ \frac{1.7 K_a}{W_a} + R_{bl} \right] \left[ \frac{1.7 K_a}{W_a} + R_{bl} \right] + 2V_{dd} - 1
\]

For 250 nm technology,

\[
\Delta V_{bl} = 9200i \left( 9200i \sqrt{9200i + 5} - 1 \right)
\]

Similarly if top up precharge time is not considered, then dissipation is given by

\[
P = \Delta V_{bl} \left[ \frac{2V_{dd} - \Delta V_{bl}}{1.7 K_a + R_{bl}} \right]
\]

It is minimum when \( V_{ddpc} = \frac{V_{dd}}{\sqrt{2}} \) \tag{4.4}
4.5 Results and Conclusions

As detailed in earlier sections, cost functions are developed; memory is designed accordingly and simulated. Simulation results are tabulated and compared in the form of charts. Summary of these results and inferences drawn are mentioned here.

Various performance parameters at $W_{aE}$ pertaining to cost function for energy are summarized in Table 4.1. Top up precharge dissipation ($P_{dpc}$) remains stable around $W_{aE}$. Total cells dissipation ($P_{dcells}$) reduces and remains stable around $W_{aE}$. Cell dissipation ($P_{dcell}$) also remains constant in this range. Leakage power ($P_{scells}$) goes on increasing as it is proportional to area of cell. Area penalty 1.75 times of without cost functional development is paid.

Performance parameters for cost function for time are summarized in Table 4.2. Power dissipation goes maximum as a price we pay for time optimization. Top up precharge dissipation increases with width of an access device as it is not related to the process of optimization. Power penalty paid is 6.09% while there is no area penalty because $W_{aT}$ is less than $W_a$.

Optimization processes have proved that device aspect ratios play vital role. Penalties are paid when optimizations are carried out for power and time. There is scope for novel ideas which will minimize dissipations with less penalties. Such ideas have been explored and experimented in the next chapters.

Table 4.1: Summary of performance parameters at $W_{aE}$

<table>
<thead>
<tr>
<th>Access device width</th>
<th>Performance parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_d$ ($\mu$W)</td>
</tr>
<tr>
<td>$W_{aE}$</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 4.2: Summary of performance parameters at $W_{aT}$

<table>
<thead>
<tr>
<th>Access device width</th>
<th>Performance parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_d$ ($\mu$W)</td>
</tr>
<tr>
<td>$W_{aT}$</td>
<td>147.5</td>
</tr>
</tbody>
</table>