Abstract

This paper presents a detailed analysis of the switching loss characteristics of various existing discontinuous PWM (DPWM) algorithms, which use only one zero state and advanced DPWM (ADPWM) algorithms which use only one zero state with active state division. These DPWM algorithms reduce the switching losses at any operating conditions when compared with conventional space vector PWM (CSVPWM). Moreover, to reduce the complexity involved in the conventional space vector approach, the proposed PWM algorithms are developed by using the concept of imaginary switching times. By analyzing the switching loss characteristics, the minimum switching loss PWM algorithms are developed for induction motor drives. The theoretical evaluation is validated through the numerical simulation studies.

Keywords: ADPWM, DPWM, MSLPWM, space vector PWM, switching loss characteristics.

1. Nomenclature

- $f_s$: Sampling frequency
- $f_{sw}$: Average switching frequency
- $E_{sub}$: Average switching energy loss per subcycle
- $V_{dc}$: DC link voltage
- $n_a$: Number of switchings per sampling time period in phase A
- $P_{sw}$: Normalized switching loss
- $\phi$: Power factor angle
- $\delta$: Phase-angle

2. Introduction

The variable speed induction motor drives require variable voltage, variable frequency voltages, which can be obtained by using the voltage source inverters (VSI). Hence, nowadays the PWM algorithms for VSI are becoming popular. A detailed survey on PWM algorithms is given in [1]. Among the various PWM algorithms the CSVPWM algorithm is popular due to its numerous advantages compared with the sinusoidal PWM [2]. By utilizing the division of zero state time, several DPWM algorithms can be generated and a detailed study about this is given in [3]. Recently, novel PWM algorithms have been developed which use only one zero state same as existing DPWM algorithms, but involve the division of active state time in every sampling time interval. These ADPWM algorithms can be generated with space vector approach very easily when compared with the triangle comparison approach [4]. A detailed analysis of these ADPWM algorithms has been given in [5]. But, in the recent years, the research is focussed on the analysis of the switching loss of the inverter. Several authors have proposed various methods for reduced switching loss of the inverter [6]-[9]. However, the above papers deal with the conventional space vector approach, which involves the calculation of angle and sector information. Hence, the complexity involved in the conventional space vector approach is more. To overcome this problem, few PWM algorithms have been developed in [10] by using the concept of imaginary switching times.

This paper presents different PWM algorithms using the concept of imaginary switching times. The
Proposed algorithm reduces the switching losses of the inverter. Also this presets the minimum switching loss PWM algorithms for induction motor drives.

Section 3 gives the details about the generation of various PWM algorithms. A detailed analysis on switching loss characteristics is given in section 4 for various PWM algorithms. Moreover, the minimum switching loss PWM algorithms are given in this section.

3. Switching Sequences

The proposed approach uses the instantaneous reference phase voltages only to calculate switching times. This method does not depend on the magnitude of the reference voltage space vector and its relative angle with respect to the reference axis. If the reference voltage vector lies in the first sector, then the actual switching times can be deduced as follows [10]:

\[ T_1 = \frac{T_s}{V_{dc}} V_{an} - \frac{T_s}{V_{dc}} V_{bn} = T_{an} - T_{bn} \]  
\[ T_2 = \frac{T_s}{V_{dc}} V_{bn} - \frac{T_s}{V_{dc}} V_{cn} = T_{bn} - T_{cn} \]

From the above expressions, the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages are defined as:

\[ T_{an} = \left( \frac{T_s}{V_{dc}} \right) V_{an} \]
\[ T_{bn} = \left( \frac{T_s}{V_{dc}} \right) V_{bn} \]
\[ T_{cn} = \left( \frac{T_s}{V_{dc}} \right) V_{cn} \]

Thus, the active voltage vector switching times can be represented by the time difference between the imaginary switching time periods. The switching times \( T_{an}, T_{bn} \) and \( T_{cn} \) could be negative when the instantaneous reference voltages are negative. Hence, these times are called as imaginary switching times. The active vector switching times can be calculated in each sampling interval as follows:

\[ T_{Max} = \text{Max}(T_{an}, T_{bn}, T_{cn}) \]
\[ T_{Min} = \text{Min}(T_{an}, T_{bn}, T_{cn}) \]
\[ T_{Mid} = \text{Mid}(T_{an}, T_{bn}, T_{cn}) \]

where Max, Min and Mid are the nominal values used during the sampling interval. The function \( \text{Max}(T_{an}, T_{bn}, T_{cn}) \) selects the maximum value among \( T_{an}, T_{bn} \) and \( T_{cn} \). Similarly \( \text{Min}(T_{an}, T_{bn}, T_{cn}) \) selects the minimum value and \( \text{Mid}(T_{an}, T_{bn}, T_{cn}) \) selects the middle value. Finally, the active state times \( T_1 \) and \( T_2 \) may be expressed as [10]

\[ T_1 = T_{Max} - T_{Mid} \]
\[ T_2 = T_{Mid} - T_{Min} \]  
\[ T_z = T_s - T_1 - T_2 \]

The zero voltage vectors switching time is calculated using (6).

The CSVPWM algorithm employs equal division of zero voltage vector time within a sampling time period. However, by utilizing the freedom of zero state time division, various discontinuous PWM (DPWM) algorithms can be generated. In the proposed PWM sequences the zero state time will be shared between two zero states as \( T_0 \) for \( V_0 \) and \( T_7 \) for \( V_7 \) respectively, and can be expressed as [6]

\[ T_0 = k_o T_z ; T_7 = (1-k_o) T_z \]

If \( k_o = 0.5, 0 \) and \( 1 \), then CSVPWM, DPWMMAX and DPWMMIN can be obtained respectively. When \( k_o = 0 \), any one of the phases is clamped to positive dc bus for 120 degrees over a fundamental interval and when \( k_o = 1 \), any one of the phases is clamped to negative dc bus for 120 degrees over a fundamental interval. Thus, in the first sector, CSVPWM uses 0127-7210 sequence, DPWMMAX uses 721-127 sequence and DPWMMIN uses 012-210 sequence. Various DPWM algorithms can be generated with step change of \( k_o \) between zero and one [3].

The above existing DPWM algorithms cannot switch more than once in every sampling time period. Hence, these can be generated with triangular comparison approach also. But in the proposed switching sequences, one of the phases will be clamped while the one of the other phases will switches twice in every sampling time interval. Hence these sequences also known as double-switching clamping sequences. Same as the existing DPWM algorithms, by changing \( k_o \) value and using the active state division, advanced DPWM algorithms can be generated. If \( k_o = 0 \) and \( 1 \), then ADPWMMAX and ADPWMMIN can be obtained respectively. The switching sequences pertaining to all six sectors for these PWM algorithms are listed in Table 1. Moreover, the Table 1 shows the clamping phase and double-switching phase also in every sector for ADPWMMIN and ADPWMMAX algorithms. The other ADPWM algorithms can be generated with step change of \( k_o \) between zero and one as given in [3]. The following Tables will
give the comparison between the existing DPWM and ADPWM algorithms. After examining the all possible advanced DPWM (ADPWM) algorithms, it can be observed that in each ADPWM algorithm though one of the phases switches twice in a sampling time interval the total number of commutations per subcycle is only three. This is same as the CSVPWM algorithm. Hence the sampling frequency of the CSVPWM and ADPWM algorithms is the twice the average switching frequency \( f_s = 2f_{sw} \), whereas the sampling frequency of the existing DPWM algorithms is three times the average switching frequency \( f_s = 3f_{sw} \).

4. Switching Loss Characteristics
The switching losses of a pulse width modulated VSI fed induction motor drive are load dependent and increase with the current magnitude. The switching losses of the inverter also depend on type of PWM method. With continuous PWM methods, all the three phase currents are commutated within each carrier cycle of a full fundamental cycle. Therefore, for all continuous PWM methods the switching losses are the same and independent of the load power factor angle. However, with the DPWM methods, the switching losses are significantly influenced by the type of modulation method and load power factor angle.

### Table 1: ADPWMMAX and ADPWMMIN sequences in all six sectors

<table>
<thead>
<tr>
<th>Sector</th>
<th>ADPWMMIN</th>
<th>ADPWMMAX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>sequence</td>
<td>Clamping phase</td>
</tr>
<tr>
<td>I</td>
<td>0121-1210</td>
<td>c</td>
</tr>
<tr>
<td>II</td>
<td>0323-3230</td>
<td>c</td>
</tr>
<tr>
<td>III</td>
<td>0343-3430</td>
<td>a</td>
</tr>
<tr>
<td>IV</td>
<td>0545-5450</td>
<td>a</td>
</tr>
<tr>
<td>V</td>
<td>0565-5650</td>
<td>b</td>
</tr>
<tr>
<td>VI</td>
<td>0161-1610</td>
<td>b</td>
</tr>
</tbody>
</table>

### Table 2: Switching sequences for DPWM0 and ADPWM0

<table>
<thead>
<tr>
<th>Sector</th>
<th>DPWM0</th>
<th>ADPWM0</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>012-210</td>
<td>0121-1210</td>
</tr>
<tr>
<td>II</td>
<td>723-327</td>
<td>7232-2327</td>
</tr>
<tr>
<td>III</td>
<td>034-430</td>
<td>0343-3430</td>
</tr>
<tr>
<td>IV</td>
<td>745-547</td>
<td>7454-4547</td>
</tr>
<tr>
<td>V</td>
<td>056-650</td>
<td>0565-5650</td>
</tr>
<tr>
<td>VI</td>
<td>761-167</td>
<td>7616-6167</td>
</tr>
</tbody>
</table>

### Table 3: Switching sequences for DPWM2 and ADPWM2

<table>
<thead>
<tr>
<th>Sector</th>
<th>DPWM2</th>
<th>ADPWM2</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>721-127</td>
<td>7212-2127</td>
</tr>
<tr>
<td>II</td>
<td>032-230</td>
<td>0323-3230</td>
</tr>
<tr>
<td>III</td>
<td>743-347</td>
<td>7434-4347</td>
</tr>
<tr>
<td>IV</td>
<td>054-450</td>
<td>0545-4545</td>
</tr>
<tr>
<td>V</td>
<td>765-567</td>
<td>7656-6567</td>
</tr>
<tr>
<td>VI</td>
<td>016-610</td>
<td>0161-1610</td>
</tr>
</tbody>
</table>

### Table 4: Switching sequences for DPWM1 and ADPWM1:

<table>
<thead>
<tr>
<th>Sector</th>
<th>DPWM1</th>
<th>ADPWM1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 ≤ α ≤ 30°</td>
<td>30° ≤ α ≤ 60°</td>
</tr>
<tr>
<td>I</td>
<td>721-127</td>
<td>012-210</td>
</tr>
<tr>
<td>II</td>
<td>032-230</td>
<td>723-327</td>
</tr>
<tr>
<td>III</td>
<td>743-347</td>
<td>034-430</td>
</tr>
<tr>
<td>IV</td>
<td>054-450</td>
<td>745-547</td>
</tr>
<tr>
<td>V</td>
<td>765-567</td>
<td>056-650</td>
</tr>
<tr>
<td>VI</td>
<td>016-610</td>
<td>761-167</td>
</tr>
</tbody>
</table>
In the DPWM methods, the devices are clamped to either negative bus or positive bus for a total of 120° and hence reduce the switching losses of inverter over continuous PWM methods. Hence, in DPWM algorithms, the load power factor and the modulation method together determine the time interval that the load current is not commutated. Therefore, it is necessary to derive the switching loss characteristics to compare the switching losses of various DPWM algorithms. This section presents a comparison of inverter switching losses due to conventional SVPWM and DPWM methods.

The switching loss in an IGBT depends mainly on the dc link voltage ($V_{dc}$) instantaneous line current and turn-on and turnoff times. However, the $V_{dc}$ and times are assumed to be constant for different instantaneous line currents. Hence, to study the switching losses of the inverter, it is sufficient to consider the product of instantaneous line current magnitude of a particular phase and the number of switchings per sampling time period in that phase ($n_a$), corresponding to the PWM sequence considered. This product is referred to as the switching loss factor (SLF). Since the three phases are symmetric, it is enough to analyze one phase only. The switching losses of a PWM-VSI induction motor drive can be modeled analytically by assuming linear current turn-on and turn-off characteristics with respect to time for the inverter switching devices and considering only fundamental component of the load current. Let the phase current is

$$i_a = I_{max} \sin(\omega t - \phi)$$  \hspace{1cm} (8)

where $i_a$ is the instantaneous fundamental phase current, $I_{max}$ is the maximum value of the fundamental phase current and $\phi$ is the line side power factor angle. The average switching energy loss per subcycle ($E_{sub}$) in an inverter leg is as given by

$$E_{sub(avg)} = \frac{1}{\pi} \int_0^{\pi} n_a I_{max} \sin(\omega t - \phi) d(\omega t)$$

$$= \frac{1}{\pi} \int_0^{\pi} n_a [\sin(\omega t - \phi)]d(\omega t)$$  \hspace{1cm} (9)

To obtain the measure of the inverter switching losses, the average switching energy loss per subcycle must be multiplied by the number of subcycles per second, i.e., the sampling frequency ($f_s$). The sampling frequency of the CSVPWM and ADPWM algorithms is two times the switching frequency ($f_{sw}$), while it is three times the switching frequency ($f_{sw}$) for the existing DPWM methods. The average switching energy loss over a fundamental cycle for CSVPWM equals ($2/\pi$). The normalized switching loss due to given PWM algorithm can be obtained as given in (10).

$$P_{sw} = \frac{E_{sub(avg)} f_s}{(2\pi)}$$  \hspace{1cm} (10)

From (10), the normalized switching loss due to existing DPWM methods can be obtained and given in (11).

$$P_{sw} = \frac{3\pi}{4} E_{sub(avg)}$$  \hspace{1cm} (11)

By observing the DPWM0, DPWM1 and DPWM2 modulating waveforms, it can be given that there is a 30° phase-angle ($\delta$) distance between their dc-link clamped 60° segments. Hence, a new PWM algorithm can be introduced as generalized DPWM (GDPWM) algorithm which covers the DPWM0, DPWM1 and DPWM2 algorithms. The $\delta$ and $\phi$ dependent switching phase current and normalized switching energy loss per subcycle waveforms of GDPWM algorithm is shown in Fig.1. The GDPWM

<table>
<thead>
<tr>
<th>Sector</th>
<th>DPWM3</th>
<th>ADPWM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>012-210</td>
<td>721-127</td>
</tr>
<tr>
<td>II</td>
<td>723-327</td>
<td>032-230</td>
</tr>
<tr>
<td>III</td>
<td>034-430</td>
<td>743-347</td>
</tr>
<tr>
<td>IV</td>
<td>745-547</td>
<td>054-450</td>
</tr>
<tr>
<td>V</td>
<td>056-650</td>
<td>765-567</td>
</tr>
<tr>
<td>VI</td>
<td>761-167</td>
<td>016-610</td>
</tr>
</tbody>
</table>
algorithm can be represented by using space vector as shown in Figure 2. For $\delta = 0^\circ$, $30^\circ$ and $60^\circ$, DPWM0, DPWM1 and DPWM2 algorithms can be obtained respectively. The variation of average switching energy loss per subcycle ($E_{avg}$) over a fundamental cycle for various DPWM algorithms for different values of $\delta$ and $\phi$ is shown in Figure 3- Figure 6. From these, it can be observed that at unity power factor DPWM1 clamps a phase around its current peak, which leads to a significant reduction in $E_{avg}$ over the remaining DPWM and conventional SVPWM algorithms. Therefore, the switching loss mainly depends on the power factor angle by which the line current lags/leads the line voltage. Moreover, it may be observed that the effect of different PWM sequences on the switching loss does not depend on $V_{ref}$ or the fundamental frequency.

Figure 1: the average switching loss of GDPWM

Figure 2: space vector illustration of GDPWM algorithm

From Figure 3 – Figure 6, the expressions for normalized inverter switching loss corresponding to different DPWM algorithms can be derived as given in [3]. The variation of normalized switching loss of different DPWM algorithms with power factor angle (both at lagging and leading) is shown in Figure 7.
Figure 4(b)
Figure 4: Variation of normalized switching energy loss for DPWM1 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

Figure 5 (a)
Figure 5 (b)
Figure 5: Variation of normalized switching energy loss for DPWM2 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

From Fig.7, it can be found that the DPWM1 gives minimum switching loss at unity power factor, because DPWM1 clamps at peak phase current at unity power factor. Similarly, DPWM0 and DPWM2 give minimum switching losses at $30^\circ$ leading and lagging power factors respectively. But, DPWM3 gives minimum switching loss near the zero power factor. The value of $\delta$ can be varied in accordance with $\phi$ to achieve reduction in switching losses.

Figure 6 (b)
Figure 6: Variation of normalized switching energy loss for DPWM3 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

The minimum switching power loss solution of the DPWM0, DPWM1 and DPWM2 yields to GDPWM algorithm. The optimal solution of GDPWM is obtained by selecting $\delta = (\pi/6) + \phi$ for $-\pi/6 \leq \delta \leq \pi/6$. Outside this range $\delta = 60^\circ$ for lagging power factor angle and $\delta = 0^\circ$ for leading power factor angle. The normalized switching loss variations for different DPWM algorithms and GDPWM algorithm are shown in Fig. 8. This shows that the GDPWM algorithm combines the DPWM0 and DPWM1 and DPWM2 algorithms and also gives less switching loss. The GDPWM does not consist of DPWM3 algorithm. But from Fig.7, it can be observed that the DPWM3 gives minimum switching losses outside the $-(5\pi/12) \leq \phi \leq (5\pi/12)$ range. In this paper, by considering DPWM3, the minimum switching loss PWM (MSLPWM) algorithm with
existing DPWM algorithms is proposed. The variations of normalized switching losses of various DPWM algorithms and proposed minimum switching loss PWM (MSLPWM) algorithm are shown in Figure 9. The comparison between GDPWM and proposed MSLPWM is shown in Figure 10.

![Figure 8](image)

Figure 8: The variation of normalized switching loss of different DPWM algorithms with power factor angle (A: DPWM0; B: DPWM1; C: DPWM2; D: DPWM3 and E=GDPWM)

Similar to the existing DPWM algorithms, the switching loss analysis of ADPWM algorithms can be carried out. The normalized switching loss due to ADPWM algorithm can be obtained same as previous chapter and given by

\[ P_{sw,ADPWM} = \frac{\pi}{2} E_{sub}(avg) \]  (12)

![Figure 9](image)

Figure 9: The variation of normalized switching loss of different DPWM algorithms with power factor angle (A: DPWM0; B: DPWM1; C: DPWM2; D: DPWM3 and E=MSLPWM)

The modulating waveforms of ADPWM0, ADPWM1, ADPWM2 and ADPWM3 are similar to corresponding existing DPWM algorithms. Hence, same as existing DPWM0, DPWM1 and DPWM2 algorithms, there is a 30° phase-angle (\( \delta \)) distance between their dc-link clamped 60° segments in the ADPWM0, ADPWM1 and ADPWM2 modulating waveforms also. Hence, a new PWM algorithm can be introduced as advanced generalized DPWM (AGDPWM) algorithm which covers the ADPWM0, ADPWM1 and ADPWM2 algorithms. The variation of average switching energy loss per subcycle (\( E_{sub} \)) over a fundamental cycle for various ADPWM algorithms for different values of \( \delta \) and \( \phi \) is shown in Figure 11 - Figure 14.

![Figure 10](image)

Figure 10: The variation of normalized switching loss of GDPWM (A) and MSLPWM (B) algorithms

At the same time ADPWM3 is not effective in reducing the switching energy loss at unity power factor. At zero power factor lagging, ADPWM3 reduces the \( E_{sub(avg)} \). Thus, both in existing as well as advanced DPWM algorithms, DPWM1 and ADPWM1 are better in terms of switching losses at power factors close to unity, while DPWM3 and ADPWM3 are better at power factors close to zero. From Figure 11 – Figure 14, the expressions for
normalized inverter switching loss corresponding to different ADPWM algorithms can be derived as given in [8]. The variation of normalized switching loss of different ADPWM algorithms with power factor angle (both at lagging and leading) is shown in Figure 15.

Figure 12: Variation of normalized switching energy loss for ADPWM1 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

Figure 13 (a): Variation of normalized switching energy loss for ADPWM2 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

Figure 14 (a): Variation of normalized switching energy loss for ADPWM3 method: (a) $\phi = 0^\circ$ (b) $\phi = 30^\circ$

Figure 15: The variation of normalized switching loss of different ADPWM algorithms with power factor angle (A: ADPWM0; B: ADPWM1; C: ADPWM2 and D: ADPWM3)
From Figure 15, it can be observed that the ADPWM1 gives minimum switching loss at unity power factor, because ADPWM1 clamps at peak phase current at unity power factor. Similarly, ADPWM0 and ADPWM2 give minimum switching losses at 30° leading and lagging power factors respectively. But, ADPWM3 gives minimum switching loss near the zero power factors. The value of $\delta$ can be varied in accordance with $\phi$ to achieve reduction in switching losses. The minimum switching power loss solution of the ADPWM0, ADPWM1 and ADPWM2 yields to AGDPWM algorithm. The optimal solution of AGDPWM is obtained by selecting $\delta = (\pi/6) + \phi$ for $-\pi/6 \leq \phi \leq \pi/6$. Outside this range $\delta = 60^o$ for lagging power factor angle and $\delta = 0^o$ for leading power factor angle. The normalized switching loss variations for different ADPWM algorithms and AGDPWM algorithm are shown in Fig. 16. This shows that the AGDPWM algorithm combines the ADPWM0 and ADPWM1 and ADPWM2 algorithms and also gives less switching loss.

The AGDPWM does not consist of ADPWM3 algorithm. But from Fig.15, it can be observed that the ADPWM3 gives minimum switching losses outside the $-5\pi/12 \leq \phi \leq 5\pi/12$ range. In this paper, by considering ADPWM3 also into account advanced minimum switching loss PWM (AMSLPWM) algorithm with ADPWM algorithms is proposed. The variations of normalized switching losses of various ADPWM algorithms and proposed AMSLPWM algorithm are shown in Fig. 17. The comparison between AMSLPWM and MSLPWM is shown in Fig. 18. From Fig 18, it can be observed that the proposed AMSLPWM algorithm gives minimum switching loss over the MSLPWM in the $-(\pi/6) \leq \phi \leq (\pi/6)$ range. At the same time, MSLPWM algorithm gives minimum switching losses outside the $-(\pi/6) \leq \phi \leq (\pi/6)$ range.

5. Conclusions
Space vector based minimum switching loss PWM algorithms are presented in this paper. The proposed algorithms did not use the information regarding sector and angle calculation of switching times and hence reduces the complexity involved. The minimum switching loss PWM algorithms are derived using existing DPWM and ADPWM algorithms and compared. From the results, it can be observed that AMSLPWM algorithm gives minimum switching loss over the MSLPWM in the $-(\pi/6) \leq \phi \leq (\pi/6)$ range. At the same time, MSLPWM algorithm gives minimum switching losses outside the $-(\pi/6) \leq \phi \leq (\pi/6)$ range.

6. References


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