CHAPTER 4

APPLICATIONS OF QUASI FLOATING-GATE MOS TRANSISTOR

4.1 Introduction

There are certain limitations in implementing the analog circuits at low supply voltages. The gate to source voltage applied to the MOSFET must be higher than the threshold voltage \((V_T)\) of the MOSFET to turn it ON in order to perform any type of signal processing. The large value of \(V_T\) ensures better noise immunity whereas the lower value of \(V_T\) makes the signal to noise ratio small. It has been observed that the threshold voltage of the MOSFET is not expected to scale down in proportion to supply voltage for future sub-micron technologies due to off-state currents in logic circuits and the related power consumption. The channel length modulation effect becomes prominent with reduced features which results in poor signal gains because of the reduced small-signal output resistance of the MOSFETs. Although, floating-gate MOSFET (FGMOS) provides solution to these problems due to tunability of threshold voltage without the need of actually lowering the threshold voltage, yet it exhibits certain limitations like isolated floating-gate which may accumulate static charge, low frequency response and need of large chip area [34, 43]. However, these limitations can be further overcome by Quasi Floating-Gate MOSFET (QFGMOS).

Current mirrors form the core structures of almost all analog and mixed-mode circuits and their characteristics largely decide the performance of analog structures [110-116]. Current mirrors (CMs) have been used as current references and as a means of transferring signals. The use of current mirror in biasing circuits yield better
insensitivity of the circuit performance with regard to the variation in power supply and
temperature. CMs have also been used as active loads for high voltage gain resulting in
smaller chip area [17]. Other applications of CMs include their use as building blocks in
voltage buffers, bidirectional current mirrors, current conveyors, current controlled
conveyors etc. [19, 23, 38].

A current mirror is a circuit designed to accept the input signal in current form at
low impedance and produce the copy of the input signal with its scaled version at the
output terminal with high output impedance. Conceptually, an ideal current mirror is
simply a current amplifier. CMs can be designed using bipolar transistors and
MOSFETs. CMs based on MOSFETs have better accuracy than bipolar CMs and are
more insensitive to process variations. However, in short channel length MOSFETs, the
performance of CMs gets constrained due to small voltage gain and low supply voltage.
Moreover, the presences of non-idealities in the CM characteristics also affect the
performance of the analog circuits.

Ideally, a current mirror should have a unity current transfer ratio which
precisely depend on the dimensions of MOSFET and be independent of temperature.
The output resistance of the current mirror should be very high so it acts as ideal current
source with its output current independent of output voltage. It should have low input
resistance ($R_{in}$) and small voltage drop at the input node which results in low input
compliance voltage suitable for low voltage applications. For maximum voltage swing
at the output terminal a current mirror should have low output compliance voltage.
Moreover, a current mirror must exhibit wide bandwidth for high frequency
applications. Therefore, alternate design techniques need to be investigated for high
performance CMs at low supply voltage using QFGMOS.
The passive components like resistors also play a significant role in integrated circuits as their direct integration need more chip area for higher values. So, implementation of active resistors in integrated circuits is desired for minimal chip area and high accuracy. A MOS transistor operating below saturation region can implement a voltage controlled resistor (VCR) but with a limited range. These VCRs are useful in the design of tunable analog circuits like voltage controlled oscillators, automatic gain controllers, voltage controlled filters, current-mode dividers, trans-resistance amplifiers etc. [117-120]. The literature survey reveals the design of tunable active resistors using FGMOS [118,121]. Since, FGMOS based circuits inherit some limitations to downgrade the performance of circuits, therefore, it is expected that the QFGMOS based VCR would exhibit better characteristics as compared to its FGMOS version.

### 4.2 Simple Current Mirror

A simple current mirror consists of two MOSFETs as shown in Fig. 4.1 where M1 is diode connected and provides gate bias to M2.

![Simple Current Mirror Diagram](image)

Fig. 4.1 Simple current mirror

This circuit is basically a current amplifier which reproduces the scaled versions of the input current at its output terminal. The current mirror uses the principle that if the gate to source voltages of two MOSFETs are made equal, then their drain currents would
also become equal. Here, input current is fed into M1 which gets biased into the saturation region being diode connected as \( V_{DS1} = V_{GS1} \) and generates a gate bias both for M1 and M2, i.e. \( V_{GS1} = V_{GS2} = V_{GS} \). Thus, M2 has a gate voltage sufficient to bias it into saturation region too on application of a proper drain to source bias such that \( V_{DS2} \geq (V_{GS2} - V_T) \). It exhibits the properties of an ideal current source at the output terminal since M2 works in saturation region and thus, provides a constant drain current which is almost independent of its drain to source voltage. Therefore, current mirror has infinite output resistance.

Now, the current transfer function of the current mirror which is defined as the ratio of the output current or the mirrored current \( I_{\text{out}} \) to the input current \( I_{\text{in}} \), is given by [15, 17, 109]:

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \left( \frac{LW_2}{W_1L_2} \right) \left( \frac{V_{GS} - V_T}{V_{GS} - V_{T1}} \right)^2 \left[ 1 + \lambda \left( \frac{K'}{K_1} \right) \right]
\]

(4.1)

where \( V_T \) is the threshold voltage, \( \lambda \) is the channel length modulation parameter, \( W \) is the channel width, \( L \) is the channel length, \( K' = \mu C_{OX} \) is the transconductance parameter and other symbols have their usual meaning. The parameters \( V_T \) and \( K' \) are identical for both M1 and M2 as they are fabricated on the same substrate. As a result, Eq. (4.1) simplifies to:

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \left( \frac{LW_2}{W_1L_2} \right) \left( 1 + \lambda V_{DS2} \right) \left( 1 + \lambda V_{DS1} \right)^{-1}
\]

(4.2)

Now if \( V_{DS2} = V_{DS1} \) then Eq. (4.2) further reduces to:

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \left( \frac{W_2/L_2}{W_1/L_1} \right)
\]

(4.3)
Thus, the current transfer function is a function of aspect ratios which can be selected accordingly to the application.

Since, the input terminal of current mirror facilitates the input signal in current form therefore it must present a minimum input resistance. However, due to non-idealities present in transistors and short channel effects, there is some minimum value of input voltage referred to as input compliance voltage and non-zero input resistance, which are given as [109]:

\[ V_{\text{in}} \text{ (min)} = V_{DS1 \text{ (sat)}} + V_{T1} \]  \hspace{1cm} (4.4)

\[ r_{\text{in}} = \frac{1}{g_{m1}} \] \hspace{1cm} (4.5)

Similarly, the current mirror also exhibit non ideal behaviour at its output terminal due to lapse of certain drain to source voltage before it enters into saturation region which is referred to as output compliance voltage and is given as:

\[ V_{\text{out}} \text{ (min)} = V_{DS2 \text{ (sat)}} \] \hspace{1cm} (4.6)

Further, the output resistance is also not infinite due to short channel effects and is given by:

\[ r_{\text{out}} = \frac{1}{g_{d2}} = \frac{1}{\lambda J_{D2}} \] \hspace{1cm} (4.7)

We can see that for a given process, output resistance can be increased by increasing the length of the device, but it increases the output capacitance also which degrades the frequency response of the current mirror. Therefore, there is always a tradeoff between output resistance and output capacitance.
4.3 FGMOS Current Mirror

A current mirror (CM) being a fundamental building block in analog signal processing circuits should be capable of operating with low supply voltage while dissipating low power. Since, the effective threshold voltage of FGMOS can be reduced by applying a bias voltage at one of its gate terminals, the current mirror based on FGMOS will require less operating voltage as compared to CM based on conventional MOSFETs. The circuit of a simple FGMOS based current mirror is shown in Fig. 4.2.

![Fig. 4.2 Simple FGMOS CM](image)

It employs a two input FGMOS M1 where one of the input gate terminals is used to apply a bias voltage \( V_{bias} \) through a large capacitance \( C_2 \) and other input gate terminal is used for signal processing. Though this implementation offers threshold voltage tunability for low voltage applications, but it demands more silicon area with reduced effective transconductance and gain bandwidth product due to large biasing capacitance [122]. Therefore, the performance of this CM can be further enhanced if we employ QFGMOS in place of FGMOS.

4.4 QFGMOS Based Current Mirror

Due to advantages of QFGMOS over FGMOS, the implementation of CM using QFGMOS would be more suitable for low voltage applications [97]. A simple CM based on QFGMOS is shown in Fig. 4.3 where M1 is diode connected through \( C_1 \) and
the gates of M1 and M2 are weakly connected to the supply voltage through a high value resistor realized by M3. We may observe that, there is no need of bias voltage through a large capacitance as required in FGMOS current mirror.

![Fig. 4.3 Simple QFGMOS CM](image)

The large-signal behavior of simple QFGMOS CM is identical to that of a conventional and FGMOS CMs. However, the small-signal behavior would differ owing to the presence of capacitance $C_1$ and MOS resistor M3. Therefore, we have performed the hybrid ($h$) parameter analysis of the QFGMOS CM to obtain the functional relationship between the input and output variables. The detailed analysis is presented in Appendix B [Eqs. (B.12), (B.13), (B.8) & (B.14)] and the resultant $h$ parameters of the simple QFGMOS CM are given below [19, 23,123].

\[
\begin{align*}
    h_{11} &= \left. \frac{V_{in}}{I_{in}} \right|_{V_{in}=0} = \frac{\left[1 + \frac{G' + sC}{sC_A} \right]}{(g_{m1} + g_{d1}) \left[1 + \left(\frac{g_{d1} + sC_A}{g_{m1} + g_{d1}}\right) \left(\frac{G' + sC}{sC_A}\right)\right]} \\
    h_{12} &= \left. \frac{V_{in}}{I_{in}} \right|_{V_{in}=0} = 0
\end{align*}
\]

where we have assumed $C_{GS} = C_{GB} = C$, $C_A = C_1 + C_{GD}$ and $G' = gd_3 + 3sC$.

\[
\begin{align*}
    h_{11} &= \left. \frac{V_{in}}{I_{in}} \right|_{V_{in}=0} = \frac{\left[1 + \frac{G' + sC}{sC_A} \right]}{(g_{m1} + g_{d1}) \left[1 + \left(\frac{g_{d1} + sC_A}{g_{m1} + g_{d1}}\right) \left(\frac{G' + sC}{sC_A}\right)\right]} \\
    h_{12} &= \left. \frac{V_{in}}{I_{in}} \right|_{V_{in}=0} = 0
\end{align*}
\]
\[ h_{21} = \left. \frac{I_{\text{out}}}{I_{\text{in}}} \right|_{V_{\text{in}}=0} = \frac{g_{m2}}{(g_{m1} + g_{d1}) + (g_{d1} + sC_A) \left( \frac{G' + sC}{sC_A} \right)} \]  

\[ h_{22} = \left. \frac{I_{\text{out}}}{V_{\text{out}}} \right|_{I_{\text{in}}=0} = \frac{V_{\text{out}} g_{d2} + V_{\text{out}} sC_{GD}}{V_{\text{out}}} = g_{d2} + sC \]  

From Eq. (4.11), we find that the output impedance of simple QFGMOS CM is given by

\[ \frac{r_{d2}}{1 + sC r_{d2}}. \]

This circuit is now expected to exhibit a better frequency response due to elimination of large capacitor used for applying bias voltage as required in FGMOS CM [34, 43]. This fact has been demonstrated by simulating the circuit of Fig. 4.3 and its FGMOS counterpart (Fig. 4.2) using level 7 PSpice parameters of 0.13 \( \mu \text{m} \) CMOS technology with supply voltage of \( \pm 0.5 \text{ V} \) by choosing \( W/L \) ratios for M1 and M2 as 7.8 \( \mu \text{m}/0.26 \mu \text{m} \) and 78 \( \mu \text{m}/0.26 \mu \text{m} \) for M3. The comparative frequency response as shown in Fig. 4.4 exhibits a bandwidth of 8.37 GHz for QFGMOS CM and 2.03 GHz for FGMOS CM.

![Fig. 4.4 Comparative frequency response](image-url)
Similarly, the input compliance voltage of QFGMOS CM (0.3 V) has also been found to be less than that of FGMOS CM (0.7 V) at an input current of 500 µA as shown in Fig. 4.5.

Fig. 4.5 Comparative input characteristics

4.5 Bandwidth Enhancement in QFGMOS CM

The high frequency application of mixed-mode low voltage circuits is usually limited by the speed of the analog sub-circuits. Though QFGMOS based CMs offer better frequency response as compared to FGMOS CMs while retaining other advantages suitable for low voltage design, yet the bandwidth may not be sufficient for some high frequency applications like high speed processors and video processing. Therefore, some bandwidth enhancement techniques must be developed for QFGMOS based CMs in order to improve upon its inherit bandwidth.

We have observed that the frequency response of QFGMOS based CM of Fig.4.3 can be further improved by adding a resistance $R$ in series with the capacitance $C_1$ as shown in Fig. 4.6 (a) [43, 124-126].
Fig. 4.6 (a) Modified QFGMOS CM with passive $R$

Now the $R$ in Fig. 4.6 (a) can be replaced by a MOSFET as desired for integration. The modified QFGMOS CM with active $R$ as shown in Fig. 4.6 (b).

We have also performed the small-signal analysis of the modified QFGMOS CM using $h$ parameters. The detailed analysis is presented in Appendix C and the expression for the transfer function (T.F.) obtained using $h_{21}$ is given by:

$$H(s) = \frac{g_{m2} \left[ s + \left( \frac{C + C_1}{2RC_1} \right) \right]}{s^2 \left( \frac{3C^2}{2C_1} + 2C_1 + \frac{7}{2}C \right) + s \left( \frac{2C^2}{RC_1} + \frac{3C_1}{R} + \frac{5C}{2} + g_{m1}C + g_{m1} \frac{C^2}{C_1} \right) + \left( \frac{g_{m1}}{2RC_1} + \frac{g_{m1}}{2RC} \right)}$$

(4.12)

where we have assumed $C_{GD} = C_{GS} = C$ and $g_{d1}, g_{d2}$ & $g_{d3}$ are ignored by assuming transistors in saturation region with infinite small-signal output resistance.
Now Eq. (4.12) can be written simply as:

$$H(s) = \frac{g_m^2 \left[ s + \left( \frac{C + C_1}{2RC_1} \right) \right]}{s^2 X + sY + \left( \frac{g_m}{2RC_1} + \frac{g_m}{2RC} \right)}$$

(4.13)

where $X = \left( \frac{3C^2}{2C_1} + 2C_1 + \frac{7}{2} C \right)$ and $Y = \left( \frac{2C^2}{RC_1} + \frac{3C_1}{R} + \frac{5C}{2} + \frac{g_mC}{2} + \frac{C^2}{C_1} \right)$

We may observe that the T.F. given in Eq. (4.13) has a zero at $s = -\frac{C + C_1}{2RC_1}$ and a pair of poles given by:

$$P_{1,2} = \frac{Y \pm \sqrt{Y^2 - 4X \left( \frac{g_m}{2RC_1} + \frac{g_m}{2RC} \right)}}{2X}$$

(4.14)

Now, the location of poles depends on the value of $R$ as shown in Eq. (4.14). For very high value of $R$, the poles and the zero moves towards the origin and one of the poles cancel out with the zero at a certain high value of $R$. The optimum value of $R$ at which a pole vanishes is given by:

$$R = \frac{2X g_m \left[ C + C_1 \right]}{g_m^2 C^2 \left[ \frac{1}{4} + \frac{C^2}{C_1^2} + \frac{C}{C_1} \right]}$$

(4.15)

The cancellation of pole with zero at a certain value of $R$ [Eq. 4.15] results in first order system, thus making the frequency response better. Now, the resulting single pole function, obtained by assuming infinitely large value of $R$ in Eq. (4.13) is given by:
\[ H(s) = \frac{g_m}{\left( \frac{3C^2}{2C_1} + 2C_1 + \frac{7}{2}C \right) s + \frac{g_m C}{2} + \frac{g_m C^2}{C_1}} \]  

(4.16)

where we have assumed \( g_{m1} = g_{m2} = g_m \). The transfer function given by Eq. (4.16) has a single pole located at \( s = -\frac{\frac{g_m C}{2} + \frac{g_m C^2}{C_1}}{\frac{3C^2}{2C_1} + 2C_1 + \frac{7}{2}C} \).

The simulated frequency response of the modified QFGMOS CM in Fig. 4.6 (a) for different values of \( R \) is shown in Fig. 4.7. We have observed the bandwidth without resistive compensation as 8.19 GHz which increases to 17.39 GHz when \( R \) is increased to 1 kΩ and afterwards, it saturates. The further increase in the value of \( R \) gives rise to peaks in frequency response and makes the system oscillatory and unstable. The similar effect has been observed in the simulation results of circuit of Fig. 4.6 (b) where M4 presents different resistance when its dimensions are varied.

Fig. 4.7 Frequency response with different values of resistance
4.6 QFGMOS Based Low Voltage Current Mirror

A low voltage CM (LVCM) based on QFGMOS has been obtained as shown in Fig. 4.8 by enhancing the characteristics of simple QFGMOS CM of Fig. 4.3. In order to reduce the input compliance voltage of the QFGMOS based LVCM, M11 is used as level shifter which receives the required bias current through M10 [4]. The output current is obtained from the drain of M5 which is biased using transistors M6 connected as a diode. M7, M8 and M10 form a current mirror arrangement to provide the scaled version of the input current.

The output resistance of the current mirror is further enhanced by using M9 which forms a self-cascode structure with M2. Here M2 and M9 act as composite transistor such that M9 operates in saturation region whereas M2 works in linear region and acts as resistor whose resistance depends on the input voltage [127-128].

The $h$ parameters of this circuit have been evaluated in Appendix D and the transfer function (T.F.) obtained using $h_{21}$ is given as:

![Fig. 4.8 QFGMOS based LVCM](image-url)
\[
H(s) = \frac{g_{m2}}{5C \left(1 + \frac{C}{(2C + C_i)} \right) s + \frac{g_{m1}}{5C \left(1 + \frac{C}{(2C + C_i)} \right)}} 
\]

(4.17)

where we have assumed \(C_{GD} = C_{GS} = C\) and \(g_{d1}, g_{d2} & g_{d3}\) are ignored by assuming transistors in saturation region having infinite small signal output resistance. The transfer function given by Eq. (4.17) has a zero at infinity and a pole given by:

\[
s = -\frac{g_{m1}}{5C \left(1 + \frac{C}{(2C + C_i)} \right)} 
\]

(4.18)

The output impedance \((Z_0)\) of QFGMOS based LVCM can be given by [Eq. (D.9)]

\[
Z_0 = \frac{\left[r_{d5} + r_{q9} \left[1 + 3sC_{r_{d2}} \right] + \left[g_{m9}r_{d2}r_{d9} + r_{d2} \left[2sC_{r_{d5}} + g_{m5}r_{d5} + 1 \right] \right] \right]}{1 + sC \left[\left(3r_{d2} + r_{d5} + 3sC_{r_{d2}r_{d5}} \right) + \left(r_{q9} + 3sC_{r_{d2}r_{d9}} + g_{m9}r_{d2}r_{d9} + r_{d2} \left[3 + 2sC_{r_{d5}} + g_{m5}r_{d5} \right] \right) \right]}
\]

(4.19)

At low frequencies Eq. (4.19) reduces to:

\[
Z_0 = r_{d2} + r_{d5} \left(1 + g_{m5}r_{d2} \right) + r_{d9} \left[1 + g_{m9} \left(r_{d2} \left(1 + g_{m5}r_{d5} \right) \right) \right] + g_{m5}r_{d5}
\]

(4.20)

### 4.6.1 Simulation Results

The LVCM of Fig. 4.8 has been simulated by selecting aspect ratios of M1 and M2 as 7.8 µm/0.26 µm, 0.13 µm/0.13 µm for M3, 0.39 µm/0.65 µm for M4, 91 µm/0.52 µm for M5, 1.3 µm/0.26 µm for M6, 78 µm/0.26 µm for M7, 91 µm/0.52 µm for M8, 45.1 µm/0.13 µm for M9 and 0.78 µm/0.78 µm for M10 and M11. The I-V characteristics of the QFGMOS based LVCM are shown in Fig. 4.9. The offset current is found to be 2.2 nA.
The current transfer ratio is observed as 0.98 with error in current transfer varying from 13.5% (for input currents below 100 $\mu$A) to 3.6% (for $I_{in} = 100 \mu$A) and it further decreases to –1.8% (for $I_{in} = 500 \mu$A) as shown in Figs. 4.10 & 4.11 respectively.
The input compliance voltage of the QFGMOS based LVCM has been found to be less by 0.1 V as compared to simple QFGMOS CM at input current of 500 µA (Fig. 4.12). The circuit offers an input resistance of 235 Ω, output resistance of 117 kΩ and consumes 0.83 mW power.

The dependence of output resistance ($R_{out}$) of the QFGMOS based LVCM on $I_{in}$ is shown in Fig. 4.13. It shows that $R_{out}$ decreases as $I_{in}$ increases and found to be 0.12 MΩ at $I_{in}$ of 500 µA and 16.7 MΩ at $I_{in}$ of 100 µA.
The frequency response is shown in Fig. 4.14 which reveals a bandwidth of 656 MHz.

In order to access the non-linearity introduced by LVCM, we have performed the transient analysis for evaluating the total harmonic distortion (THD). The plot of THD with respect to the magnitude of the input sine wave current signal at 10 MHz, 50 MHz and 100 MHz for a quiescent current of 200 µA is shown in Fig. 4.15. It has been observed that THD increases with the increase in frequency and amplitude of the input signal.
The THD increases from 0.4 % to 1.22 % as current amplitude is increased from 10 µA to 200 µA at a frequency of 10 MHz. Now as frequency of input signal is increased to 50 MHz, the corresponding THD increases from 0.6 % to 3.15 %. It further increases from 1.97 % and 6.87 % for sine wave of 100 MHz with increase in current amplitude from 10 µA and 200 µA.

The enhancement in bandwidth has also been observed, when resistive compensation is applied to the QFGMOS based LVCM. The passive $R$ has been replaced by the floating MOS resistor whose channel resistance is varied by varying its aspect ratio. The effect of variation of both passive and active $R$ on bandwidth is summarized in Table 4.1.
Table 4.1 Bandwidth enhancement in QFGMOS based LVCM

<table>
<thead>
<tr>
<th>Passive R</th>
<th>BW</th>
<th>Active R</th>
<th>BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 Ω</td>
<td>656 MHz</td>
<td>13 μm/0.26 μm</td>
<td>656 MHz</td>
</tr>
<tr>
<td>1 kΩ</td>
<td>686 MHz</td>
<td>10.04 μm/0.26 μm</td>
<td>671 MHz</td>
</tr>
<tr>
<td>2 kΩ</td>
<td>733 MHz</td>
<td>7.8 μm/0.26 μm</td>
<td>733 MHz</td>
</tr>
<tr>
<td>3 kΩ</td>
<td>875 MHz</td>
<td>5.2 μm/0.26 μm</td>
<td>856 MHz</td>
</tr>
<tr>
<td>4 kΩ</td>
<td>1.04 GHz</td>
<td>3.9 μm/0.26 μm</td>
<td>1.02 GHz</td>
</tr>
<tr>
<td>5 kΩ</td>
<td>1.19 GHz</td>
<td>1.04 μm/0.26 μm</td>
<td>1.52 GHz</td>
</tr>
</tbody>
</table>

The monte carlo analysis for 100 runs has also been performed both for dc and ac behaviour of the QFGMOS based LVCM for variations of 1 %, 5 % and 10 % in model parameters of the transistors. It has been observed that the maximum values of mean deviation for $I_{in} = 100 \mu A$ is $2.03E-18$ and standard deviation is $3.2E-18$ whereas for $I_{in} = 500 \mu A$ the maximum value of mean deviation is found to be $-622.28E-18$ and that of standard deviation is $4.48E-21$. Similarly, for ac analysis the monte carlo analysis yields mean deviation of $-227.37E-15$ and standard deviation zero for bias current of $100 \mu A$ while mean deviation of $-2.27E-12$ and standard deviation of zero for bias current of $500 \mu A$.

4.6.2 Multiple Output Low Voltage Current Mirror

The QFGMOS based LVCM can have multiple outputs to provide the different scaled versions of the input current. It may be achieved by simply adding the additional output transistors (M12 & M13) as shown in Fig. 4.16. Each output can independently provide different currents by setting the aspect ratio of output transistors. Though this structure enhances the utility of current mirror but it results in higher power dissipation and poor
frequency response due to increased parasitic capacitances because of additional MOSFETs.

4.6.3 P-type QFGMOS Low Voltage Current Mirror

A P-type QFGMOS LVCM can be obtained simply by replacing the NMOS transistors by PMOS transistors and vice versa in N-type structure as shown in Fig. 4.17.
The resultant circuit is simulated by selecting aspect ratios of $M_1$ and $M_2$ as $13 \mu m/0.13 \mu m$, $0.13 \mu m/0.13 \mu m$ for $M_3$, $52 \mu m/0.52 \mu m$ for $M_4$, $194.87 \mu m/0.52 \mu m$ for $M_5$, $1.3 \mu m/0.13 \mu m$ for $M_6$, $52 \mu m/0.26 \mu m$ for $M_7$, $39 \mu m/0.52 \mu m$ for $M_8$, $156 \mu m/0.26 \mu m$ for $M_9$, and $5.2 \mu m/0.13 \mu m$ for $M_{10}$ and $M_{11}$.

The input resistance offered by the circuit is $292.6 \Omega$, output resistance of the circuit is $2.99 \ M\Omega$ and the circuit consumes $1.97 \ mW$ power. The $I-V$ characteristics of the P-type QFGMOS LVCM are shown in Fig. 4.18. The offset current is found to be $6.1 \ nA$. The current transfer ratio is found to be $0.96$ with error in current transfer varying from $9.2 \%$ (for input currents below $100 \ \mu A$) to $2.6 \%$ (for $I_{in} = 100 \ \mu A$) and further decreases to $-9.2\%$ (for $I_{in} = 500 \ \mu A$) as shown in Figs. 4.19 & 4.20 respectively. The variation of $R_{out}$ with input current is shown in Fig. 4.21. It is found that $R_{out}$ decreases as $I_{in}$ increases and found to be $2.98 \ M\Omega$ at $I_{in}$ of $500 \ \mu A$ and $304 \ M\Omega$ at $I_{in}$ of $100 \ \mu A$. The frequency response is shown in Fig. 4.22 which reveals a bandwidth of $660 \ MHz$. The total harmonic distortion (THD) analysis of P-type LVCM has also been performed to measure the non linearity introduced by the circuit. The plots of THD as a function of the amplitude of input sine wave current signal at frequency of $10 \ MHz$, $50 \ MHz$ and $100 \ MHz$ for a quiescent current of $200 \ \mu A$ are shown in Fig. 4.23 which reveals that the percentage THD increases from $0.2$ at current amplitude of $10 \ \mu A$ to $3.98$ at current amplitude of $200 \ \mu A$ for $10 \ MHz$ input signal. The corresponding values of THD for $50 \ MHz$ sine wave input are $2.58 \%$ and $14.5 \%$ and it further increases to $7.88 \%$ and $17.25 \%$ as frequency of input signal is increased to $100 \ MHz$. 

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Fig. 4.18 $I$-$V$ Characteristics of P-type QFGMOS LVCM

Fig. 4.19 Current transfer characteristic of P-type QFGMOS LVCM

Fig. 4.20 Error in current transfer characteristics
Fig. 4.21 Variation of $R_{out}$ with $I_{in}$ in P-type QFGMOS LVCM

Fig. 4.22 Frequency response of P-type QFGMOS LVCM

Fig. 4.23 THD plot for P-type QFGMOS LVCM
4.7 Voltage Controlled Resistor

The circuit of a simple MOS based voltage controlled resistor (VCR) is shown in Fig. 4.24 where MOSFETs M1 and M2 are biased in triode region and M2 acts as resistor whose resistance can be controlled by its gate voltage \( (V_C) \). The N-type current mirror formed by M3-M4 and P-type current mirror formed by M5-M6 ensures the same drain current in both M1 and M2.

![Fig. 4.24 MOS based VCR](image)

The transistors M1 and M2 are assumed to be perfectly matched transistors with same drain currents \( I_1 \) and \( I_2 \) in absence of input current \( (I_{in}) \) and M1 is biased in ohmic region. This arrangement makes M2 to operate in ohmic region whose conductivity can be further varied by \( I_{in} \). Thus, M2 act as a variable resistor whose resistance value is controlled by \( V_C \) [129].

The equivalent resistance of the MOS based VCR is given by [116]

\[
R_{eq} = \frac{V_{DS2}}{I_{in}} = \frac{1}{\beta V_C}
\]  

(4.21)
The circuit of Fig. 4.24 is simulated using PSpice level 7 parameters with supply voltage of ±0.5 V by selecting aspect ratio (W/L) as 0.39 µm/0.13 µm for M1 and M2, 7.8 µm/3.9 µm for M3 and M4, 13 µm/0.26 µm for M5 and 26 µm/0.13 µm for M6. The variation of resistance with different control voltages is shown in Fig. 4.25. It is observed that as control voltage varies from 0.1 V to 0.5 V, the resistance varies from 4.28 kΩ to 1.87 kΩ which is in accordance with Eq. (4.21).

The frequency response of MOS based VCR is shown in Fig. 4.26 at a control voltage of 0.3 V which shows that a MOS based VCR has a bandwidth of 5.95 GHz.
4.8 QFGMOS Based Voltage Controlled Resistor

The QFGMOS based voltage controlled resistor is shown in Fig. 4.27. It differs from the FGMOS based voltage controlled resistor presented in reference [118] in a way that the gates of FGMOS are connected to a bias voltage through a large value capacitor ($C_2 >> C_1$) whereas the gates of QFGMOS are connected to supply rails through reverse biased MOSFETs M8-M11.

The drain currents of M1 and M2, biased in the ohmic region are given by:

$$I_1 = \beta \left[ \left( \frac{C_1}{C_{\text{Total}}} (V_{SS} - V_{SS}) + \frac{C'_{GD}}{C_{\text{Total}}} V_{DD} - \frac{C_{GS}}{C_{\text{Total}}} V_{SS} \right) - V_{Tn1} \right] - \frac{V_{DS1}}{2} \right] V_{DS1}$$  \hspace{1cm} (4.22)

where $\beta = \frac{\mu_0 C_{\text{OX}} W}{L}$

and

$$I_2 = I_{in} + I_4 = \beta \left[ \left( \frac{C_1}{C_{\text{Total}}} (V_C - V_{SS}) + \frac{C'_{GD}}{C_{\text{Total}}} V_{DD} - \frac{C_{GS}}{C_{\text{Total}}} V_{SS} \right) - V_{Tn2} \right] - \frac{V_{DS2}}{2} \right] V_{DS2}$$  \hspace{1cm} (4.23)
The current mirror arrangement of transistors M5 and M6 generates a current $I_3$ such that $I_3 = I_4 = I_i$. Since transistors M3 and M4 are assumed to be perfectly matched and are biased in saturation region, their drain currents are given by:

\[ I_3 = \frac{\beta}{2} (V_{GS3} - V_{th3})^2 \]  
(4.24)

\[ I_4 = \frac{\beta}{2} (V_{GS4} - V_{th4})^2 \]  
(4.25)

which gives

\[ I_{in} = \beta (K_1 V_{DD} + K_2 V_C) V_{DS2} \]  
(4.26)

From Eq. (4.26), the equivalent resistance ($R_{eq}$) is given by:

\[ R_{eq} = \frac{V_{DS2}}{I_{in}} = \frac{1}{\beta (K_1 V_{DD} + K_2 V_C)} \]  
(4.27)

where $K_1 = \frac{C_{GD}'}{C_{Total}}$ & $K_2 = \frac{C_1}{C_{Total}}$  
(4.28)

Eq. (4.27) reveals that circuit in Fig. 4.28 implements a voltage controlled resistor whose resistance value depends on the control voltage ($V_C$). The corresponding equation for $R_{eq}$ using FGMOS is given by [118]:

\[ R_{eq} = \frac{1}{\beta (K_1 V_D + K_2 V_C)} \]  
(4.29)

where $K_2$ is same as in Eq. (4.28) for VCR using QFGMOS and $K_1 = \frac{C_2}{C_{Total}}$. Since $C_2 \gg C'_{GD}$ therefore, the resistance value for QFGMOS based VCR will be larger than FGMOS based VCR at a given value of control voltage. It also results in better frequency response of QFGMOS based VCR than its FGMOS counterpart [37, 43].
4.8.1 Simulation Results

The circuit of Fig. 4.27 is simulated using PSpice level 7 parameters with supply voltage of ± 0.5 V and by selecting \( W/L \) of 0.52 \( \mu \text{m}/0.131 \mu \text{m} \) for M1 and M2, 7.8 \( \mu \text{m}/3.9 \mu \text{m} \) for M3 and M4 13 \( \mu \text{m}/0.26 \mu \text{m} \) for M5, 26 \( \mu \text{m}/0.31 \mu \text{m} \) for M6 and 0.13 \( \mu \text{m}/0.13 \mu \text{m} \) for M8-M11. The variation of resistance with different control voltages is shown in Fig. 4.28. It has been observed that the value of the simulated resistance varies inversely with the control voltage as shown by Eq. (4.27).

![Fig.4.28 Resistance simulation with QFGMOS VCR](image)

The circuit of VCR is also implemented using FGMOS and its performance compared with its QFGMOS counterpart. The performance of QFGMOS based VCR has been found to be better than that of its FGMOS version due to the inherent advantages of QFGMOS over FGMOS. The values of the equivalent resistance realized using QFGMOS vis-a-vis FGMOS for different values of \( V_C \) are given in Table 4.2.
Table 4.2 Variation of $R_{eq}$ with $V_C$

<table>
<thead>
<tr>
<th>$V_C$ (V)</th>
<th>$R_{eq}$ with QFGMOS (kΩ)</th>
<th>$R_{eq}$ with FGMOS (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>3.38</td>
<td>1.62</td>
</tr>
<tr>
<td>0.2</td>
<td>2.18</td>
<td>1.56</td>
</tr>
<tr>
<td>0.3</td>
<td>1.76</td>
<td>1.51</td>
</tr>
<tr>
<td>0.4</td>
<td>1.56</td>
<td>1.47</td>
</tr>
<tr>
<td>0.5</td>
<td>1.43</td>
<td>1.43</td>
</tr>
</tbody>
</table>

It can be seen that $R_{eq}$ decreases from 3.38 kΩ to 1.43 kΩ for QFGMOS based VCR and from 1.62 kΩ to 1.43 kΩ for FGMOS based VCR with the increase in $V_C$ from 0.1 V to 0.5 V. The large value of the resistance of the order of kΩs or more can be obtained for smaller dimensions of transistors which may lead to nonlinearity.

It has also been found that for control voltage ($V_C$) of the order of supply voltage, both QFGMOS and FGMOS topologies of VCR yield the same value of resistance. It can be attributed to the fact that when $V_C$ approaches positive supply voltage, Eqs. (4.27 and 4.29) approximately become identical and resemble Eq. (4.21). The frequency response of QFGMOS based VCR at different control voltages is shown in Fig. 4.29. It can be observed that as control voltage is increased from 0.1 V to 0.5 V, bandwidth of QFGMOS based VCR increases from 3.93 GHz to 9.39 GHz with the corresponding decrease in the value of simulated resistance. The same trend has also been observed in FGMOS based VCR. It is due to the fact that with increase in control voltage, the drain current of transistors increases which results in higher bandwidth and lower resistance.
Fig. 4.29 Frequency response of QFGMOS based VCR

The comparative resistance simulation characteristics of VCR based on FGMOS and QFGMOS are shown in Fig. 4.30. It is found that for the same value of control voltage ($V_C = 0.3 \text{ V}$) $R_{eq}$ for FGMOS is 1.51 kΩ whereas $R_{eq}$ is 1.76 kΩ for QFGMOS based VCR. The power dissipation of QFGMOS based VCR (0.03 μW) is found to be less than that of its FGMOS version (4.12 μW).

Fig. 4.30 Comparative resistance simulation characteristic

The comparative frequency response of QFGMOS and FGMOS based VCRs is shown in Fig. 4.31. The bandwidth of QFGMOS based VCR is found to be 7.47 GHz which
is greater than that of FGMOS based VCR (347 MHz) due to the absence of large capacitance ($C_2$).

![Graph of frequency response comparison between QFGMOS and FGMOS]

**Fig. 4.31 Comparative frequency response**

### 4.9 Conclusion

QFGMOS has been employed to implement a current mirror circuit suitable for low voltage applications. The QFGMOS based current mirror is compared to FGMOS current mirror in terms of its frequency response and input voltage requirement. It is found that QFGMOS based current mirror has better frequency response and require less input voltage as compared to its FGMOS counterpart due to its inherited advantages. A novel resistive compensation technique has been employed to enhance the bandwidth of QFGMOS based CM. The compensation technique has been thoroughly analyzed along with the derivation of the optimal value of the compensating resistor and results discussed. A N-type QFGMOS based LVCM has been presented and simulated using 0.13 µm technology at supply voltage ±0.5 V.

The circuit offers input resistance of 235 Ω, output resistance of 117 kΩ and consumes 0.83 mW of power. The input compliance voltage of the QFGMOS based LVCM has been found to be less by 0.1 V as compared to simple QFGMOS CM for an
input current of 500 µA. The offset current is found to be 2.2 nA and current transfer ratio is 0.98 with error that varies from 13.5 % for input currents below 100 µA to −1.8 % at input current of 500 µA. The bandwidth of the QFGMOS based LVCM was found to be 656 MHz. Enhancement in bandwidth for QFGMOS based CM is also shown using both passive as well as active resistors. A P-type version of the QFGMOS based LVCM has also been obtained and simulated.

Finally, QFGMOS has also been used to design a voltage controlled resistor suitable for low voltage applications. The QFGMOS based VCR is thoroughly analysed and its performance is compared to FGMOS based VCR. It has been found that for a given value of controlling voltage, the QFGMOS based VCR simulates a higher value of resistance and offers larger bandwidth as compared to its FGMOS version due to its inherent advantages and consume less power.