CHAPTER 2

FLOATING-GATE MOS TRANSISTOR

2.1 Introduction

The portability and low power consumption of modern electronic gadgets have aroused great interest in the design of low voltage and low power circuits [2-4, 18-20, 38-42]. The miniaturization trend of CMOS technology which favors the low voltage and low power operation results in scaling down of device feature size and threshold voltage. However, the diminishing dimensions of MOS devices with reduced threshold voltage does not facilitate the analog design due to influence of noise signals, increased leakage currents, short channel and parasitic effects besides large variation of threshold voltage [2-3]. Thus, the alternative design techniques for low voltage analog design need to be explored.

Floating-Gate MOS transistor (FGMOS) has proved to be a suitable device for low voltage applications owing to its unique feature of programmability of threshold voltage which can be lowered from its conventional value [43]. The motivation behind the use of FGMOS in low voltage analog design has been attributed to its characteristics like high reliability for data computation due to slow memory decay and low power dissipation. It also ensures good matching of devices by tuning of threshold voltage and does not require frequent adjustment due to long term charge retention property of the device. Moreover, the implementation of FGMOS on silicon does not demand a specialized fabrication process and is fully compatible with the standard double-polysilicon CMOS technology [44-47].
The first FGMOS structure was reported by Kahang and Sze in 1967 for non-volatile storage of information and the first commercial product known as EPROM (Erasable Programmable Read Only Memory) was fabricated using a FAMOS transistor (Floating-gate Avalanche-injection MOS) in 1971 [48-49]. Since then FGMOS has been widely used as memory element in EPROMs, EEPROMs and Flash memories [50-51]. The FGMOS is not only used in digital memories but has also been widely used as trimming element for tuning purposes in analog circuit design as evidenced by Sackinger and Guggenbuhl’s work [52-54]. They proposed an application of the FGMOS transistor as tunable element in analog CMOS amplifiers. Yu and Geiger presented a very low voltage operational amplifier using FGMOS by scaling down the threshold voltage and injecting charge using tunneling effect [55-56].

Op’t Eynde and Zorio proposed a new alternative for using FGMOS in circuits which only had to memorize a few tens of bits, for example, for trimming of analog circuits by means of digital calibration [57]. Since the ON and OFF of the FGMOS transistor is based on result of a weighted sum operation, Shibata and Ohimi called FGMOS as neuron MOS transistor [58-60]. The transistor was used in multivalued logic with advantages over binary logic, since large amount of data can be processed per unit area with reduced number of connections [61-62]. Fujita and Amamiya developed a FGMOS device which could be used as analog memory for neural networks. This device had two floating gates with one gate used for charge injection through Fowler-Nordhein tunnel junction and the other gate was for charge storage. The charge injection gate was made smaller so that it has smaller capacitance than that of the charge storage gate and both the gates were connected by a high resistance. By applying control pulses to the charge injection gate, it was possible to charge and discharge the MOS floating gate in order to modify the current with high resolution over 10 bits [63]. This had a high applicability for on-chip learning in analog neural network. Learning on
a neural network is the change in synaptic weight according to learning algorithm. Kosaka et al. presented a synapse with a good weight updating linearity under constant pulse programming. This was done by using a simple self feedback regime in each cell circuit [64-65]. Literature survey reveals that FGMOS has also found applications in fuzzy logic [66-68]. Yang and Andreou employed FGMOS in multiple-input floating-gate differential amplifier which functioned like a standard differential difference amplifier (DDA) [69]. It had some unique advantages like better transistor matching and lesser circuit complexity. The sub-threshold analysis of FGMOS was also developed by these authors [70]. The sub-threshold model of FGMOS was used by Hasler et al. in various applications like non linear function implementation in current mode and design of memory cells [71-74].

FGMOS was also used as low voltage analog circuit building blocks such as current mirrors, multipliers, rectifiers and amplifiers because of its capability to perform the weighted sum operation of voltage signals applied at its gate and the long term charge retention characteristic of the device [43, 75-80]. Other applications of FGMOS include digital-to-analog converter circuits and means for offset compensation in operational amplifier [81-83]. A number of low voltage realizations of current mode as well as voltage mode computational circuits [84-85], tunable transconductor and filter structures [86-88], high swing amplifiers [89-90] and differential voltage attenuator [91] have also been reported using FGMOS. Recently, a split length FGMOS MOS cell connected in self-cascode arrangement, working as a single device has been proposed and its usefulness verified by designing a current mirror and active inductor [35]. Despite the wide applications of FGMOS, there exists a problem of residual charge in its structure that might remain trapped at the floating-gate during fabrication which could be eliminated by using ultra violet light and lay out techniques [92-93].
In this chapter, we shall discuss the FGMOS structure, its equivalent circuit, large-signal and small-signal model of $N$-input FGMOS. A PSpice simulation model of FGMOS using standard MOS models is also developed which has been used to simulate the characteristics of FGMOS.

### 2.2 Floating-Gate MOS Transistor

The basic structure of Floating-Gate MOS transistor (FGMOS) is shown in Fig. 2.1. The FGMOS is similar to an ordinary MOSFET whose gate is floating being electrically isolated, implying no resistive connections to its gate. A number of secondary gates or inputs are then deposited over the floating-gate (FG) which are electrically isolated from it as shown in Fig. 2.1. These gates are only capacitive connected to FG, since the FG is completely surrounded by highly resistive silicon dioxide. Therefore, under DC operating conditions, the FG becomes a floating node [1].

![Fig. 2.1 Structure of multi-input FGMOS](image)

The concept of leaving the gate of a MOS transistor floating enables to achieve almost infinite input impedance at the gate terminal. The FGMOS can be easily fabricated in a standard double-polysilicon CMOS process where the first polysilicon (polycrystalline silicon) layer forms the floating-gate (FG) over the channel and the second polysilicon layer forms the multiple-input control gates (MIG) over the FG such that MIGs are electrically isolated from FG. It is possible to have several control gates...
over FG but with the trade-off of silicon area. The use of many input gates in FGMOS which results in increased chip area, and is thus, undesired for integration. As illustrated, the FG inserted between the transistor channel and MIG, provides indirect control over the operation of MOSFET.

The voltage on FG can be determined by the amount of charge deposited on it besides the voltage on MIG, drain, source and substrate which in turn modulates the channel conductivity \([2, 34]\). The polysilicon gate being electrically insulated from the transistor channel by a thin sheet of silicon dioxide \((\text{SiO}_2)\), imparts a very high degree of electric isolation between the FG and MIGs in FGMOS. It facilitates the electric charge to stay at FG for a long time without appreciable leakage. It has been demonstrated experimentally that the loss of FG charge is less than 2 % in 10 years at room temperature \([2, 45]\). The threshold voltage of FGMOS can be adjusted by changing the amount of charge on FG. By transferring electrons onto FG the threshold voltage can be increased while removal of electrons from FG decreases the threshold voltage. In FGMOS circuits though we mainly depend on the insulating properties of \(\text{SiO}_2\) yet we need to temporarily break the insulating properties of \(\text{SiO}_2\) in order to manipulate the charge on FG.

The charge stored on FG gets trapped due to an energy barrier provided by the insulating \(\text{SiO}_2\). Free particles like electrons are trying to move through the energy barrier but will not usually make it all the way through and will bounce back again. However, if we make the energy barrier thin and also provide sufficient energy to the free particles, then particles can be made to penetrate the energy barrier all the way through the other side. This process is a quantum mechanical effect called tunneling. There are different ways by which charge on FG can be manipulated like ultra-violet light shining, Hot electron injection and Fowler-Nordheim tunneling. In ultra-violet light shining process \(\text{SiO}_2\) layer is made temporarily conductive by using short-wave
ultra-violet (UV) light. Exposing SiO$_2$ to UV light will shake loose free electron-hole pairs with sufficient kinetic energy to surmount the SiO$_2$ energy barrier around the FG charge, as a result, the static charge on FG charge leaks away. The efficiency of this method is not high since the UV-activated current through SiO$_2$ is very small which makes the erasing time too large.

In hot electron injection (HEI) method, free carriers are produced with sufficiently high energy in the channel underneath the gate. Carriers with sufficient energy (greater than the SiO$_2$ energy barrier of 3.2 eV), which are called “hot carriers”, tunnels through the thin gate oxide. Due to collisions in the channel, the free carriers will scatter in random directions and a fraction will tunnel through the gate oxide. This phenomenon is normally not experienced in every MOSFET because the electric field in the gate oxide makes the carriers bounce back to the channel. So, we need to help this process by applying an electric field towards the gate. HEI technique, when used to implement fast transfer of gate charge, usually requires fairly high channel currents and the desired electric field in the gate-oxide is not always easy to establish without special processing efforts. Hence, this technique is generally not preferred being complicated.

Another well established technique for charge transport through SiO$_2$ is called Fowler-Nordheim (FN) tunneling that requires a sufficiently high electric field across the gate-oxide so as to tunnel the electrons through the SiO$_2$ energy barrier. FN electron tunneling allows charge to be transferred to or from FG depending on the polarity of the field. The amount of charge to be transferred depends on the magnitude and duration of the programming pulse that is needed to produce a large enough electric field in the tunnel oxide. As charge transfer to or from FG affects the threshold voltage of FGMOS, therefore, parameters of the programming pulse like the magnitude, polarity and pulse duration can be used to control its value. This method is preferred for analog
applications being faster and the accurate control over the FG charge due to the exponential relation between programming voltage and current [2, 45].

2.3 Modeling of FGMOS

In FGMOS if the control gates are ignored then its physical structure becomes identical to the conventional MOS transistor. Hence, the drain characteristics of FGMOS are similar to that of a conventional MOS transistor [2, 94-96]. Thus, the model of FGMOS can be obtained by suitably modifying the models of conventional MOSFET.

2.3.1 Large-Signal Model

The symbolic representation of an N-channel multi-input FGMOS is shown in Fig. 2.2 and its equivalent circuit is shown in Fig. 2.3. The large-signal model of FGMOS is derived by first obtaining the voltage on FG as a function of the voltages on the nodes that are capacitively coupled to its inputs. The equation for drain current in FGMOS is then obtained by modifying the corresponding equation of the conventional MOSFET wherein the gate voltage is replaced by the voltage obtained on the FG [1-2].

![Fig. 2.2 Symbol of multi-input FGMOS](image-url)
The values of input capacitance of MIG which are capacitive connected to FG can be
given by [1]:

\[ C_i = \left[ \frac{\varepsilon_{si}}{t_{si}} \right] A_i \]  \hspace{1cm} (2.1)

where \( \varepsilon_{si} \) is the permittivity of SiO\(_2\) layer, \( t_{si} \) is the thickness of SiO\(_2\) layer between the
FG and MIGs and \( A_i \) is the area of each input capacitor plate.

The voltage on FG (\( V_{FG} \)) is determined using the charge conservation law and is given
by:

\[ \sum_{i=1}^{N} C_i (V_i - V_{FG}) + C_{FGS}(V_S - V_{FG}) + C_{FGD}(V_D - V_{FG}) + C_{FGB}(V_B - V_{FG}) + Q_{FG} = 0 \]  \hspace{1cm} (2.2)

where \( Q_{FG} \) refers to certain amount of charge that has been trapped in the FG during the
fabrication of FGMOS.

Eq. (2.2) gives

\[ V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_i + \frac{C_{FGS}}{C_{Total}} V_S + \frac{C_{FGD}}{C_{Total}} V_D + \frac{C_{FGB}}{C_{Total}} V_B + \frac{Q_{FG}}{C_{Total}} = 0 \]  \hspace{1cm} (2.3)

where \( N \) is the number of inputs, \( C_i \) represent the capacitances between MIGs and FG
and \( V_i \) represent the voltages applied on the input gates. \( C_{FGS}, C_{FGD} \) & \( C_{FGB} \) denote the
capacitances from FG to source, drain and bulk respectively. \( V_S, V_D \) & \( V_B \) represent the
voltages on the source, drain and bulk respectively. The term $C_{Total}$ denotes the total capacitance seen by FG and is given by:

$$C_{Total} = \sum_{i=1}^{N} C_i + C_{FGS} + C_{FGD} + C_{FGB}$$  \hspace{1cm} (2.4)$$

Now, the equations used to model the large-signal behavior of FGMOS can be derived by replacing $V_{GS}$ in the corresponding equations of the conventional MOSFET with the expression of $V_{FG}$ with respect to source and assuming $V_B = 0$.

The drain current ($I_D$) of the FGMOS in weak inversion saturation region is obtained by substituting Eq. (2.3) for $V_{GS}$ in the equation $I_D = \frac{W}{L} I_{DO} \exp\left(\frac{V_{GS}}{n\left(\frac{KT}{q}\right)}\right)$ where $n$ is subthreshold slope factor, and $I_{DO}$ is a process dependent parameter that is dependent also on $V_{SB}$ and $V_T$. The MOSFET can be operated in sub-threshold region for $V_{GS} < V_T + n \frac{KT}{q}$.

Now the expression for $I_D$ for FGMOS in weak inversion saturation region becomes

$$I_D = \frac{W}{L} I_{DO} \exp\left(\sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{IS} \frac{KT}{q} + \frac{C_{FGD}}{C_{Total}} V_{DS} \frac{KT}{q} + \frac{Q_{FG}}{C_{Total}} \frac{KT}{q}\right)$$  \hspace{1cm} (2.5)$$

under the condition $$\left(\sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{IS} + \frac{C_{FGD}}{C_{Total}} V_{DS} + \frac{Q_{FG}}{C_{Total}}\right) < \left(V_T + n \frac{KT}{q}\right).$$

If we assume zero initial charge present on FG, then Eq. (2.5) becomes

$$I_D = \frac{W}{L} I_{DO} \exp\left(\sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{IS} \frac{KT}{q} + \frac{C_{FGD}}{C_{Total}} V_{DS} \frac{KT}{q}\right)$$  \hspace{1cm} (2.6)$$

Now the drain current ($I_D$) of the FGMOS in ohmic region is obtained by substituting Eq. (2.3) for $V_{GS}$ in equation $I_D = \beta \left(V_{GS} - V_T\right) - \frac{V_{DS}}{2} V_{DS}$.
Now the expression for $I_D$ in ohmic region for FGMOS is given by:

$$I_D = \beta \left\{ \left\{ \sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{iS} \right\} + \frac{C_{FGD}}{C_{Total}} V_{DS} + \frac{C_{FGB}}{C_{Total}} V_{BS} + \frac{Q_{FG}}{C_{Total}} \right\} - V_T - \frac{V_{DS}}{2} \right\} V_{DS}$$  \hspace{1cm} (2.7)

under the biasing condition of

$$0 < V_{DS} \leq \left\{ \left\{ \sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{iS} \right\} + \frac{C_{FGD}}{C_{Total}} V_{DS} + \frac{C_{FGB}}{C_{Total}} V_{BS} + \frac{Q_{FG}}{C_{Total}} \right\} - V_T \right\} \& V_{GS} > V_T.$$

where $\beta = \frac{\mu_{0} C_{ox} W}{L}$ is the transconductance parameter & $V_T$ represents the threshold voltage as seen from FG.

Assuming $V_{BS}$ and $Q_{FG}$ to be zero Eq.(2.7) becomes

$$I_D = \beta \left\{ \left\{ \sum_{i=1}^{N} \frac{C_i}{C_{Total}} V_{iS} \right\} + \frac{C_{FGD}}{C_{Total}} V_{DS} \right\} - V_T - \frac{V_{DS}}{2} \right\} V_{DS}$$  \hspace{1cm} (2.8)

In a $N$ input FGMOS since a bias voltage ($V_{bias}$) is applied to one of the inputs through a large value capacitor so that effectively there are $N-1$ inputs. Therefore, the above Eq. can be written as:

$$I_D = \beta \left\{ \left\{ \sum_{i=2}^{N} \frac{C_i}{C_{Total}} V_{iS} \right\} + \frac{C_1}{C_{Total}} V_{bias} + \frac{C_{FGD}}{C_{Total}} V_{DS} \right\} - V_T - \frac{V_{DS}}{2} \right\} V_{DS}$$  \hspace{1cm} (2.9)

Eq. (2.9) may be simplified to:

$$I_D = \beta \left( \sum_{i=2}^{N} \frac{C_i}{C_{Total}} \right) \left[ \left\{ \sum_{i=2}^{N} V_i - V_{T, eff} \right\} V_{DS} - \frac{C_{Total}}{2 \sum_{i=2}^{N} C_i} V_{DS}^2 \right]$$  \hspace{1cm} (2.10)

where $V_{T, eff}$ is the effective threshold voltage which is equal to:

$$V_{T, eff} = \frac{C_{Total}}{\sum_{i=2}^{N} C_i} V_T - \frac{C_1}{\sum_{i=2}^{N} C_i} V_{bias}$$  \hspace{1cm} (2.11)

For $C_1 \gg (C_{FGS} + C_{FGD} + C_{FGB})$, Eq. (2.11) reduces to:
\[ V_{T,\text{eff}} = V_T + \frac{C_1}{\sum_{i=2}^{N} C_i} (V_T - V_{\text{bias}}) \]  

(2.12)

The essential reduction in \( V_{T,\text{eff}} \) can be obtained by selecting \( V_{\text{bias}} > V_T \) and \( C_1 > C_i \). Hence, we achieve lower \( V_{T,\text{eff}} \). This property is utilized in low voltage applications.

The drain current of the FGMOS in saturation region is given by:

\[
I_D = \frac{\beta}{2} (V_{FG} - V_T)^2 = \frac{\beta}{2} \left[ \sum_{i=1}^{N} \frac{C_i}{C_{\text{Total}}} V_{iS} + \frac{C_{FGD}}{C_{\text{Total}}} V_{DS} + \frac{C_{FGB}}{C_{\text{Total}}} V_{BS} + \frac{Q_{FG}}{C_{\text{Total}}} - V_T \right]^2 
\]

under the biasing condition of

\[ 0 < \left( \sum_{i=1}^{N} \frac{C_i}{C_{\text{Total}}} V_{iS} + \frac{C_{FGD}}{C_{\text{Total}}} V_{DS} + \frac{C_{FGB}}{C_{\text{Total}}} V_{BS} + \frac{Q_{FG}}{C_{\text{Total}}} - V_T \right) \leq V_{DS} \]

Assuming \( V_{BS} \) and \( Q_{FG} \) to be zero Eq. (2.13) becomes

\[
I_D = \frac{\beta}{2} (V_{FG} - V_T)^2 = \frac{\beta}{2} \left[ \sum_{i=1}^{N} \frac{C_i}{C_{\text{Total}}} V_{iS} + \frac{C_{FGD}}{C_{\text{Total}}} V_{DS} \right] - V_T 
\]

(2.14)

We find that the drain current in FGMOS depends on the weighted sum of input voltages. This feature enables a linear addition of signals in voltage form and is useful for analog computation.

Eq. (2.14) can be further simplified to:

\[
I_D = \frac{\beta}{2} \left( \sum_{i=2}^{N} \frac{C_i}{C_{\text{Total}}} \right)^2 \left[ \sum_{i=2}^{n} \frac{C_i}{C_{\text{Total}}} V_{iS} \right] - V_{T,\text{eff}}^2 
\]

(2.15)

It is obvious from Eq. (2.15) that if drain is strongly capacitively coupled (that is \( C_{FGD} \) is large) with the floating-gate then the drain current in saturation region will not saturate and increase continuously with the drain voltage. However, if this capacitance (\( C_{FGD} \)) is negligibly small, then the drain characteristics of FGMOS become similar to those of conventional MOSFET. The capacitance between floating-gate and input...
gate, $C_i$, can be made much greater than $C_{FGD}$ by using layout techniques. Eq. (2.15) also implies that $I_D$ for FGMOS is less than that of a conventional MOSFET due to the multiplication factor $\left(\frac{C_i}{C_{Total}}\right)^2$ which is always less than unity.

### 2.3.2 Small-Signal Model

A $N$-input FGMOS has $(N-1)$ more terminals than a conventional MOS transistor, and therefore, $(N+2)$ small signal parameters can be defined for FGMOS which are $N$ effective input transconductances, $g_{mi,eff.}$ for $i = [1, N]$, an output conductance $g_{o,eff.}$ and bulk transconductance $g_{mbs,eff.}$.

The effective transconductance of FGMOS ($g_{mi,eff.}$) is given by:

$$
g_{mi,eff.} = \left(\frac{C_i}{C_{Total}}\right) g_m \tag{2.16}
$$

where $g_m$ is the gate transconductance of a MOS transistor. The $g_m$ of FGMOS ($g_{mi,eff.}$) is also less than that of conventional MOSFET by a factor of $(C_i/C_{Total})$.

Hence, FGMOS structures are basically low gain structures.

The effective output conductance of FGMOS ($g_{o,eff.}$) is given by:

$$
g_{o,eff.} = g_o + \frac{C_{FGD}}{C_{Total}} g_m \tag{2.17}
$$

Thus, $g_{o,eff.}$ is higher and as a result, the output impedance of the FGMOS based structures is lower than that of conventional MOSFET based structures due to the feedback taking place from drain to floating-gate through $C_{FGD}$. In order to increase the output impedance cascoding may be used in FGMOS.

The channel transconductance due to $V_{SB}$ ($g_{mbs,eff.}$) is found to be same as that of conventional MOSFET and it is given as:
\[ g_{\text{mrs.eff.}} = g_m \frac{\gamma}{2(2|\phi_r| + |V_{SB}|)^{1/2}} \]  

where \( \gamma \) is bulk threshold parameter and \( 2|\phi_r| \) is surface potential at strong inversion [1].

The transition frequency of a two-input FGMOS \( (f_{T.eff.}) \) is given by:

\[ f_{T.eff.} = \frac{1.5\mu_n}{2\pi L} \left( \frac{C_1}{C_{\text{Total}}} \right) \left[ V_i + \frac{C_{FGD}}{C_1} V_B - V_{T.eff.} \right] \]  

Eq. (2.19) indicates the lowering in \( f_{T.eff.} \) by a factor of \( (C_i/C_{\text{Total}}) \), resulting in the poor frequency response of FGMOS structures.

The small-signal (high frequency) model of FGMOS is obtained by adding the parasitic capacitances to the low frequency model. The small-signal model so derived for two-input FGMOS is shown in Fig. 2.4 which may be further simplified as shown in Fig. 2.5.

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Fig. 2.4 High frequency model of FGMOS
However, at low frequencies, the equivalent model reduces to the DC model of the conventional MOSFET.

### 2.3.3 PSpice Simulation Model

The design of circuit structures using FGMOS requires the validation of performance of resulting structures using simulators like PSpice. Since the model parameters for FGMOS are not available, hence standard MOS models can be used to simulate these structures. The appropriate electrical components are added to the standard MOS models to represent the FGMOS structures.

The equivalent circuit of FGMOS as shown in Fig. 2.3 contains many capacitances between the various terminals. When this circuit is simulated using PSpice, the simulations fail to converge because of floating nodes arising in the circuit. Since PSpice cannot accept floating nodes with no dc path to ground, we need to bypass each capacitance with very high resistance. The resistance value should be chosen so that it behaves like an open circuit. Thus, the problem of floating node is avoided in the simulation of FGMOS based circuits. In actual practice, the leakage resistances through capacitor structures may account for these bypass resistances.
The PSpice model of multi-input FGMOS is shown in Fig. 2.6 where each capacitor is bypassed by its corresponding resistor [2-4]. Here, the resistances are chosen such that each branch has the same time constant that is:

\[ R_1C_1 = R_2C_2 = \ldots = R_nC_n = R_{FGD}C_{FGD} = R_{FGS}C_{FGS} = R_{FGB}C_{FGB} \] (2.20)

This condition ensures that the dc voltage present on the FG is not affected by the introduction of the resistors which may be supported by mathematical formulation.

We have the dc nodal equation for the floating-gate given as:

\[ V_{FG} \left( \frac{1}{R_{FGD}} + \frac{1}{R_{FGS}} + \frac{1}{R_{FGB}} + \sum_{i=1}^{N} \frac{1}{R_i} \right) - \frac{V_D}{R_{FGD}} - \frac{V_S}{R_{FGS}} - \frac{V_B}{R_{FGB}} - \sum_{i=1}^{N} \frac{V_i}{R_i} = 0 \] (2.21)

Using Eq. (2.20), Eq. (2.22) can be rewritten as:

\[ V_{FG} = \frac{\left( \frac{V_D}{R_{FGD}} + \frac{V_S}{R_{FGS}} + \frac{V_B}{R_{FGB}} + \sum_{i=1}^{N} \frac{V_i}{R_i} \right)}{\left( \frac{1}{R_{FGD}} + \frac{1}{R_{FGS}} + \frac{1}{R_{FGB}} + \sum_{i=1}^{N} \frac{1}{R_i} \right)} \] (2.22)

\[ V_{FG} = \frac{\left( C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum_{i=1}^{N} C_i V_i \right)}{C_{Total}} \] (2.23)
Eq. (2.23) gives the expression for FG voltage with the assumption that there is no
initial charge present on FG. If there is any initial charge present on FG then the PSpice
simulation model can be appropriately modified.

The simulation model of FGMOS has been used to simulate the behavior of two-
input FGMOS shown in Fig. 2.7. For simulation of characteristics, we have chosen
$C_1 = 0.1 \text{ pF}$, $R_1 = 200 \text{ M} \Omega$, $C_2 = 0.2 \text{ pF}$, $R_2 = 100 \text{ M} \Omega$, $V_{\text{bias}} = +0.5 \text{ V}$ and
$W/L = 39/0.13 \mu\text{m}$ at supply voltage of $\pm 0.5 \text{ V}$.

![Fig. 2.7 Two-input FGMOS](image)

The drain characteristics of FGMOS for different values of input signal are shown in
Fig. 2.8. The drain characteristics depict the square law and resemble to that of
conventional MOSFET.

![Fig. 2.8 Drain characteristics of FGMOS](image)
The transfer characteristics of FGMOS are shown in Fig. 2.9. The behaviour of FGMOS transfer characteristic differs from that of the conventional MOSFET due to the presence of voltage at FG ($V_{bias}$) even in the absence of input signal. The appreciable drain current at low $V_{in}$ for FGMOS as compared to the characteristic of conventional MOSFET reveals that there takes place a reduction in threshold voltage in FGMOS and the low level of drain current at higher values of $V_{in}$ accounts for the low transconductance of FGMOS.

![Fig. 2.9 Transfer characteristics of FGMOS](image)

2.4 Conclusion

In this chapter, we have discussed the utility of FGMOS for low voltage and low power applications with its historical background. We have dealt with the structure and operation of FGMOS. The mathematical modeling of $N$-input FGMOS both for large-signal and small-signal operation has been presented. The relevant equations have been derived which are based on the corresponding equations for a conventional MOSFET. The high frequency model of two-input FGMOS has also been presented followed by a PSpice simulation model which has further been used to simulate its characteristics.