## Chapter 6

**ACTIVE CLAMP ZVS FLYBACK CONVERTER WITH OUTPUT VOLTAGE DOUBLER**

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6.1 Introduction

The main disadvantage of resonant converters dealt in chapter 4 and 5 are high voltage and current stress in the devices. For a primary ZVS resonant converter the voltage across the main switch is more than twice the supply voltage. In order to reduce it, clamping capacitors are used. It reduces the voltage stress across the switches. The results obtained from the hardware prototype developed are discussed in detail.

6.2 Single output Active Clamped ZVS Flyback Converter

Integrating an active-clamp circuit with flyback resonant circuit eliminates transformer leakage losses, minimizes turn-OFF voltage stress across the power switch and achieves ZVS in the power switch.

6.2.1 Principle of operation

The active-clamp ZVS flyback converter configuration is shown in Fig. 6.1. To minimize voltage spike due to transformer inductance when the main switch is turned OFF; an auxiliary switch and one clamping capacitor are incorporated within the converter. In Fig. 6.1, S₁ and S₂ are the main and the auxiliary switches respectively, Lᵣ is the resonant inductance and Cᵣ is the resonant capacitance. To minimize the voltage spike due to leakage inductance during the turn OFF of the main switch S₁, the auxiliary switch S₂ and clamp capacitor Cₖ are integrated with the circuit. Cᵣ and Lᵣ resonate during the transition of main switch (S₁) and
auxiliary switch ($S_2$). $D$ is diode in the secondary side and $C_o$ is the filter capacitor.

**Fig: 6.1 Circuit diagram of actively clamped ZVS flyback converter**

Assumptions in addition to those assumed in section 4.2.2 are:

- The turn OFF time of the main switch is less than the resonant period
- To achieve ZVS for both $S_1$ and $S_2$, the resonant capacitor energy is less than that of resonant inductor energy

### 6.2.2 Modes of Operation

**A. Mode 1 ($t_0$-$t_1$)**

Before the 1st mode of operation, both switches are in OFF condition and the coupling capacitor has an initial charge of $V_{cc} = nV_0$. When the main switch $S_1$ is ON, the supply voltage is applied across the transformer primary and accordingly, a secondary voltage is induced in the transformer. The inductor $L_r$ charges linearly and the induced voltage on secondary side reverse biases the diode $D_1$. The filter capacitor provides the output voltage.
**B. Mode 2 \((t_1-t_2)\)**

Switch \(S_1\) is switched OFF in this mode. By utilizing the energy stored in the inductor, the capacitor \(C_r\) starts to charge and when the capacitor voltage is equal to \((V_{in} + V_{cc})\), the body diode of \(S_2\) turns ON. The
capacitor $C_c$ charges through this diode. On the secondary side, the energy stored in the magnetising inductance forward biases diode $D_1$ and the energy stored in the transformer is delivered to the load and thus charges the output capacitor $C_0$. Fig. 6.2(b) and (c) show the equivalent circuit for mode 2 operation.

![Fig: 6.3 Theoretical waveforms for actively clamped ZVS flyback converter](image)

**C. Mode 3 ($t_2$-$t_3$)**

This mode is responsible for achieving ZVS in switch $S_2$. During turn ON, the current flows through the switch and energy is released from the coupling capacitor. This causes the capacitor to discharge and the
inductor charges in the reverse direction as illustrated in Fig. 6.2(d). The operation of the secondary side is same as in mode 2.

**D. Mode 4 (t₃-t₄)**

When switch S₂ is turned OFF, the clamp capacitor is removed from the control circuit as explained in Fig. 6.2(e). During this mode, resonant capacitor Cᵣ discharges and the resonant inductor charges. Fig. 6.3 shows waveforms for one switching period of the desired converter.

**6.2.3 Design**

The design process of the active clamped ZVS flyback converter is considered in this section.

**6.2.3.1 Specifications**

Specifications for the converter circuit are same as given in section 5.4.3.1.

**6.2.3.2 Resonant Component Design**

To achieve soft switching in the switches the design of Lᵣ and Cᵣ are carried out with ZVS criteria as given by equations (4.1) – (4.4) and the designed values are Cᵣ = 10nF and Lᵣ = 55μF.

**6.2.3.3 Transformer and Inductor Design**

Design of the transformer and inductors are carried out as per the design elaborated in section 5.3.1.3 and the results obtained are tabulated in Table 6.1.
### Table 6.1 Transformer and Inductor design details

<table>
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<th>Parameters</th>
<th>Core selected</th>
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<tr>
<td>Transformer design</td>
<td>From Appendix –I : core - EE 20/10/5</td>
</tr>
<tr>
<td>$A_p = 91.838 \text{ mm}^4$, $N_p = 19$, $N_S = 22$</td>
<td>$A_p = 0.149 \text{ mm}^4$, $A_w = 47.8 \text{ mm}^2$, $A_c = 31 \text{ mm}^2$</td>
</tr>
<tr>
<td>Resonant Inductor Design</td>
<td>From Appendix –I : core - EE 20/10/5</td>
</tr>
<tr>
<td>$E = 6.05 \times 10^{-6}J$, $A_p = 91.8\text{mm}^4$, $N = 23$ turns</td>
<td>$A_p = 0.15 \text{ mm}^4$, $A_w = 47.8 \text{ mm}^2$, $A_c = 31 \text{ mm}^2$</td>
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#### 6.2.3.4 Design of $C_o$ and $C_c$

Taking 1% output voltage ripple, $\frac{\Delta V_o}{V_o} = \frac{D}{R C_0 f}$

Output Capacitance, $C_{01} = 160\mu\text{F}$

Clamping capacitor, $C_c = \frac{1-D_{\text{min}}}{\pi^2 L_r \ast f_s^2} = 1\mu\text{F}$

#### 6.2.4 Open-loop Simulation Results

The converter is simulated in PSIM platform using the designed values and the results obtained are discussed in this section. As shown in Fig. 6.4(b) and (c), switching pulses with main switch pulse width of 47% and auxiliary switch pulse width of 46% are observed with a small delay of 0.5\mu s between them. The output voltage and current obtained are (3.3V, 0.33A) as shown in Fig. 6.4(a). From Fig. 6.4(b) and(c) it is observed that switch-1 is turned ON at ZVS, and switch-2 is turned ON at ZCS. Fig. 6.5(a) shows the resonant capacitor voltage with peak value of 24V and peak current through the capacitor at 1.5A. The resonant capacitor charges when switch-1 is turned OFF. The peak clamping
capacitor voltage of 11.7V and peak capacitor current of 1A obtained are shown in Fig. 6.5(b).

**Fig: 6.4** (a) Output voltage-1 and current-1 (b) Switch-1 pulse, voltage and current (c) Switch-2 pulse voltage and current

**Fig: 6.5** (a) Switch-2 pulse, resonant capacitor voltage and current (b) Switch-2 pulse, coupling capacitor voltage and current

### 6.2.5 Experimental Results

Based on the designed values, an actively clamped ZVS flyback converter circuit model is implemented. The active switches used are a power MOSFET IRF840 which has a gate source voltage of +/-20V and
drain current of 8A. The secondary diodes used are ultra-fast recovery rectifier IN5817.

The hardware set up is shown in Fig. 6.6. The microcontroller LPC2148 is used for generating the gate pulses for switches. To provide isolation between the gating circuit and power circuit the pulses are given to switches through an opto-coupler IC TLP250. The peak to peak amplitude of the pulses are 12.4V and 14V, with 47.3% and 46.7% duty cycle respectively, as illustrated in Fig. 6.7(a). The output voltage with 3.68V magnitude and current with 334mA magnitude obtained is shown in Fig. 6.7(b).

Fig: 6.6 Hardware set up for actively clamped ZVS flyback converter

Fig: 6.7 (a) Switch pulses (b) Output voltage and current
The peak voltage across the switches (3.36V) and peak current through the switch (2.05V) are shown in Fig. 6.8(a). Voltage across the switches is zero, when the switches are turned ON with the gate pulses. Thus, ZVS is achieved in the power switches. Switch-2 with peak voltage of 3.2V and peak current of 2A is shown in Fig. 6.8(b). Switch-2 is turned ON only when the voltage across the switch is zero with the gating pulses. This technique helps to achieve soft switching which leads to protection of the switches from high voltage stress.

![Fig: 6.8(a) Switch-1 pulse, voltage and current (b) Switch-2 pulse, voltage and current](image)

Fig. 6.9(a) shows the resonant capacitor Voltage (12.7V) and current (1.02A). When switch S1 is turned off, the capacitor resonates with the inductor. The coupling capacitor starts resonating when switch S2 is turned ON and peak voltage obtained is 9.86V as shown in Fig. 6.9(b).

The active clamp circuit reduces the switch voltage to a nominal range thereby addressing the voltage stress issue across the ZVS
switches. Still the problem of diode losses remain which is solved by adding voltage doubler in the secondary and is dealt in the next section.

![Graphs showing Switch-2 pulse, resonant capacitor voltage and current](image)

**Fig: 6.9 (a) Switch-2 pulse, resonant capacitor voltage and current (b) Switch-2 pulse, coupling capacitor voltage and current**

### 6.3 Active Clamp ZVS Flyback Converter Voltage Doubler

Voltage doubler circuit is introduced in the secondary of the transformer to reduce the voltage stress in the secondary diodes. Hence this converter possesses the advantages of resonance, clamping capacitors and voltage doubler circuits. Fig. 6.10 shows the actively clamped ZVS flyback converter circuit with voltage doubler added to secondary side of the transformer.

![Circuit Diagram](image)

**Fig: 6.10 Circuit diagram**
The voltage doubler circuit consists of capacitor $C_s$ and diodes $D_1$ and $D_2$. All other parameters are similar to the actively clamped ZVS flyback circuit.

### 6.3.1 Modes of Operation

The converter operation is spilt as 5 modes and they are explained as follows.

**A. Mode 1 ($t_0$-$t_1$): $S_1$ - ON**

Before the 1st mode, both the switches $S_1$ and $S_2$ are OFF and the initial voltage across the coupling capacitor is $V_{cc}(0) = nV_0$. At time $t_0$, the main switch is turned ON and the current starts to flow through $V_{in}$, $L_r$ and primary winding of the transformer. The inductor current $i_{Lr}$ increases linearly and the supply voltage is fed to the primary of the transformer. As a result, an equivalent current builds up in the secondary side, as shown in Fig. 6.11(a). Diode $D_1$ is forward biased and capacitor $C_{s1}$ starts charging. The output filter capacitor supplies the load.

**B. Mode 2 ($t_1$-$t_2$): $S_1$ - OFF**

This starts when switch $S_1$ is switched OFF. The primary current flows through the resonant capacitor and starts charging it. The coupling capacitor voltage is maintained at $nV_0$ as per the previous mode. By the effect of switching, a reverse polarity voltage is induced in the primary and secondary windings as shown in Fig. 6.11(b). This forward biases the
diode D₂ and the transformer secondary is connected to the load end through the capacitor Cₛ₁.

![Diagrams of Modes 1 to 4]

Fig: 6.11 Modes of operation

**C. Mode 3 (t₂ - t₃): S₂ - ON**

Fig. 6.11(c) & (d) shows this mode of operation. The mode starts when the voltage across the resonant capacitor reaches \((V_{in} + V_{CC})\) and
forward biases the body diode of $S_2$. The inductor $L_m$ and $L_r$ discharges its stored energy. Using the positive resonant current $i_{Lr}$, the clamp capacitor is charged. Across the resonant inductor and the transformer magnetizing inductor, the clamp capacitor fixes a voltage which results in a voltage divider in between the two inductances. As a result, the resonant inductor $L_r$ and clamping capacitor $C_c$ begin to resonate. The capacitor charges in the reverse direction when the gating signal is applied to $S_2$, which results in ZVS, as shown in Fig. 6.12. On the secondary side, diode $D_2$ is still forward biased and the working is similar to the previous mode.

**D. Mode 4 ($t_3$-$t_4$: $S_2$ - OFF)**

In this mode, the auxiliary switch $S_2$ is turned OFF hence the effect of the clamp capacitor in the circuit is removed. The resonant capacitor $V_{cr}$ starts charging. On the secondary side, the capacitor $C_{s1}$ charges through diode $D_1$ and the output is supplied from the filter capacitor. The equivalent circuit is as shown in Fig. 6.11(e).

Fig. 6.12 shows the theoretical waveforms for one switching period for actively clamped multi-output flyback converter with voltage doubler. The circuit configuration changes whenever the switching devices are changed from one state to another.
6.3.2 Design and Specifications

Specifications for the circuit are as discussed in section 5.6.3. The transformer, resonant inductor, resonant capacitor and coupling capacitor for a 5V and 500mA are the same as explained in section 6.2.3.

The capacitor on the secondary side, \( C_s = \frac{4(\pi N_p D T_s)^2}{L_r} = 1\mu F \),

Where,

\( N_p \) - No. of turns in primary

\( D \) - duty cycle

\( L_r \) - resonant inductor

6.3.3 Open-loop Simulation Results

With the designed specifications, the converter is simulated in PSIM platform. The output voltage (5V) and current (0.5A) obtained are
as captured in Fig. 6.13(a). To achieve ZVS, the switches are turned ON at zero voltage.

![Graphs showing output voltage and current, secondary capacitor voltage and current](a) (b)

Fig: 6.13 (a) Output voltage and current (b) Secondary capacitor voltage and current

The switch voltage and current waveforms obtained are similar to the waveforms shown in Fig. 6.4(b) and (c) as given in section 6.2.4. The duty cycle for the switches S₁ and S₂ are 47% and 46% respectively. The secondary capacitor voltage (2.13V) and current (3A) are shown in Fig. 6.13(b). The leakage inductance of the transformer resonates with the secondary capacitor Cₛ, hence no large filter inductor is required. The primary switch turn-OFF loss, RCD snubber loss is minimized and secondary side D₁ is turned-OFF smoothly because the resonant operation shapes the current to be sinusoidal. The input voltage for the converter is 12V. The coupling capacitor voltage is obtained as 11.7V. The voltage and current for the diodes D₁ and D₂ are shown in Fig. 6.14(a) and (b). When switch S₁ is turned ON, the diode D₁ (4.5V and
2.4A) gets forward biased and when switch S₂ is turned OFF, the diode D₂ (2.5V and 1A) gets forward biased. The resonant inductor current and voltage obtained are 2.4A and 10V.

![Fig: 6.14](a) Switch-1 pulse, diode-1 voltage, current (b) Switch-1 pulse, diode-2 voltage, current

### 6.3.4 Experimental Results

The converter explained and designed in the previous section is built as a hardware prototype and the results obtained are discussed in detail. The hardware implementation is similar to that explained in section 6.2.5. The hardware setup is shown in Fig. 6.15(a). The output voltage (5V) and current (500mA) are obtained according to the designed values which are shown in Fig. 6.15(b). The input voltage supplied is 12V. The voltage and current for the diodes D₁ (V₁pk = 7.6V and I₁pk =
1.22A) and D₂ (V_{D2-pk} = 7.2V and I_{D2-pk} = 1.92A) are shown in Fig. 6.16(a) and (b).

Fig: 6.15 (a) Hardware set up for active clamp ZVS flyback converter with voltage doubler (b) Output voltage and current

![Image](image_url)

Fig: 6.16 (a) Switch-1 pulse, diode-1 voltage, current (b) Switch-1 pulse, diode-2 voltage, current

When switch S₁ is turned ON, the diode D₂ gets forward biased and when switch S₁ is turned OFF, the diode D₁ gets forward biased. When the diode is forward biased, the voltage across the diode is less than 1V.

The duty cycle for the switches S₁ (V_{sw-pk} = 12.7V and I_{sw-pk} = 138mA) and S₂ (V_{sw-pk} = 7.2V and I_{sw-pk} = 1.07A) are 47% and 46% respectively. The coupling capacitor voltage is 9.8V. The peak values of resonant inductor current and voltage are 2.4A and 29.6V respectively. It is observed that, with the incorporation of the voltage doubler circuit in the secondary, the
output voltage is increased by 2V. Thus, the voltage conversion ratio is increased with the addition of one capacitor and two diodes while the space utilized remains the same. The drawback of single output topology still remains.

6.4 Active Clamp ZVS Multi-output Flyback Converter

The multi-output converters are generally used in low power applications which require different output voltage levels. Compared to the collection of single output converters these are more compact and less costly. To obtain multi-output DC voltages with isolation, multiple secondary windings are added to the high frequency transformer’s secondary.

In addition to advantages like resonance and clamping capacitors, multi-output concept is also incorporated in the active clamp ZVS flyback converter to obtain multiple outputs with same component count. The converter hardware prototype and its results obtained are discussed in detail.

6.4.1 Principle of Operation

The actively clamped ZVS multi-output flyback converter is shown in Fig. 6.17. The transformer of this topology is designed for two outputs to obtain a multi-output converter with actively clamped ZVS. The explanation of circuit for secondary-2 is same as secondary-1 explained in section 6.2. The converter is powered by a DC voltage of 12V.
6.4.2 Modes of Operation

Modes of operation of the converter are same as those explained in section 6.2.2. The waveforms obtained are also similar to that given in Fig. 6.3. The secondary capacitor and diode waveforms for secondary-2 is same as secondary-1.

6.4.3 Design

The specifications and design aspects of the power supply are discussed in detail in this section.

6.4.3.1 Specifications

Converter Specifications:

Switching frequency \( (f_s) = 50 \) kHz

Input Voltage \( (V_{dc}) = 12 \pm 15\% V \)

Output power = 1.9W

Outputs = 2.8V / 0.28A, 3.3V / 0.33A
6.4.3.2 Parameters design

Resonant inductor, resonant capacitor, coupling capacitor, transformer primary and secondary-1 designs are same as those given in section 6.2.3. The design details for the transformer secondary-2 is $N_{s2} = 15$.

6.4.4 Open-loop Simulation Results

The simulation is carried out in the PSIM platform with the designed values. The switch pulses are same as shown in Fig. 6.4(b) and (c). Fig. 6.18(a) and (b) show the output voltage and current as per designed specifications (2.8V, 280mA and 3.3V, 330mA). The switch voltage and current waveforms, the resonant waveforms and diode-1 voltage and current waveforms obtained are same as the waveforms presented and explained in section 6.2.4. The input voltage applied is 12V. The duty cycle of switches $S_1$ ($V_{S1-pk} - 23.6V$ and $I_{S1-pk} - 0.8A$) and $S_2$ ($V_{S2-pk} - 23.6$ and $I_{S2-pk} - 0.8A$) are 47% and 46% respectively. From the simulated results, the observed peak values are coupling capacitor voltage ($V_{Cc-pk} - 11.7V$), resonant inductor current ($I_{Lr-pk} - 2.4V$), resonant inductor voltage ($V_{Lr-pk} - 10V$), diode 1 voltage ($V_{D1-pk} - 8.4V$), diode 1 current ($I_{D1-pk} - 1.3A$), diode 2 voltage ($V_{D2-pk} - 8.9V$) and diode 2 current ($I_{D2-pk} - 1.35A$). The diode 2 details are shown in Fig. 6.18(c).
6.4.5 Experimental Results

Based on the specifications, an experimental model of actively clamped ZVS multi-output flyback converter is implemented and the implementation details are similar to the details explained in section 6.2.5. Fig. 6.20(b) shows the hardware setup. The output voltage and current obtained in hardware (2.8V, 280mA and 3.68V, 334mA) are shown in Fig. 6.19(a) and (b). The voltages and current waveforms across and through the switches, diodes and resonant elements are similar to the waveforms explained in section 6.2.5. Diode-2 current ($I_{D2-pk} = 531mA$) and voltage ($V_{D2-pk} = 7.2V$) waveforms of secondary-2 is as viewed in Fig. 6.20(a). The voltage across the switches $S_1$ and $S_2$ are $V_{sw1-pk} = 12.7V$ and $V_{sw2-pk} = 7.2V$ and current through the switches are $I_{sw1-pk} = 138mA$ and $I_{sw2-pk} = 1.07A$ respectively. The coupling capacitor voltage obtained is 9.8V. The resonant inductor current and voltage obtained is 2.4A and 29.6V respectively. By adding multiple secondary windings with
high frequency isolation, transformer multi-output are easily obtained. Multi-output converters are less costly and are more compact than ‘n’ number of single output converters.

![Fig: 6.19 (a) Output-1 voltage and current (b) Output-2 voltage and current](image)

The drawback of this converter is the voltage stress in the diodes which is addressed by voltage doubler circuit in the following section.

6.5 Active Clamp ZVS Multi-output Flyback Converter with Voltage doubler

To obtain a compact circuit with reduced voltage stress in switches specifically suitable for low power applications - the active clamp circuit, voltage doubler circuit and multi-output are combined to form a modified
topology. Actively clamped ZVS multi-output flyback converter with voltage doubler is shown in Fig. 6.21. The voltage doubler circuit in secondary-2 consists of capacitor \( C_{s2} \), and diodes \( D_3 \) and \( D_4 \). The circuit explanation for secondary-2 is same as secondary-1 explained in section 6.3. When the main switch is turned OFF, the voltage spike in the flyback converter due to the transformer leakage inductance is very high. The auxiliary switch and the clamp capacitor used in the designed converter minimize this effect.

![Image of actively clamped ZVS multi-output flyback converter with voltage doubler](image)

**Fig: 6.21 Circuit diagram of actively clamped ZVS multi-output flyback converter with voltage doubler**

### 6.5.1 Modes of Operation

The modes of operation and theoretical waveforms of the converter are same as explained in section 6.3.1. The working of the additional secondary winding added for obtaining the multi-output is similar to the first secondary winding circuit.

### 6.5.2 Design and Specification

The design of the resonant part of the converter is same as active clamp ZVS flyback converter - explained in section 6.2.3. The design of
the secondary side of the converter is same as single output voltage doubler and multi-output ZVS PWM flyback converter which is discussed in sections 6.3.2 and 6.4.3 for outputs of -3.3V, -0.33A and -5V and -0.5A. The transformers, resonant inductor, resonant capacitor, coupling capacitor designs are same as given in section 6.2.3 and 6.4.3. The secondary capacitor calculation is as given in section 6.3.2.

6.5.3 Open-loop Simulation Results

The PSIM software is used for the simulation of the converter with the design specifications. Output voltage and current, as per design specifications, are given in Fig. 6.22(a) and (b). The output voltage-1 obtained is 3.3V and current is 330mA; similarly, the output voltage-2 obtained is 5V and current-2 is 500mA. Switch voltage, current waveforms and resonant waveforms are same as those explained in section 6.2.4 and the secondary part is same as that in section 6.3.3. The secondary capacitor voltage and current for secondary-1 is shown in Fig. 6.23(a). The diode voltage and current for secondary-1 and 2 are same as those given in Fig. 6.14(a) and (b). Input voltage supplied is 12V.

The duty cycles of the two switches S₁ and S₂ are 47% and 46% respectively. The voltage and current for both switches are the same with peak magnitude of 23.6V and 0.8A. The coupling capacitor peak voltage obtained is 11.7V. The resonant inductor peak current and voltage are 2.4A and 10V. The diode voltages for D₁, D₂, D₃ and D₄ are 4.5V, 3.4V,
5V and 3.4V, and the currents are 2.4A, 2.8A, 2.4A and 1A respectively. The diode-3 and diode-4 voltages and currents are shown in Fig. 6.23(b) and (c).

Fig: 6.22 (a) Output-1 voltage and current (b) Output-2 voltage and current

Fig: 6.23 (a) Secondary-1 capacitor voltage and current (b) Diode-3 voltage and current with switch-1 pulse (c) Diode-4 voltage and current with switch-1 pulse
An actively clamped multi-output flyback converter with voltage doubler circuit designed has all the advantages of resonance, clamping capacitance, multi-output and voltage doubler, hence a closed loop implementation of the converter is carried out with analog controller IC UC3825. The design details and the controller IC implementation are as explained in the next section.

### 6.5.4 Hardware Open Loop Results

An actively clamped ZVS multi-output flyback converter with voltage doubler model is implemented with the designed values and the implementation details are similar to that explained in section 3.4.1, 3.4.2 and 5.4.4. Fig. 6.24(a) shows the hardware setup. Fig. 6.24(b) and (c) shows the output voltages (3.3V and 5V) and current (330mA and 500mA) obtained as per design specifications. The diode voltage and current for secondary-1 is same as that given in Fig. 6.16(a) and (b) and secondary-2 diode voltages and current are shown in Fig. 6.25(a) and (b). The peak diode voltages and currents for D₁, D₂, D₃ and D₄ are 7.6V, 7.2V, 7.2V, 7.6V and 1.22A, 1.92A, 2.3A, 2.08A respectively. The currents and voltages of S₁ and S₂ are same with magnitudes 0.8A and 23.6V. The coupling capacitor voltage obtained is 11.7V. The resonant inductor current and voltage are 2.4A and 10V, while the secondary capacitor voltage and current obtained are 2.13V and 3A.
6.5.5 Closed Loop Implementation

Closed loop is essential for obtaining a regulated output voltage during load variation. Fig. 6.26(a) illustrates the closed loop simulations carried out with PI controller to verify the controller results, before hardware implementation. The hardware implementation of the PI controller is carried out with IC UC3825 as shown in Fig. 6.26(b) and the obtained simulation and experimental results are presented and discussed in detail.
6.5.5.1 Simulation Results

For the designed PI controller and analog controller IC UC3825, with a load variation of ±20%, the regulated output voltage obtained is as noticed in Fig. 6.27(a) and (b) respectively. The PI controller designed using PWM controller IC UC3825 regulates the output voltage for load variations. From the figures we can infer that the output voltage is regulated for the load variations.
6.5.6 Experimental Results

The waveforms obtained from closed loop hardware implementation are discussed in this section. UC3825 is used as analog controller to produce the closed loop pulses for the converter. Design details are same as explained in section 3.4.1 and 3.4.2 for a $D_{\text{max}}$ of 0.9 and $f_S$ of 100kHz. The designed values are $R_t = 3.3K\Omega$ and $C_t = 4.36nF$. The output voltage of the converter is compared with reference voltage generated in IC and the pulse generated by error detector and compensator is fed back to the converter switches. IC TLP250 optocoupler is used for the isolation of power circuit from the gating circuit.

The closed loop circuit diagram with PWM controller IC UC3825 is as noticed in Fig. 6.26(b). The working and design of the startup circuit is as explained in section 3.4.2 and the designed values are $R_8 = 7.8k\Omega$ and $R_5 = 140\Omega$. 

Fig: 6.27 Regulated output voltage-1 from (a) PI controller (b) PWM controller IC UC3825
In Fig. 6.28(a) the gating pulses obtained from the IC for both the switches are given for rated conditions. Fig. 6.28(b) shows the saw tooth waveform obtained from the IC for twice the switching frequency (100kHz).

6.5.6.1 Load transients

Fig. 6.29(a) and (b) shows the unregulated output voltage and current-1 waveforms for ±20% load-1 variations. Similarly the regulated output voltage and current-2 waveforms for same load variations are depicted in Fig. 6.30(a) and (b).
From these waveforms it can be concluded that, when disturbance is given to any load the current and voltages are disturbed and both settle to a new value for the unregulated output, while the regulated output observes a constant voltage. The output voltages for ± 20% load-2 variations, as shown in Fig. 6.31, clearly proves the stringent nature of output-2 for load variations. The change in output voltage from the desired value is calculated to be 980mV, 225mV for outputs 1 and 2 respectively.

**6.5.6.2 Line transients**

The response of the converter for ±15% supply variations are shown in Fig. 6.32 and 6.33. The analog controller regulates the output
voltage-2 through the feedback network, compensator, etc. The hardware prototype of the closed loop system is displayed in Fig. 6.34. The change in output voltage from the desired value is calculated to be 1.02V, 355mV, for outputs 1 and 2 respectively.

![Fig: 6.32 Unregulated output-1 voltage and current for supply voltage (a) increase (b) decrease](image)

![Fig: 6.33 Regulated output-2 voltage and current for supply voltage (a) increase (b) decrease](image)

![Fig: 6.34 Hardware set up for closed loop implementation](image)
6.6 Fuzzy Controller

This section deals with the simulation and hardware implementation of the converter with Conventional Fuzzy Logic Controller (CFLC) and Single input Fuzzy Logic Controller (SFLC). The basic concept behind Fuzzy Logic Controller is to utilize the expert knowledge and experience of a human operator for assigning a controller in controlling an application process. Mamdani and Takagi Sugeno types are the two main typical fuzzy control systems. In Mamdani type, fuzzy sets are used and hence it is well suited for applications whose membership ranges cannot be well defined. The output membership function in Sugeno is either a constant or a linear function of input variables. It is a computationally efficient method and works well with linear techniques like PID control. For applications where the nonlinearities are not predictable, Mamdani technique is a better option and hence it is opted for simulation and implementation.

6.7 Simulation of CFLC

The overall simulation circuit diagram of the converter is given in Fig. 6.35. This controller utilizes two inputs; the error and its change. Output of the controller is the change in pulse width for the switches of the converter. The converter operates in constant frequency mode and hence the change in pulse width from the previous value is detected by
the controller for - the error $e(k)$ and change in error $ce(k)$ present at that particular instant. They are calculated as follows:

$$e(k) = V_{ref} - V_0(k)$$  \hfill (6.1)

$$ce(k) = e(k) - e(k - 1)$$  \hfill (6.2)

Fig: 6.35 Closed loop simulation circuit using fuzzy logic controller

Where error $e(k)$ is the difference between the reference and output voltage at the $k^{th}$ instant and the change in error $ce(k)$ is the difference between the error at the $k^{th}$ instant and its previous instant $k-1$. The rules of the fuzzy controller are designed from the open loop analysis of the converter for various load and line variations. For ease of control, three variables are chosen using trapezoidal function and are named as NB (negative big), Z (zero) and PB (positive big). The membership
functions chosen are depicted in Fig.6.36 and the rules assigned are tabulated in Table.6.2.

**Table 6.2 Rule table for two input fuzzy logic controller**

<table>
<thead>
<tr>
<th>Change in error (ce)</th>
<th>Error (e)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>PB</td>
</tr>
<tr>
<td>Z</td>
<td>Z</td>
</tr>
<tr>
<td>PB</td>
<td>Z</td>
</tr>
<tr>
<td>Z</td>
<td>NB</td>
</tr>
<tr>
<td>Z</td>
<td>NB</td>
</tr>
</tbody>
</table>

(a) Membership functions for error (e(k))
(b) Membership functions for change in error (ce(k))
(c) Surface view

Fig: 6.36 Membership functions for error and change in error for two input fuzzy logic controller and the surface view

The rules derived for the closed loop operation of the circuit are:

i) When the output voltage is very less than the reference value (negative big), the pulse width has to be high enough, to bring the output to the reference value (output has to be positive big).
ii) When the output voltage is approaching the reference value (near zero), the pulse width has to be maintained at the same value as the output is near to the reference value (output has to be zero).

iii) When the output voltage is higher than the reference value (positive big), then the pulse width has to be lowered to bring the output to the reference value (output has to be negative big).

The weighing factor is obtained by Mamdani minimum fuzzy implication of the input membership functions. Centroid value of the output membership function is obtained from Table 6.2. Defuzzification method used is the centre of gravity. It is observed from the membership table that there is skew symmetry over the diagonal.

**6.8 Simulation of SFLC**

As discussed in CFLC, there exists skew symmetry in the CFLC rule table. Hence, the modified version of CFLC, that is, SFLC is proposed as the digital controller technique. The magnitude of the output signal is calculated approximately based on the distance from the main diagonal in the rule table. Similar to the CFLC, trapezoidal membership functions with three linguistic variables (NB, Z, PB) for error e(k) and one output linguistic variable (O) are choosen as depicted in Fig. 6.38 and in Table 6.3. The inference and defuzzification is same as discussed in CFLC. From Fig. 6.38(a) and (b), it is observed that the performance of the converter for CFLC and SFLC are more or less the same except that
the rules are reduced in SFLC and obviously the memory space is less utilised. Hence, SFLC is considered for hardware implementation. It is also wise to select more membership functions to increase the regulation of the converter and its performance. The resonant waveforms obtained are displayed in Fig. 6.38(c).

Fig: 6.37 Membership functions for error in SFLC

Table 6.3 Rule table for single input fuzzy logic controller

<table>
<thead>
<tr>
<th>Error(e)</th>
<th>NB</th>
<th>Z</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>PB</td>
<td>Z</td>
<td>NB</td>
</tr>
</tbody>
</table>

Fig: 6.38 Converter output for (a) CFLC (b) SFLC (c) resonant waveforms
6.8.1 **Hardware Implementation using Digital Controller**

An experimental model of actively clamped ZVS multi-output flyback converter with voltage doubler is implemented using digital controller. Power MOSFETs IRF840 are used as active switches. Ultra fast recovery rectifier IN5817 is used as the secondary diode. The rules created in SFLC are stored in LPC2140 in the form of a look up table. Output of the converter is fed to the ADC of the keil kit through a potential divider circuit. This output is then compared with the reference value and based on the error produced, its corresponding output function $O$ is selected from the look up table. The pulses produced are then passed through an opto-coupler MC2TE to isolate the ground between the two switches. Fig. 6.39 (a) and (b) show the output voltages and currents obtained as per design specifications (3.3V, 0.33A and 5V, 0.5A).

![Output Waveforms](image)

**Fig: 6.39 (a) Output-1 voltage and current (b) Output-2 voltage and current (c) hardware model**

Fig. 6.40(a) and (b) show the resonant waveforms. It is observed from Fig. 6.40(a) that the main switch is turned ON at zero crossing of the
capacitor voltage thus achieving ZVS condition. The mean voltage across the coupling capacitor was observed to be 7.88V and its corresponding peak value is 9.4V as displayed in Fig. 6.40(b).

Fig: 6.40 (a) Resonant capacitor voltage and current with switch-1 pulse. (b) Coupling capacitor voltage with switch-2 pulse

6.8.2 Load Regulation

The effect of increase and decrease in the second load resistor is depicted in Fig. 6.41 and Fig. 6.42 respectively. The former shows the regulated second output voltage and current (5V, 0.5A), while the latter displays output voltages 1 & 2. The outcome of output voltages for increase and decrease in first load resistor is shown in Fig. 6.43(a) and (b). From Fig. 6.41 to 6.43, it is observed that the second output voltage is maintained constant by the controller action for load resistor change in both load-1 and 2. The change in output voltage from the desired value is calculated to be 930mV and 120mV, which is lesser than that of the analog controller output deviation as discussed in section 6.5.6.1. Thus, the controller effectively works in regulating the output voltages for load disturbances.
Working of the controller for load variations is explained in the following steps. The same steps are applicable for line regulation also.
(i) When there is a sudden increase in the load resistance (either 1 or 2) output voltage-2 increases from the set point and its corresponding error calculated is positive big (PB). From Table 6.3, the controller selects the output pulse width as negative big (NB). This in turn reduces the pulse width of the switching pulses, thus bringing down the output voltage to a value lesser than the previous instant.

(ii) When the output voltage is approaching the reference value (near zero (Z)), the pulse width has to be maintained at the same value as the previous output state. Hence, the controller selects the output pulse width as zero (Z). This maintains the previous pulse width for the switches.

(iii) When the output voltage is lesser than the reference value (i.e) when there is a sudden decrease in load resistance, error becomes negative big (NB). From table 6.3, the controller selects the output pulse width as positive big (PB). This in turn increases the pulse width of the switching pulses, thus bringing up the output voltage to a greater value than the previous instant.

6.8.3 Line Regulation

Fig. 6.44(a) shows the regulated secondary-2 voltage and current for increase in supply voltage, and corresponding voltage and current for decrease in supply is shown in Fig. 6.44(b). It is observed that the controller is responding for variations in supply voltage as well. The effect
of supply voltage increase and decrease on both output voltages is shown in Fig. 6.45(a) and (b) respectively. It is clear from the figure that the second output voltage is regulated for both supply voltage variations while the variation in the first output is seen clearly from the waveform. The change in output voltage from the desired value is calculated to be 430mV and 90mV, which is lesser than that of the analog controller output deviation as discussed in section 6.5.6.2.

(a)                                                       (b)
Fig: 6.44 Regulated second output voltage and current for supply voltage (a) increase (b) decrease

(a)                                                   (b)
Fig: 6.45 Output voltages for supply voltage (a) decrease (b) increase

6.9 Converter analysis

To analyse the advantages of active clamp ZVS converter the performance of other flyback topologies of same power ratings are
compared. The waveforms and comparison tables are presented and analysed in this section.

**6.9.1 Topology Comparison**

In Fig. 6.46 (a) and (b), the voltage across switch for both flyback ZVS and actively clamped flyback ZVS topologies are shown. It is observed that the voltage across the switch in ZVS topology is higher by 40V than that of active clamp topology. Similarly, the secondary diode peak current is half and diode peak voltage is 3V less than that of the ZVS topology.

![Graph](image)

**Fig: 6.46 Voltage across switch for (a) ZVS flyback (b) Actively clamped ZVS flyback**

The active clamp ZVS single output flyback converter, flyback ZVS and hard switched flyback converters are considered for the comparison and the results obtained are tabulated in Table 6.4. From the comparison table, it is clear that in the active clamp ZVS flyback converter the voltage stress across the switch is 24V, while that of ZVS
topology is 65V and also the efficiency is 77%, which is more than that of ZVS topology (47%). This topology has a voltage stress ten times lesser and the efficiency is found to be more than double - than that of hard switched topologies. The active clamped circuit introduced in the flyback ZVS converter reduces the switch voltage and current stress. Also, the reduced switching losses and absence of RCD snubber in secondary diodes, leads to higher efficiency than that of conventional flyback converter and ZVS topologies.

**TABLE 6.4 Comparison between flyback, flyback ZVS and actively clamped flyback**

<table>
<thead>
<tr>
<th>Parameters used</th>
<th>Flyback</th>
<th>Flyback ZVS</th>
<th>Active clamped flyback</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of switches</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>No. of inductors</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>No. of capacitors</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>No. of diodes</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Output current (A)</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Switch Voltage stress (V)</td>
<td>$8.7\times10^4$</td>
<td>65</td>
<td>24</td>
</tr>
<tr>
<td>Secondary peak current (A)</td>
<td>2.6</td>
<td>4.7</td>
<td>2.4</td>
</tr>
<tr>
<td>Clamping capacitor voltage (V)</td>
<td>-</td>
<td>-</td>
<td>12.5</td>
</tr>
<tr>
<td>Diode voltage stress (V)</td>
<td>8.9</td>
<td>8.4</td>
<td>5.5</td>
</tr>
<tr>
<td>Secondary capacitor voltage (V)</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>42</td>
<td>47</td>
<td>77</td>
</tr>
</tbody>
</table>
6.9.2 Effect of Voltage Doubler

A comparative analysis is carried out for flyback topology with and without voltage doubler. From the analysis it is noted that the magnitude of voltages and current in the active switches, passive switches, inductors and capacitors in both topologies are the same and the differences observed are tabulated in Table 6.5. From Fig.6.47 it is also observed that the voltage doubler circuit does not affect the resonant and clamping waveforms. Comparison between output voltage and current obtained from the multi-output flyback active clamp circuit without (2.5V, 0.25A and 1.12V, 0.112A) and with voltage doubler (5V, 0.5A and 2.28V, 0.228A) are shown in Fig.6.48(a) and (b).

Similarly for a single output flyback active clamp circuit without (3.3V, 0.33A) and with voltage doubler (6.6V, 0.66A) are shown in Fig.6.48(c) and (d). Introduction of voltage doubler rectifier in the transformer secondary doubles the secondary output voltage. The space utilized remains the same for both circuits with and without voltage doubler, that is, the inclusion of one extra capacitor and diode does not require additional space, resulting in same volume utilization. Therefore, the power density, which is the ratio of power to its volume, also increases in voltage doubler. Thus, the voltage doubler circuit is a compact model.
Fig: 6.47 Resonant waveforms of active clamp multi-output converters (a) without voltage doubler rectifier (b) with voltage doubler rectifier

Table 6.5 Voltage doubler circuit comparison

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Active clamp ZVS multi-output flyback</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>with VD</td>
</tr>
<tr>
<td>No. of switches/Diodes</td>
<td>2/4</td>
</tr>
<tr>
<td>No. of inductors/ capacitors</td>
<td>1/6</td>
</tr>
<tr>
<td>Output -1 voltage/ current</td>
<td>5V/1A</td>
</tr>
<tr>
<td>Output -2 voltage/ current</td>
<td>3.3V/0.33A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>91%</td>
</tr>
</tbody>
</table>
Fig: 6.48 Output waveforms of active clamp flyback (a) and (b) multi-output converters without and with voltage doubler rectifier (c) and (d) single-output converters without and with voltage doubler rectifier

6.9.3 Effect of Multi-output

The multi-output and single output active clamp ZVS topologies are compared and the results obtained are tabulated in Table 6.6. From the table, the following conclusions are derived:
In order to obtain multi-output DC voltage with isolation, multiple secondary windings are added to the high frequency transformer without much increase in size of the single output transformer.

- Two isolated switched mode power supplies are obtained from the same single unit hence they are compact and less expensive.

They are used in household appliances and communication systems.

**TABLE 6.6 Single and multi-output circuit comparison**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Active clamped ZVS flyback converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single output</td>
</tr>
<tr>
<td>No. of switches/ diodes</td>
<td>2/1</td>
</tr>
<tr>
<td>No. of inductors/ capacitors</td>
<td>1/2</td>
</tr>
<tr>
<td>Output -1 voltage &amp; current</td>
<td>5V/1A</td>
</tr>
<tr>
<td>Output -2 voltage &amp; current</td>
<td>-</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>77%</td>
</tr>
</tbody>
</table>

**6.9.4 Efficiency Analysis**

The efficiency analysis of active clamp topology is carried out at rated load conditions and the efficiencies obtained are tabulated in table 6.7. It is obvious from the table that the modified active clamp ZVS MO VD has higher efficiency when compared to other topologies.
Table 6.7 Efficiency comparison

<table>
<thead>
<tr>
<th></th>
<th>Active clamped ZVS Flyback</th>
<th>Active clamped ZVS Flyback VD</th>
<th>Active clamped Flyback ZVS MO</th>
<th>Active clamped Flyback ZVS MO VD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency (%)</td>
<td>77%</td>
<td>80%</td>
<td>85%</td>
<td>91%</td>
</tr>
</tbody>
</table>

6.9.5 Regulation Analysis

For switched mode power supply, the percentage regulation is a figure of merit. It is the deviation of the average DC output voltage ($V_o$) at the desired level from a regulated power supply ($V_s$) regardless of variable output loads and fluctuating input voltage resources.

The regulation of 2% and cross regulation of 4% at rated input and load conditions is observed for the active clamped ZVS multi-output voltage doubler controlled by the analogue controller UC3825. The same is about 1.1% and 2.5% for fuzzy controller. The wire connections in the experimental model implemented, increases the parasitic capacitance and inductance effect. This can be further reduced if the experimental prototype is fabricated on a Printed Circuit Board (PCB).

6.10 Conclusion

The active clamped ZVS multi-output flyback converter with voltage doubler has the combined advantages of multi-output converters, voltage doubler rectifier and active clamp circuits namely - compactness,
increased power density and reduced voltage stress in the ZV switch. This system is highly efficient as demonstrated and substantiated by simulation and experimental results. The combined techniques (active clamp, ZVS, multi-output and voltage doubler) introduced on the basic flyback converter results in a efficiency of 91% for low power applications; this proves the suitability of this modified converter for applications like CMOS circuits, TTL logic circuits and for powering robotic arm motors.

For load and line variation the corresponding closed loop implementation is performed and from the analysis it is concluded that the output voltage is maintained constant even against the supply or load variations. dsPIC30f3011, UC3825 and IC SG3525 are used to produce the open loop gating pulses and closed loop pulses for the two switches respectively. The results justify the design and it is observed that resonance is preserved for load and supply deviations. The efficiency of active clamp multi-output ZVS with voltage doubler has higher efficiency when compared to the other topologies and hence best suited for low power applications like aerospace and communication systems.