CHAPTER 4

NEURAL BASED OPTIMIZATION ANALYSIS OF DISTRIBUTED MEMS TRANSMISSION LINE PHASE SHIFTERS

The field of RF MEMS has grown rapidly over the last decade due to its tremendous potential to greatly enhance the performance of existing circuits such as phase shifters and switches, as well as the promise of new capabilities for low loss tuning. In nonlinear transmission lines since about 1960, a CPW transmission line is loaded with millimeter-wave Schottky diodes and is used in voltage-level pulse shaping, picoseconds level sampling and harmonic multipliers (Barker 1999). However, diode based periodically loaded lines are quite lossy at millimeter wave frequencies, due to the series resistance of the Schottky diodes and cannot be used in low loss phase shifters and wideband switches above 26 GHz. For these frequencies, MEMS bridges offer excellent performance with very low additional transmission line losses. In this work, neural model is proposed for the following analysis of distributed MEMS transmission line phase shifter.

- Optimization of Distributed MEMS Transmission Line (DMTL) phase shifter for maximum phase shift.
- Loss Analysis in Distributed MEMS Transmission Line Phase Shifter
4.1 INTRODUCTION

In distributed MEMS transmission line, a CPW transmission line is loaded periodically with MEMS bridges which results in analog control of the transmission line phase velocity and therefore used in true time delay phase shifter (Larson et al 1991). In addition to this, if the MEMS bridges are pulled down, the distributed transmission line results in a wideband switch. Traditional electronic phase shifters are generally built on GaAs and use MESFET’s (Schindler & Miller 1988) or pHEMT’s as switches. These devices switch between different line lengths or switch between different low and high pass filters to achieve the desired phase shift. Millimeter wave phased array is widely used in radar, missile guidance, satellite communication and so on. High isolation and low loss phase shifters are required for millimeter wave applications. MEMS phase shifter is very popular for its good properties such as small size, low weight, wide frequency band, low insertion loss, and easy integrated with microwave circuits. RF phase shifters are essential building blocks for phased array antennas in telecommunication and radar applications. To reduce cost and power dissipation and improve RF performance of such applications, much research about MEMS switch integration (as opposed to an active approach) is carried out currently.

In this work we propose an efficient approach based on neural network for optimization of DMTL phase shifter to obtain the maximum phase shift with minimum insertion loss. Based on the work of Rodwell et al for analysis of loss in distributed non linear coplanar waveguide line, we extend the work for optimization with maximum phase shift. A stand - alone model for optimization of DMTL phase shift is derived efficiently using ANN. The results from the neural models trained by LM algorithm are in very good agreement with the theoretical results derived by MATLAB.
4.1.1 Optimization of DMTL Phase Shifter

In order to carry out the optimization based on Nagra et al (Nagra & York 1999) for higher phase shift with minimal insertion loss, analytic expressions for both the phase shift per unit length and the insertion loss per unit length must be found. This must be used with the set of design constraint for optimization (Barker 1999). The constraints are as follows:

- The zero - bias loaded impedance $Z_{lu}$ is 48 $\Omega$ for higher phase shift. But this will increase the return loss and reduce the bandwidth for loaded impedance.

- The Bragg frequency (the upper frequency limit of the phase shifter) is set to 120 GHz in order to limit the return loss up to 10 dB for the frequency up to 60 GHz.

- The capacitance ratio ($C_r$) is chosen to be 1.2.

For the distributed MEMS transmission line, the MEMS bridge can be modeled as a shunt capacitor, resulting in a loaded line model as shown in Figure 4.1 in which $C_b$ is the shunt capacitance due to the MEMS bridge and $S$ is the periodic spacing of the bridges.

The phase shift is found to be (Barker 1999).

$$\Delta \phi = \omega \sqrt{L_i C_i} \left( \sqrt{1 + \frac{C_{b0}}{SC_i}} - \sqrt{1 + \frac{C_r C_{b0}}{SC_i}} \right)$$

(4.1)
where $L_t = C_t Z_0^2$ and $C_t = \sqrt{\varepsilon_{\text{eff}}/(\varepsilon Z_0)}$ are the unit length inductance and capacitance respectively of the loaded transmission line, $\varepsilon_{\text{eff}}$ is the effective dielectric constant of the unloaded transmission line, $c$ is the free space velocity and $C_r$ is the capacitance ratio (Barker 1999) and is found to be

$$C_r = \frac{Z_0^2 \left( \frac{1+S_{11}}{1-S_{11}} \right) - 50^2}{Z_0^2 \left( \frac{1-S_{11}}{1+S_{11}} \right) - 50^2}$$

(4.2)

$$Z_0 = \sqrt{L_t/C_t}$$

(4.3)

is the characteristics impedance of the unloaded transmission line. $C_{b0}$ is the bridge capacitance (Barker 1999) and is given by

$$C_{b0} = S \left[ \frac{L_t}{Z_{lu}} - C_t \right]$$

(4.4)

and $Z_{lu}$ is the upper bound of the characteristics impedance for the given reflection coefficient $S_{11}$ and is given by
\[ Z_{lu} = 50 \left( \frac{1 + S_{11}}{1 - S_{11}} \right)^2 \]  

(4.5)

### 4.1.2 Development of ANN Model

The MLP neural model as shown in Figure 4.2 has been successfully used to compute the phase shift per unit length in order for the optimization of distributed MEMS transmission line phase shifters. The input ranges are $20 \ \mu m \leq W \leq \mu m$, $Z_{lu} = 48 \ \Omega$, $f_B = 120 \ GHz$ and $C_r = 1.2$ with different values of effective dielectric constant for calculating the phase shift. Training an ANN involves presenting these data sets ($W$, $Z_{lu}$, $f_B$ and $C_r$) sequentially and/or randomly and correspondingly calculating the value of the phase shift.

![Figure 4.2 Proposed ANN structure for DMTL phase shifter analysis](image)

Differences between the target from MATLAB and the actual outputs of the neural model $\Delta \Phi$ are calculated through the network to adopt its weights. The adaptation is carried out after presenting each dataset $(W, Z_{lu}, f_B$ and $C_r)$ until the calculation accuracy of the network is deemed satisfactory to the intension. The criterion includes root mean square errors for all training set or the maximum allowable number of epochs to be reached.
After many trial two hidden layered neural model which provides high accuracy has been selected. The suitable network configuration was 5 x 14 x 8 x 1. This means that the number of neurons were 5 for the input layer, 14 & 8 for the first & second hidden layers respectively and 1 for the output layer. The hyperbolic tangent sigmoid was used for input and hidden layers and linear activation functions was used in output layer.

4.1.3 Results and Discussion

The proposed neural model was trained with four different training algorithms. When the performance of neural models are compared in terms of root means square error of training algorithms, the best results for training and test were obtained from the models trained with LM algorithm. In order to show the validation of the neural model the results of ANN model trained with LM algorithm and the results of MATLAB simulation for the phase shift for silicon, quartz and air substrate are compared. Using all equation specified in the second section, the phase shift per centimeter versus the center conductor width is calculated for DTMLs on silicon, quartz and air at 40 GHz for the specification listed as in the input ranges of the neural network. The DTML can be used as a true time delay (TTD) phase shifter since a change in the MEMS bridge capacitance changes the phase velocity of the line (Barker 1999).

Figure 4.3 shows the calculated phase shift per centimeter for CPW center conductor width at 40 GHz with the impedance for the corresponding center conductor given at the top of each plot. As can be seen from figure, the phase shift is much larger for narrow center conductor widths (high impedance). This is due to the larger loading capacitance per unit length, $C_{bo}/S$, needed to load the line to 48 $\Omega$ and the change in bridge capacitance (from $C_{bo}$ to 1.2 $C_{bo}$) has a larger effect on the phase velocity.
It is observed from the trained neural network result that for the same substrate, the two different total CPW widths gives the same phase shift for the same impedance. For instance, on air the 600 µm total width line with a center conductor width of 250 µm and the 1 µm total width line with a center conductor width of 467 µm have an impedance of 138 Ω and a corresponding phase shift of -110°/cm.

Figure 4.3 Comparison of calculated phase shift $\Delta \phi$ per centimeter versus CPW center conductor width (W) using MATLAB and neural results at 40 GHz (a) silicon (b) quartz (c) air. The impedance ($Z_0$) for the corresponding center conductor width is given on top each plot.
From Figure 4.3, we observed that there are very good agreement between the results of the neural model and the results computed by MATLAB for the phase shift calculation of DTML. This good agreement supports the validation of the neural model for the optimization analysis distributed MEMS transmission line phase shifters in terms of maximum phase shift.

From Table 4.1 it is clear that, on quartz the 500 µm total width line with a center conductor width of 100 µm and the 700 µm total width line with a center conductor width of 140 µm have an impedance of 122.77 Ω and a corresponding phase shift of -155°/cm. Those curves of silicon with 180 µm total width line is seen to hit zero degrees at a center conductor width of 92 µm, which corresponds to an unloaded impedance of 48 Ω resulting in $C_{bo}/S = 0$ and no phase shift.

Table 4.1  Comparison of phase shift and impedance parameter for the total CPW line width of 500 µm and 700 µm with 40 µm to 200 µm center conductor width

<table>
<thead>
<tr>
<th>Center Conductor Width W (µm)</th>
<th>Total CPW Line Width of 500 µm</th>
<th>Total CPW Line Width of 700 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Phase Shift $\Delta\Phi$ (°/cm)</td>
<td>Impedance $Z_o$ (Ω)</td>
</tr>
<tr>
<td>40</td>
<td>-218.74</td>
<td>161.62</td>
</tr>
<tr>
<td>80</td>
<td>-171.11</td>
<td>132.45</td>
</tr>
<tr>
<td>100</td>
<td>-154.81</td>
<td>137.31</td>
</tr>
<tr>
<td>120</td>
<td>-141.01</td>
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<tr>
<td>140</td>
<td>-128.88</td>
<td>122.70</td>
</tr>
<tr>
<td>160</td>
<td>-117.98</td>
<td>101.67</td>
</tr>
<tr>
<td>200</td>
<td>-98.62</td>
<td>91.15</td>
</tr>
</tbody>
</table>
4.2 LOSS ANALYSIS IN DISTRIBUTED MEMS TRANSMISSION LINE PHASE SHIFTER

In DTML, a CPW transmission line is loaded periodically with MEMS bridges which results in analog control of the transmission line phase velocity and therefore used in true time delay phase shifter (Larson et al 1991). When the analogue voltage is used between the centre conductor and the ground wire, the MEMS bridges will be pulled down for forming ‘up’ or ‘down’ states. As a result, the phase velocity is increased to change the phase shift (Rebeiz et al 2002). In addition to this, if the MEMS bridges are pulled down, the distributed transmission line results in a wide band switch.

In the proposed methodology, the detailed loss analysis for the optimization of DMTL to obtain the maximum amount of phase shift with minimum insertion loss is obtained by combined conformal mapping / neural modeling. Based on the work of Rodwell et al work for analysis of loss in distributed non linear coplanar waveguide line, we extend the work for optimization to achieve maximum phase shift.

4.2.1 Theory of Loss Analysis

For the case where the DMTL is constructed using a CPW line with center conductor width W and total width W+2G, the MEMS bridge is with the width w as shown in Figure 4.4 (a), $Z_0$ (characteristics impedance) and $\varepsilon_{r,\text{eff}}$ (effective dielectric constant) of CPW line can be calculated by the physical parameters using conformal mapping (Hoffmann 1987) and are given as

$$Z_0 = \frac{\eta_0 K(k)}{4\sqrt{\varepsilon_{r,\text{eff}}} K(k)}$$

(4.6)
\[ \varepsilon_{r,\text{eff}} = \frac{\varepsilon_r + 1}{2} \]  
\( \text{(4.7)} \)

\[ k = \frac{W}{S} \]  
\( \text{(4.8)} \)

\[ k' = \sqrt{1 - k^2} \]  
\( \text{(4.9)} \)

where \( W \) and \( S \) are the center conductor width and total width of the CPW line, respectively, \( \eta_0 \) is the free space impedance, and \( K(k') \) and \( K(k) \) are the complete elliptic integrals of the first kind and \( \varepsilon_r \) is the relative permittivity. Using these equations, the DMTL phase shifter can be designed to a set of specifications. Figure 4.4 (b) shows the top view of DMTL structure.

The transmission line loss for the unloaded CPW line is found from a conformal mapping technique (Barker 1999) and is given by

\[ \alpha = \frac{8.686 \times 10^{-2} R_s \sqrt{\varepsilon_{r,\text{eff}}}}{4 \eta_0 SK(k)K(k')(1 - k^2) \left[ \frac{2}{W} \left[ \Pi + \ln \left( \frac{4\Pi W (1 - k)}{t(1 + k)} \right) \right] \right] + \left[ 2 \left[ \Pi + \ln \left( \frac{4\Pi S (1 - k)}{t(1 + k)} \right) \right] \right] } \]  
\( \text{(4.10)} \)
where $t$ is the metal thickness, $R_s$ is the surface resistance given by

$$R_s = \sqrt{\prod f \mu_0 / \sigma}$$

and $\sigma$ is the conductivity of the metal (Hoffmann 1987). The load loss is calculated by multiplying $\alpha$ with the ratio of the unloaded impedance to the loaded impedance. The line loss is calculated from the above equation and then multiplied by the ratio of change in impedance to arrive at the loaded loss.

### 4.2.2 Development of ANN Model

The MLP neural model has been successfully used to compute the loss in order for the optimization of distributed MEMS transmission line phase shifters. The optimization analysis is carried out for silicon, quartz and air substrates with the total width of the CPW ($S$) chosen approximately $\lambda_d/8$ and $\lambda_d/5$ and the Bragg frequency ($f_B$) of 120 GHz. A total width of $\lambda_d/8$ is typical for CPW designs in order to limit radiation loss. The DMTL should not suffer from radiation loss and therefore a large total width, $\lambda_d/5$, is usable.

The input ranges are $f_B = 120 \times 10^{12}$ Hz, $180 \times 10^{-6}$ m $\leq S \leq 1000 \times 10^{-6}$ m, $Z_{lu} = 48$ $\Omega$, $C_r = 1.2$ and $20 \times 10^{-6}$ m $\leq W \leq 100 \times 10^{-6}$ m with different values of effective dielectric constant for calculating the loss. By presenting these datasets ($S, W, f_B, Z_{lu}$ and $C_r$) to the neural model, the phase shift values are calculated. Differences between the target value of loss $\alpha$ and the actual outputs of the neural model $\alpha_{ANN}$ are calculated through the network to adopt its weights. The adaptation is carried out after presenting each datasets ($S, W, f_B, Z_{lu}$ and $C_r$) until the calculation accuracy of the network is deemed satisfactory to the intension. The criterion includes RMS (root mean square) errors for all training set or the maximum allowable number of epochs to be reached.
4.2.3 Results and Discussion

Figure 4.5 show the comparison MATLAB (solid) and neural simulation (dashed) results with values overlie each other. Figure 4.5 (a) shows the calculated loss versus frequency for a 300 µm total width CPW line on quartz with a 100 µm wide center conductor ($Z_0=100$ Ω). The line loss is calculated from the Equation (4.10) for a metal thickness of 0.8 µm which, at 40 GHz, is 1.8 µm skin depths. However, according to the above equation, if the metal thickness is increased to 3 µm the loss would decrease by a factor of 1.15 independent of frequency. In order to show the validation of the neural model the results of ANN model trained with LM algorithm and the results of conformal mapping for the loss for silicon, quartz and air substrate are compared. Figure 4.5 (b) & (c) and (d) show the calculated loss at 40 GHz for the unloaded and loaded CPW line for silicon, quartz and air using the specification as in the input ranges for ANN model.

(a)                                                                 (b)

Figure 4.5 (Continued)
Figure 4.5 (a) Transmission loss of unloaded CPW line versus frequency and loss versus CPW center conductor width for different values of total CPW width (b) silicon (c) quartz (d) air substrates for different total CPW line width

It is clear from the above figure that, the loaded line loss for silicon, with a 180 µm total CPW width, converges with the unloaded line loss at a center conductor width of 92 µm where the unloaded line impedance is 48 Ω and the capacitive loading goes to zero.