CHAPTER 7

CONCLUSIONS

7.1 OVERVIEW

In this Chapter, the highlights of the thesis and potential future research directions are provided.

The synopsis of this thesis lies in the design of suitable low power digital FIR filters for real-time signal processing applications. The filter structures proposed and algorithms designed are to be chosen that are hardware (mostly targeted for FPGA) realizable; dynamic power optimization being the most important constraint; suitable low power VLSI techniques for RTL synthesis, semi-custom design and transistor level design must be applied in each case to minimize power. All digital filters should be implemented in FPGA to test functionality, and power analysis is carried out in Xpower and HSPICE.

The Scope of the research work concentrates on the efficient measure for the implementation of MAC operation in a normal filter architecture using various proposed design techniques, here in my work efficient measure in terms of hardware complexity, delay and dynamic power dissipation are considered for RTL level synthesis model, Gate level synthesis model and mathematical representation of parallel FIR filter architecture.

7.2 CONCLUSIONS

The work done in this thesis is summarized below:

7.2.1 Algorithmic RTL Synthesized Low Power Model

A suitable filter architecture for RTL synthesized filter designed for signal
processing is designed using Modified folded architecture, Dynamic Distributed Arithmetic Algorithm, Sign Magnitude DAA and two-dimensional By-pass multiplier structure. The filter uses decimation filter followed by two filters, i.e., FIR filter followed by a corrector filter. Using efficient modified folded filter architecture, the filter structure is proposed for low power and hardware optimization with delay in throughput. Using Dynamic DAA method, the RNS number systems are used to represent large filter coefficients for real-time processing with existing n-tap FIR filters based on RNS-Binary conversion and back Binary-RNS number systems. For applications where multiplier-less filter implementation is required, the signed magnitude DAA for coefficient with signed numbers works well. Finally, the bypassing technique for general multipliers is utilized to reduced unnecessary switching transitions to reduce leakage and dynamic power when filters are constructed with the generic multiplier architecture. The FIR filter architecture constructed based on RTL synthesis model, and the power and delay are calculated using Xilinx Xpower analysis and the values are 7 mW and 5 ns, respectively. From these values, it is observed that the proposed FIR structure consumes lower power than the conventional FIR filter architecture, but still it is high due to the fact that filters are highly serial and latency is also very high. However, the use of ‘Distributed Arithmetic’ in the decimation filter certainly facilitates reduction of power compared to Canonical Signed Digit (CSD) approach already adopted in literature.

7.2.2 Semi-Custom based Low Power Model for Digital FIR Filter

The implementation of a digital filter using Booth-Wallace tree multiplier and Braun-array multiplier structure was implemented on 180 nm technology. This filter after getting implemented in transistor level successfully is tested for its power consumption. The power consumption is calculated using Microwind which comes out to be 60% reduction when compared to the traditional FIR filter. In most image processing applications where truncation error does not contribute to significance changes in the output performance, an optimized truncation error multiplexer based multiplier for low power design is proposed. The multiplier when used in the basic MAC operation using various number representations, proves to be power efficient than the traditional array multiplier exclusively used for image processing applications. It shows lower power consumption for Variable Correction Truncation (VCT) scheme among the other conventional truncation schemes such as Constant Correction Truncation (CCT) scheme. An adaptive filter using Booth-Wallace tree multiplier shows a reduction in power consumption when compared to a similar filter that
uses Booth multiplier and consumes 40 mW power on the same platform.

### 7.2.3 Transistor level integration for Low Power VLSI design

In this level, the transistor level technique for low power filter implementation for FIR filters is carried out. The power consumption is not less due to certain thermal constraints. A combination of both algorithmic level and circuit level for low power VLSI design reduces the power consumption in a digital filter. In VLSI circuit design, the clock consumes a lot of power due to existence of clock jitters and clock skew. Clock gating principle is applied to achieve low power. A novel low power detection unit based on clock gating principle was constructed to remove the existing detection logic with clocked registers in order to detect a redundant switching transition in a basic multiplier design. We have taken PIT based multiplier structures for constructing a basic filter design that reduces the number of multiplications which facilitates power reduction. This filter is implemented using the designed new low power latch. The power consumed by the detection unit is about 35 μW and 50 μW for clock-gating and D-latch methods, respectively. It is observed that a significant power reduction is achieved using AND-logic gate based detection unit to avoid redundant switching activity for a low power multiplier construction in a FIR filter design. Therefore, integration of circuit level approach and the algorithmic approach facilitates further reduction in power dissipation in the digital filter.

### 7.2.4 Low Power Full Adder Cell

Performance analysis of FIR filters are analyzed by constructing a low power multiplier with 16 types of 1-bit full-adder cells. The adder cell is anatomized into smaller modules. The adder and multiplier modules are studied and evaluated extensively. Sixteen different Novel 1-bit full-adder cells are constructed by connecting combinations of different designs of these modules. Several designs of multipliers with different combinations of full adders are developed, prototyped, simulated, and analyzed. Each of these cells exhibits different power consumption, speed, area, and driving capability. A library of full-adder cells is developed and presented to the circuit designers to pick the full-adder cell that satisfies these specific applications. Two realistic multiplier structures based on Braun-Array multiplier and Wallace tree multiplier were constructed from the low power Full adder module and maximum power Full adder module from the proposed Full adder library available in discussion. Finally, a low power FIR Filter was designed using the least power
multiplier architecture and full adder module.

7.2.5 Low Power parallel FIR Filter Design

The goal of this work is to reduce hardware complexity of higher order FIR filters used in multimedia or wireless communications whose filter order is very high (greater than 64-tap) with symmetric coefficients. The aim is to design efficient Fast FIR Algorithms (FFAs) for parallel FIR filter structure with the constraint that the filter tap must be a multiple of 2.

A brief discussion for \( L = 2, 3 \) and 4 parallel implementation schemes is made. The reduction in silicon area complexity is achieved by eliminating bulky multipliers with an adder, namely ripple carry and carry save adder. Overall, the proposed parallel FIR structures can lead to significant hardware savings for symmetric coefficients from the existing FFA parallel FIR filter, especially when the length of the filter is very large. The parallel FIR filter structure based on the proposed FFA technique has been implemented based on carry save and ripple carry adder for low power design optimization. In a 6-parallel 1024-tap filter, the proposed structure saves 14 multipliers at the expense of 10 adders, whereas for a six-parallel 512-tap filter, the proposed structure saves 108 multipliers at the expense of 10 adders. Overall, the proposed parallel FIR structures based on FFA technique can lead to significant hardware savings of nearly 30-50% for symmetric coefficients from the existing FFA parallel FIR filter, especially when the order of the filter is very high for complex applications.

7.2.6 Real-time hardware Validation

All filter structures are implemented in FPGA and power dissipation is calculated for all cases. The proposed parallel FIR filter of order 37 with symmetric coefficients and Branched Tree Adder (BTA) architecture are considered. This parallel FIR filter is considered for real-time validation, and is tested for real-time experimentation. The filter provides necessary amplification and frequency response in the case of removal of EMG signal form the Electro CardioGram (ECG) signal in real-time. Hence, it can be concluded that the proposed parallel FIR digital filter in conjunction with BTA architecture is a suitable choice for noise removal from ECG signal.
7.3 SCOPE FOR FUTURE WORK

Future study can be carried out in the following areas:

1. Detailed Dynamic power calculations for various abstraction levels discussed above can be made using Prime power, Encounter, Libero IDE, Xilinx Xpower Analyser, etc., from leading EDA Tools used in real-time design industry, and hence, possibility of power reduction at various design levels can be considered. Furthermore, a trade-off between area, speed and power can be brought satisfying the power constraints.

2. Either semi-custom or Full-custom ASIC design methodology can be adopted for low power digital filters proposed at various abstraction levels with low power multiplier structures and clock gating methods.

3. A more robust FIR filter structure (suitable for removal of EMG form ECG signals) can be investigated and VLSI design can be carried out.