CHAPTER 5

DESIGN OF DSTATCOM CONTROLLER FOR COMPENSATING UNBALANCES

5.1 INTRODUCTION

Distribution systems face severe power quality problems like current unbalance, current harmonics, and voltage unbalance, which have drawn much attention for their severity in the power systems. This Chapter proposes a phase sequence method for correcting the current unbalance problem. The unbalanced load currents are produced by unequal loads present in each phase of a three-phase system or a short-circuit fault or an open-circuit fault in the three-phase system. The unbalanced load draws negative sequence current from the source that makes the whole system unbalanced. One way of correcting this problem is to supply negative sequence load current by some compensating device at the load side. The Distribution Static Synchronous Compensators (DSTATCOMs) is capable of supplying the reactive power also; it can compensate the unbalance current by the design of an appropriate controller. This chapter explains the symmetrical component based Hysteresis Current Controller (HCC) design for a three-phase three-wire unbalanced system. The performance of the controller is studied by simulating the entire system in the MATLAB/ Simulink environment.

Distribution systems face severe power quality problems due to different types of linear and nonlinear loads such as the solid-state controllers, which draw harmonics and reactive currents from the AC mains. Power
quality problems in electrical systems mainly include voltage and current unbalance, flicker, harmonics, voltage sag, voltage dip, swell, and power interruption (Ghosh & Josh 2000, Haque 2001, Hingorani 1995, Jain et al 2004 and Mishra et al 2007). These may cause abnormal operation of the facilities or even trip the protection devices. Power quality issues especially voltage unbalance, current unbalance and current harmonics has drawn much attention of researchers. Providing reactive power compensation can correct these power quality problems. The remedial options reported in the literature for these problems include the DSTATCOM, the Dynamic Voltage Restorer (DVR) or the Static Synchronous Series Compensators (SSSC) and the Unified Power Quality Conditioner (UPQC). The generic name for these devices is custom power devices (Hingorani 1995, Rao et al 2008, Iyer et al 2005 and Molavi et al 2012). The DSTATCOM mitigates power quality problems by injecting current while the DVR mitigates power quality problems by injecting voltage. A UPQC is a combination of a DSTATCOM and a DVR that provides the solution for the power quality problems by injecting current as well as voltage. DSTATCOMs for three-phase four-wire systems with neutral conductor have been successfully developed at the customer end for unbalanced systems and reported in the literature (Lee & Wu 1993, Lee & Wu 2000 and Arsoy et al 2001). However, DSTATCOMs for three-phase three-wire systems are still under investigation. Balanced three-phase systems use the traditional Park’s transformation based methods for the design of the controllers.

The HCC method uses symmetrical components for designing the compensation circuit of an unbalanced system. This method transforms the asymmetrical voltages and currents into symmetrical positive sequence, negative sequence and zero sequence components of three-phase voltages or currents. The voltage unbalance is generally not as severe as the current unbalance. The unbalanced currents have a more severe impact on the loads
and the power system equipments. Hence, it is important to balance the unbalanced current to improve the power quality. A new and fast control technique is implemented in the DSTATCOM for compensating a three-phase three-wire unbalanced system. The system is built and simulated in the MATLAB / Simulink blockset.

5.2 PROBLEM FORMULATION

The power quality problem arises due to the unbalance current in the distribution system interrupting other users. Hence, it is necessary to solve the unbalance problem by suitable controller design for the compensators. This chapter investigates a new method to control the DSTATCOM to compensate for an unbalanced system. The controllers proposed in the previous chapters namely the PI controlled SPWM, the PI controlled SVPWM and the SVM based HCC are usually used for compensating a balanced system and are not suitable for compensating an unbalanced system. These methods fail to compensate an unbalanced system as these controllers are designed based on the dq transformation. The unbalanced system is created by opening any one phase of the three-phase system. When the system becomes unbalanced, load voltages and load currents also become unbalanced. These unbalanced voltages and currents affect other sensitive elements in the three-phase systems. It is necessary to reduce the impact of the unbalanced currents using the DSTATCOM custom device. By appropriate design of the controllers, the DSTATCOM reduces the negative impact of the unbalanced currents. The control system is demonstrated by simulation.
5.3 SYSTEM CONFIGURATION

The system shown in Figure 5.1 illustrates the performance of the controllers to compensate for an unbalanced load. The DSTATCOM is connected in shunt with the load while the rest of the system is simplified as an infinite utility voltage source with a source impedance of $Z_s (Z_s = R_s + j\omega L_s)$. The DSTATCOM, connected at the point of common coupling (PCC) through the coupling inductor $L$, employs a VSC to convert the DC-link voltage $V_{dc}$ of the capacitor to a voltage source of adjustable magnitude and phase. Therefore, the DSTATCOM can be treated as a controlled voltage-source. In some applications, due to the Norton equivalent, the DSTATCOM can also be considered as a controlled–current source. By providing a certain amount of reactive power, the DSTATCOM eliminates or mitigates the unwanted effects such as reactive power, harmonics, and unbalance in the load currents.

In a three-phase power system, voltages or currents are balanced if the amplitudes of the three-phase voltages or currents are equal and the phase-angles between the consecutive phases are equal to $2\pi/3$ radians. Two types of unbalance arise in a three-phase system. One is due to the unbalanced load, and the other is due to the unbalanced source. Power system generators or other unbalanced loads in the system cause the unbalanced voltage source. Unequal loads on each phase or open-circuit / short-circuit fault result in the unbalanced load. Hence, the load currents $I_L$ is not balanced in each phase and unbalanced currents are drawn from the utility. The DSTATCOM supplies the unbalanced currents to the unbalanced load to compensate for the load unbalance. Hence, balanced currents are drawn from the utility, thus improving the power quality of the system. Hence, the unbalanced load does not affect other loads connected to the system.
In Figure 5.1, the total load power is \( P_L + j Q_L \), the total source power is \( P_S + j Q_S \), and the total compensation power is \( P_C + j Q_C \). Equations (5.1) and (5.2) give the expressions for the power balance for the real and the reactive powers respectively

\[
P_L = P_S + P_C
\]

\[
Q_L = Q_S + Q_C
\]

where, \( P_L \) is the real power required by the load, \( P_S \) is the real power supplied by the source, \( P_C \) is the real power supplied by the DSTATCOM, \( Q_L \) is the reactive power required by the load, \( Q_S \) is the reactive power supplied from the source and \( Q_C \) is the reactive power supplied by the DSTATCOM. The reactive power supplied by the DSTATCOM can be controlled by operating the DSTATCOM in the inductive or capacitive mode.

### 5.4 PROPOSED COMPENSATION SCHEME FOR THE DSTATCOM

Figure 5.1 shows the three-phase three-wire distribution system with an unbalanced load and a DSTATCOM. As the load is unbalanced, the PI controlled SPWM or SVPWM methods cannot be used for compensation. A new controller for deriving the compensation scheme uses the method of symmetrical components. The reference currents obtained from this method are used in the HCC to compensate the unbalanced system.

The unbalanced load currents are extracted either from the power measured by the two-wattmeter method or by a fast power detection method (Chang & Yeh 2001, Chang & Yeh 2003, Chang & Yeh 2009). These methods are complicated, computationally intensive and indirect because the reference currents are extracted from the real and reactive power measurements. This Chapter proposes a new method in which the voltage and current sensors directly measure the voltages and currents respectively.
These measured quantities may have unequal values in each phase because of the unbalanced loads present in the system. According to the symmetrical components method, the unbalanced voltages and currents are transformed into a set of balanced quantities. The DSTATCOM output voltages are measured and transformed into positive and negative sequence voltages. Similarly, the load currents are measured and transformed into positive and negative sequence currents. Since the load is delta connected, only the positive and negative sequence components exist. First, the symmetrical components transformation matrix \([A]\) transforms the unbalanced load voltages into balanced symmetrical components. Equation (5.3) defines the general relationship between the line voltages and the positive, the negative and the zero sequence voltages. Similarly, Equation
(5.4) transforms three-phase load currents $I_{abc}$ into their symmetrical components

\[
\begin{bmatrix}
V_{ab} \\
V_{bc} \\
V_{ca}
\end{bmatrix} =
\begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
V^0 \\
V^1 \\
V^2
\end{bmatrix} = [A] \begin{bmatrix}
V^0 \\
V^1 \\
V^2
\end{bmatrix}
\]

\[ (5.3) \]

\[
\begin{bmatrix}
I_a \\
I_b \\
I_c
\end{bmatrix} =
\begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
I^0 \\
I^1 \\
I^2
\end{bmatrix} = [A] \begin{bmatrix}
I^0 \\
I^1 \\
I^2
\end{bmatrix}
\]

\[ (5.4) \]

where, \( \alpha = e^{j(\pi/3)} \) and

\[
[A] = \begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\]

Using Equations (5.3) and (5.4), the sequence components of the voltages and the currents are given in Equations (5.5) and (5.6) respectively

\[
\begin{bmatrix}
V^0 \\
V^1 \\
V^2
\end{bmatrix} = [A]^{-1} \begin{bmatrix}
V_{ab} \\
V_{bc} \\
V_{ca}
\end{bmatrix}
\]

\[ (5.5) \]

\[
\begin{bmatrix}
I^0 \\
I^1 \\
I^2
\end{bmatrix} = [A]^{-1} \begin{bmatrix}
I_a \\
I_b \\
I_c
\end{bmatrix}
\]

\[ (5.6) \]

where,

\[
[A]^{-1} = \frac{1}{3}
\begin{bmatrix}
1 & 1 & 1 \\
1 & a & a^2 \\
1 & a^2 & a
\end{bmatrix}
\]

By applying the symmetrical components transformation to the phase currents, Equations (5.7) and (5.8) transform the three-phase load currents to positive and negative-sequence components.

\[
I_E^1 = \frac{1}{3}[I_a + aI_b + a^2I_c]
\]

\[ (5.7) \]

\[
I_E^2 = \frac{1}{3}[I_a + a^2I_b + aI_c]
\]

\[ (5.8) \]
If the DSTATCOM is controlled to supply the required negative sequence currents, the currents drawn from the source remains balanced and other balanced loads on the system will not be affected.

To compensate for the load currents as fast as possible, the DSTATCOM should supply the entire negative-sequence load currents and the imaginary part of the positive-sequence load currents as soon as possible. Hence, the power source supplies only the real part of the positive-sequence load currents. Due to the delta-connected load, there will not be any path for the zero sequence currents in the three-phase three-wire system. Equations (5.9) to (5.11) give the command signals required for the current compensation. The DSTATCOM locally supplies the needed compensation currents for on-site load compensation.

\[
\bar{I}_{d} = lm(\bar{I}_{L}) + \bar{I}_{L}^2 \tag{5.9}
\]

\[
\bar{I}_{b} = a^2 lm(\bar{I}_{L}) + a \bar{I}_{L}^2 \tag{5.10}
\]

\[
\bar{I}_{c} = a lm(\bar{I}_{L}) + a^2 \bar{I}_{L}^2 \tag{5.11}
\]

The sequence-based controller for the unbalanced system, the magnitude and phase angle required for the control purpose are computed using Equations (5.12) to (5.14).

\[
i_{ca} = \sqrt{2} |\bar{I}_{d}| \sin (\omega t + \theta_a) \tag{5.12}
\]

\[
i_{cb} = \sqrt{2} |\bar{I}_{d}| \sin (\omega t + \theta_b - \frac{2\pi}{3}) \tag{5.13}
\]

\[
i_{da} = \sqrt{2} |\bar{I}_{d}| \sin (\omega t + \theta_c + \frac{2\pi}{3}) \tag{5.14}
\]
The PLL gathers the line frequency information at the PCC. The magnitude information is computed by comparing the actual capacitor voltage with the capacitor reference voltage and by controlling the error signal through a PI controller. Using these frequency and magnitude information signals, the sinusoidal current signals are generated as given by Equations (5.15) to (5.17). These three signals are compared with the three signals given in Equations (5.12) to (5.14)

\[
i_{ra} = |I_r| \sin(\omega t)
\]

(5.15)

\[
i_{rb} = |I_r| \sin(\omega t - \frac{2\pi}{3})
\]

(5.16)

\[
i_{rc} = |I_r| \sin(\omega t + \frac{2\pi}{3})
\]

(5.17)

where,

\[
|I_r| = K_p \Delta v_{dc} + K_i \int \Delta v_{dc} \, dt
\]

(5.18)

In order to keep the DC-link voltage of the DSTATCOM at the assigned level, the DSTATCOM needs to absorb a small amount of active power from the grid to meet the switching losses and charge the DC-link capacitor. A PI controller in the DSTATCOM regulates the instantaneous current for the active power balance $|I|$ of the DSTATCOM, as given by Equation (5.18). The Hysteresis Current Controlled inverter is used in the DSTATCOM for generating the compensation current and the overall compensation scheme of the DSTATCOM is now completed. Figure 5.2 shows the complete block diagram of the proposed unbalanced load compensation scheme for the DSTATCOM. The HCC is capable of directly controlling the output current of the DSTATCOM.
Figure 5.2 Block diagram of the controller of the DSTATCOM for an unbalanced load
5.5 SIMULATION RESULTS

The performance of the DSTATCOM’s controller is studied in simulation for compensating an unbalanced system. Figure 5.2 shows all the transformation blocks and the control blocks. Each block is mathematically modeled to study the effectiveness of the proposed DSTATCOM controller in the MATLAB/ Simulink blockset. The power circuits with power electronic switches namely the IGBTs are taken from the MATLAB/ Simpower system blockset. Table 5.1 gives the simulation parameters.

Table 5.1 Simulation parameters of the DSTATCOM for compensating unbalances

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Simulation Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Source voltage ( (V_s) ) in V</td>
<td>220</td>
</tr>
<tr>
<td>2</td>
<td>Frequency ( (f) ) in Hz</td>
<td>50</td>
</tr>
<tr>
<td>3</td>
<td>Filter inductor ( (L_f) ) in mH</td>
<td>15</td>
</tr>
<tr>
<td>4</td>
<td>Filter Resistors ( (R_f) ) in ( \Omega )</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>DC link Capacitor ( (C) ) in ( \mu F )</td>
<td>2200</td>
</tr>
<tr>
<td>6</td>
<td>Proportional gain ( (K_p) )</td>
<td>0.3</td>
</tr>
<tr>
<td>7</td>
<td>Integral gain ( (K_i) )</td>
<td>0.08</td>
</tr>
<tr>
<td>8</td>
<td>Load power ( (P_l +jQ_l) ) in VA</td>
<td>2400+j1800</td>
</tr>
<tr>
<td>9</td>
<td>Load power ( (P_c -jQ_c) ) in VA</td>
<td>2400-j1800</td>
</tr>
</tbody>
</table>

Simulation is carried out for two different cases, one with compensation for an unbalanced load, and the other one with a change of load from RC to RL.
5.5.1 Case 1: Compensation for an Unbalanced Load

For simulation studies, the unbalanced system is created by opening one of the phases of the three-phase system. Figure 5.3 shows the load current when the phase A is opened at time t = 0.2 s. Figure 5.4 shows that the DSTATCOM supplies the balanced compensation currents until t = 0.2 s and after that the compensator currents are unbalanced. The DSTATCOM is controlled to compensate the unbalanced load currents. Hence, the current drawn from the source is balanced at all the times, as shown in Figure 5.5. During the unbalanced load compensation, the compensator supplies the negative sequence load current as shown in Figure 5.6.

It is clear from Figures 5.7 to 5.9 that the voltage at the point of common coupling, the load voltages and the source voltages are balanced until t = 0.2 s and then the unbalance arises. Figure 5.10 shows the positive sequence load current that is equal to the sum of the positive sequence current from the source and the positive sequence current from the compensator. The active power required by the load is the sum of the active power from the source and the active power from the compensator as shown in Figure 5.11. However, the majority of the active power is supplied by the source. Similarly, Figure 5.12 shows that the reactive power required by the load is the sum of the reactive power from the source and the reactive power from the compensator, but the compensator supplies the majority of the reactive power.
Figure 5.3 Load currents $I_{abc}$

Figure 5.4 Compensation currents
Figure 5.5 Source currents $I_{abc}^S$

Figure 5.6 Negative sequence currents

$I_{L2} = I_{C2} + I_{S2}$
Figure 5.7 Unbalanced load voltages at the PCC

Figure 5.8 Source voltages
Figure 5.9 DSTATCOM voltages

Figure 5.10 Positive sequence currents
5.5.2 Case 2: Change in Load from RC to RL

The controller designed based on the phase sequence method has a very good performance for compensating the unbalanced loads. The same controller performance is studied for a balanced load that changes from RC to RL. Figures 5.13 to 5.17 show the performance of the DSTATCOM when the
balanced load changes from RC to RL. The load is varied from RC to RL at
time \( t = 0.05 \) s. When the load is balanced, and changes from RC to RL, the
power factor of the load changes from 0.8 leading to 0.8 lagging. Figure 5.13
shows the variation in the load current for this case. If the load is balanced, it
does not require any negative sequence current during the steady state
conditions, as shown in Figure 5.14. During the transition, when the load
changes from RC to RL, the load requires a negative sequence current. This
negative sequence current is supplied by the DSTATCOM, which keeps the
source current constant, as shown in Figure 5.15. If the DSTATCOM is not
present in the system, the RL (lagging power factor) load draws more power
that is reactive from the source. The DSTATCOM supplies the required
reactive power to the system and hence the current drawn from the source is
maintained constant, as shown in Figure 5.16. To keep the source current
constant during the load change, the DSTATCOM supplies the balanced
current with varying magnitude, as shown in Figure 5.15. During this
transition period, the voltage at the PCC also varies while during the steady-
state period, the voltage at the PCC is maintained constant as shown in
Figure 5.17.

![Figure 5.13 Variation in the load currents at t = 0.05 s](image)
Figure 5.14 Variation of the negative sequence currents

Figure 5.15 Variation of the DSTATCOM currents
Figure 5.16 Source currents

Figure 5.17 Variation of the bus voltage at the PCC for the change in load at $t = 0.05$ s
5.6 SUMMARY

The power quality improvement is important in a distribution system. In this Chapter, the unbalanced system behavior is studied and a phase sequence method is proposed for correcting the unbalanced current problem. The design and implementation of a DSTATCOM, for the unbalanced load compensation, for a three-phase three-wire system is studied in the MATLAB simulation environment. The symmetrical components based HCC method for the three-phase three-wire unbalanced systems has fast response. This method of control is suitable for unbalanced load compensation and for compensating the change of balanced load from RC to RL and vice-versa.