CHAPTER 3

MULTILEVEL INVERTER TOPOLOGIES AND MODULATION TECHNIQUES

3.1 INTRODUCTION

This chapter gives the brief description of conventional inverters with their advantages and disadvantages. Topologies of various multilevel inverters such as diode clamped, flying capacitor and cascaded H-bridge with their concepts are discussed. Modulation techniques such as space vector PWM, selective harmonic elimination and sinusoidal PWM are presented and their applicability for the different topologies is also discussed in this chapter.

3.2 CONVENTIONAL TWO LEVEL AND THREE LEVEL VOLTAGE SOURCE INVERTERS

Switched mode DC to AC inverters produce a sinusoidal AC output voltage whose magnitude and frequency can be controlled (Kajaer et al 2005). They are widely used in the area of AC induction motor drives. Half bridge inverter is the simplest topology which produces the two level square wave output voltage waveform. Circuit configuration of half bridge topology is given in Figure 3.1. To avoid shoot through fault, either switch $S_1$ or $S_2$ is turned ON at a time to give a load voltage, $V_{AO}$ of $+V_S/2$ as shown in Figure 3.1. To complete one cycle, $S_1$ is turned OFF and $S_2$ is turned ON to give a load voltage, $V_{AO}$ of $-V_S/2$. 
Figure 3.1 Two level voltage source inverter

(a) Half bridge configuration

(b) Output voltage waveform

(a) Full bridge configuration
Circuit configuration of full bridge topology is given in Figure 3.2. This topology is used to synthesize a three level square wave output voltage waveform. The three possible levels are given in Table 3.1. Neither $S_1$, $S_3$ nor $S_2$ and $S_4$ should be closed at the same time. If so, a short circuit will occur across the DC source.

**Table 3.1 Load voltage with corresponding conducting switches**

<table>
<thead>
<tr>
<th>Conducting Switches</th>
<th>Load Voltage VAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$ &amp; $S_4$</td>
<td>$+V_s$</td>
</tr>
<tr>
<td>$S_2$ &amp; $S_3$</td>
<td>$-V_s$</td>
</tr>
<tr>
<td>$S_1$&amp;$S_2$ or $S_3$ &amp;$S_4$</td>
<td>0</td>
</tr>
</tbody>
</table>

Some of the problems of classical inverters are summarized as follows:

- The entire DC voltage appears across each switch when it is OFF. This will be greater than the voltage rating of the individual devices.
• The devices will not automatically share the voltage in the OFF state because of the differences in their leakage currents. High value of parallel resistors can be used to overcome this static sharing problem.

• More seriously, the devices will not share the voltage during switching due to variations in switching speed. Special gate drive techniques and special snubber is required for dynamic sharing.

• Two level output causes very large voltage steps on the load which will create a problem for motor insulation.

• Harmonic content of the output voltage is larger for high switching frequency.

On the flip side, classical inverters too have finite advantages. They are,

• Standard PWM techniques can be used.

• Number of power circuit components is less as compared to other inverter circuits.

• Redundancy can be incorporated to improve reliability by using more series devices than actually required.

From the above discussion, it is clear that the conventional inverter have many drawbacks than merits. So alternative solution to meet the high power demand is through multilevel inverter concept.

3.3 MULTILEVEL INVERTER

Numerous industrial applications have begun to use high power apparatus in recent years. Some medium voltage motor drives and utility
applications require medium voltage and megawatt power levels. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel inverter structure has been introduced as an alternative in medium and high power applications (Jose Rodriguez et al 2007). With this type of inverters, improvements in the harmonic quality of the output voltage can be achieved. Multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for medium and high power applications (Venkatachalam Kumar Chinnaiyan et al 2013).

Multilevel inverter produces a desired AC voltage waveform from several levels of DC voltages. These DC voltages may be or may not be equal. AC voltage produced from these DC voltages is of stepped waveform. One drawback of using multilevel inverter is to approximate sinusoidal waveforms from stepped waveform. The staircase waveform produced by the multilevel inverter contains sharp transitions. Fourier series theory makes clear that this phenomenon results in harmonics, in addition to the fundamental frequency of the sinusoidal waveform (John Chiasson et al 2003).

The power quality of the power system is affected by the harmonics generated on the AC side. The power quality of the multilevel inverter is improved by performing the power conversion in small voltage steps. Multilevel inverter widely replaces the conventional two level three phase Voltage Source Inverter (VSI) by its performance such as lower switching stress (dv/dt) and lower THD on output voltage (Jose Rodriguez et al 2007).

The multilevel inverters start from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels is limited by voltage unbalance problems, voltage
clamping requirement, circuit layout and packaging constraints (Nabae et al 1981). A multilevel inverter has several advantages over a conventional two level inverter that uses high switching frequency PWM. The attractive features of a multilevel converter can be briefly summarized as follows:

- Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses. Therefore electromagnetic compatibility problems can be reduced.

- Multilevel inverters produce smaller CM voltage; Therefore, the stress in the bearings of a motor connected to a multilevel inverter drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation techniques.

- Multilevel inverters will draw input current with low distortion.

- Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

The main drawback of multilevel inverters is that the number of switches increases with the number of levels. In early stages of multilevel inverters, development of control circuitry for large number of power switches was a significant problem. But continuous evolution of CPLD, DSP and FPGA devices easily solved this inconvenience. Other drawback of this inverter is the requirement of multiple numbers of DC voltage sources, mainly provided by capacitors. Balancing the voltage sources during operation under different load conditions is an important challenge.
In spite of these drawbacks, introducing multilevel inverters will decrease switching losses occurred in the power device. By comparing with two level inverters, smaller size filter is required for the elimination of harmonics. This reduces the inverter weight, dimension and cost. Many multilevel inverter topologies have been proposed during the last two decades. Contemporary research has evolved novel inverter topologies and unique modulation schemes. Moreover, three different major multilevel inverter structures have been reported in the literature. They are,

- Diode clamped /Neutral clamped Multilevel Inverter
- Flying capacitors /Capacitor clamped Multilevel Inverter
- Cascaded H-bridge Multilevel Inverter

Abundant modulation techniques and control paradigms have been developed for multilevel inverters such as Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Elimination (SHE-PWM), Space Vector Modulation (SVM) and others (Jose Rodriguez et al 2002). Multilevel inverters replace the existing two level inverters from the applications such as power supplies, traction drive systems, industrial medium-voltage motor drives (Jose Rodriguez et al 2007), utility interface for renewable energy systems (Kajaer et al 2005) and Flexible Alternating Current Transmission System (FACTS) (Rajesh Gupta et al 2007).

3.3.1 Multilevel Concept

The concept of multilevel inverters has been introduced since 1975. However, the elementary concept of a multilevel inverter to achieve high power is to use a series of power semiconductor switches with several low voltage DC sources to perform power conversion by synthesizing a staircase voltage waveform. One phase leg of multilevel inverter is shown in
Figure 3.3. In this schematic diagram, operations of semiconductors are shown by an ideal switch with several states. The switching algorithms of switches and commutation of them allow the addition of the capacitor voltages as temporary DC voltage sources, whereas the semiconductors should withstand limited voltages of capacitors.

![Figure 3.3 One phase leg of a multilevel inverter](image)

Nearly for the three decades, multilevel inverters are being used in the world of power electronics. They are named by the number of voltage levels they generate and the different topologies they have. Usually the number of output voltage levels is odd instead of even. It means that the definition of a zero voltage level in the output of inverter, like in three level or in five level inverters, makes it more sinusoidal with less harmonics.

### 3.3.2 Diode Clamped Multilevel Inverter

Three phase eleven level diode clamped inverter is shown in Figure 3.4. Each phase of the inverter shares a common DC bus, which has been subdivided by five capacitors into six levels. The voltage across each
capacitor is $V_{dc}$ and the voltage stress across each switching device is limited to $V_{dc}$ through the clamping diodes. Switching states of diode clamped multilevel inverter is given in Table 3.2.

![Figure 3.4 Three phase eleven level structure of a diode clamped inverter](image)

Table 3.2 Diode clamped eleven level inverter voltage levels and corresponding switch states

<table>
<thead>
<tr>
<th>Voltage $V_{a0}$</th>
<th>$S_{a5}$</th>
<th>$S_{a4}$</th>
<th>$S_{a3}$</th>
<th>$S_{a2}$</th>
<th>$S_{a1}$</th>
<th>$S_{a'5}$</th>
<th>$S_{a'4}$</th>
<th>$S_{a'3}$</th>
<th>$S_{a'2}$</th>
<th>$S_{a'1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_5 = 5V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_4 = 4V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_3 = 3V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_2 = 2V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_1 = V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_0 = 0$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Table 3.2 lists the output voltage levels possible for one phase of the inverter with the negative DC rail voltage $V_0$ as a reference. Switch state condition one (1) means the switch is ON, and zero (0) means the switch is OFF. Each phase has five complementary switch pairs such that turning ON one of the switches of the pair requires that the other complementary switch be turned OFF (Alireza Nami et al 2011). The complementary switch pairs for phase leg-A are ($S_{a1}$, $S_{a'1}$), ($S_{a2}$, $S_{a'2}$), ($S_{a3}$, $S_{a'3}$), ($S_{a4}$, $S_{a'4}$) and ($S_{a5}$, $S_{a'5}$). The switches that are ON for a particular phase leg is always adjacent and in series. For an eleven level inverter, a set of five switches are ON at any given time. The resulting line voltage is an eleven level staircase waveform as shown in Figure 3.5. The line voltage $V_{a-b}$ consists of a phase leg-A voltage and phase leg-B voltage. This means that $N_L$ level diode clamped inverter has $N_L$ level output phase voltages and a $(2N_L - 1)$ level output line voltages.

![Figure 3.5 Line voltage waveform of eleven level diode clamped inverter](image)

Major advantages of diode clamped multilevel inverter are listed as follows:

- When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters.
Inverter efficiency is high because all devices are switched at the fundamental frequency.

The control method is simple.

Disadvantages of the diode clamped multilevel inverter can be listed as follows:

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to control the real power flow of the individual converter.

3.3.3 Flying Capacitor Multilevel Inverter

The structure of this inverter is similar to that of the diode clamped inverter. Instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure 3.6. This topology has a ladder structure of DC side capacitors. The voltage on each capacitor differs from that of the next capacitor (Anshuman Shukla et al 2008).

The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the flying capacitor based inverter is that it has redundancies for inner voltage levels. Unlike the diode clamped inverter, the flying capacitor inverter does not require all of the switches that are ON (conducting) in a consecutive series (Chunmei Feng et al 2007). Moreover, the flying capacitor inverter has phase redundancies, whereas the diode clamped inverter has only line-line redundancies. These redundancies allow a choice of charging and discharging
specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

![Figure 3.6 Three phase eleven level structure of a flying capacitor inverter](image)

In addition to the \((N_L-1)\) DC link capacitors, the \(N_L\)-level flying capacitor multilevel inverter will require \((N_L -1) \times (N_L -2)/2\) auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static var generation. Advantages of the flying capacitor multilevel inverter are summarized as follows:

- Provides switch combination redundancy for balancing different voltage levels.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.
On the flip side, flying capacitor multilevel has some disadvantages. They are,

- Control is complicated to track the voltage levels of all the capacitors. Also, pre-charging of all the capacitors to the same voltage level and startup are complex.

- Switching utilization and efficiency are poor for real power transmission.

- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode clamped converters. Packaging is also more difficult in inverters with a large number of levels.

### 3.3.4 Cascaded H-bridge Multilevel Inverter

Each Separate DC Source (SDCS) is connected to a single phase full bridge or H-bridge inverter (Anup Kumar Panda & Yellasiri Suresh 2012). A single phase structure of eleven level cascaded inverter is illustrated in Figure 3.7.

Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0 and $-V_{dc}$ by connecting the DC source to the AC output by different combinations of the four switches, $S_1$, $S_2$, $S_3$ and $S_4$. To obtain $+V_{dc}$, switches $S_1$ and $S_4$ are turned ON, whereas $-V_{dc}$ can be obtained by turning ON switches $S_2$ and $S_3$. By turning ON $S_1$ and $S_2$ or $S_3$ and $S_4$, the output voltage of zero is obtained. The AC outputs of different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs (Krishna Kumar Gupta & Shailendra Jain 2013).
Phase voltage waveform for eleven level cascaded H-bridge inverter is shown in Figure 3.8. The number of output phase voltage levels \( N_L \) in a cascaded inverter is defined by \( N_L = 2s+1 \), where \( s \) is the number of separate DC sources. Output phase voltage \( V_{an} \) is given in Equation 3.1.

\[
v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}
\]  
(3.1)
Major advantages of the cascaded inverter can be summarized as follows:

- The number of possible output voltage levels is more than twice the number of DC sources ($N_L = 2s + 1$).
- The series of H-bridges makes for modularized layout and packaging. This will make the manufacturing process to be done more quick and cheap.

Major disadvantage of the cascaded inverter is given below:

- It needs separate DC sources for real power conversions, thereby limiting its applications.
3.3.5 Component Requirements

Component requirements of diode clamped, flying capacitor and cascaded H-bridge multilevel inverters for number of levels is given in Table 3.3. From the Table 3.3, cascaded inverter requires the least number of components and has the potential for utility interface applications because of its capabilities for applying modulation and soft-switching techniques.

Table 3.3 Components required for different MLI topologies

<table>
<thead>
<tr>
<th>Components</th>
<th>Diode Clamped</th>
<th>Flying Capacitors</th>
<th>Cascaded H-bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Switching devices</td>
<td>(N_L-1) * 2</td>
<td>(N_L -1) * 2</td>
<td>(N_L -1) * 2</td>
</tr>
<tr>
<td>Main diodes</td>
<td>(N_L -1) * 2</td>
<td>(N_L -1) * 2</td>
<td>(N_L -1) * 2</td>
</tr>
<tr>
<td>Clamping diodes</td>
<td>(N_L -1) * (N_L -2)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DC bus capacitors</td>
<td>(N_L -1)</td>
<td>(N_L -1)</td>
<td>(N_L -1) / 2</td>
</tr>
<tr>
<td>Balancing capacitors</td>
<td>0</td>
<td>(N_L -1) * (N_L -2) / 2</td>
<td>0</td>
</tr>
</tbody>
</table>

The switching devices do not encounter any voltage-sharing problems. For this reason, multilevel inverters can easily be applied for high power applications. The system kV rating can be extended beyond the limits of an individual device through the voltage clamping techniques. So, diode clamped inverters are used more in high power motor drive applications (Dietmar Krug et al 2007). The intriguing feature of the multilevel inverter structures is their ability to scale up the kVA rating and also to improve the harmonic performance in the output voltage. By considering the cost of semiconductor switches and passive components, converter losses and simplicity of modulation schemes, cascaded H-bridge inverter is also a best choice for medium and high power applications (Shuai Lu & Keith Corzine 2007).
3.4 MODULATION TECHNIQUES

Modulation is the process of switching the power electronic device in a power converter from one state to another. All modulations are aimed at generating a stepped waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component that is usually sinusoidal in steady state. Each topology has different switching configuration to achieve commanded output voltage. Modulation strategies are responsible for synthesizing reference control signals and for keeping all voltage sources balanced. The requirements of multilevel modulation algorithm are as follows.

- Voltage quality should be good
- Modular design
- Simultaneous switching of multiple voltage levels is not allowed.
- Switching frequency of power devices should be minimized.
- Power modules should share the load equally.
- Control algorithm should be simple.
- Implementation cost should be low.

In many industrial applications, the output voltage of inverters should be controlled to overcome the changes in input voltage and to meet the need of voltage/frequency control. It is obvious that harmonics in the output voltage depend on the selected modulation technique. Using more number of semiconductor devices and switching redundancies, bring a higher level of complexity in multilevel topologies, when compared with a two level inverter.
However, this complexity can be used to improve the modulation technique, such as, minimizing the switching frequency, reducing the common-mode voltage or balancing the DC link voltages (Poh Chiang et al 2005). The modulation methods used in multilevel inverters can be classified according to switching frequency (Jose Rodriguez et al 2002) as shown in Figure 3.9.

Methods that work with high switching frequencies have many commutations for the power semiconductors in one cycle of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based Sinusoidal PWM that uses the phase shifting technique to reduce the harmonics in the load voltage (Ilhami Colak & Ersan Kabalci 2013). Another interesting alternative is the SVM strategy, which has been
used in three level inverters (Amit Kumar Gupta & Ashwin Khambadkone 2007).

Table 3.4  Applicability of modulation techniques for different multilevel inverter topologies

<table>
<thead>
<tr>
<th>Switching Frequency</th>
<th>Modulation Techniques</th>
<th>Multilevel Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NPC</td>
</tr>
<tr>
<td>High Frequency</td>
<td>SVM</td>
<td>Applicable</td>
</tr>
<tr>
<td></td>
<td>Level Shifted PWM</td>
<td>Applicable</td>
</tr>
<tr>
<td></td>
<td>Phase Shifted PWM</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Fundamental Frequency</td>
<td>SHE</td>
<td>Applicable</td>
</tr>
<tr>
<td></td>
<td>SVC</td>
<td>Applicable but not recommended</td>
</tr>
</tbody>
</table>

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Based on the switching frequency and modulation techniques, their applicability for different type of multilevel inverters are given in Table 3.4.

It must be noted that lower switching frequency usually means lower switching loss and higher efficiency. Representatives of this family are the multilevel selective harmonic elimination and the Space Vector Control (SVC). It is found that SVM and SHE are the most widely used modulation techniques for all the types of multilevel inverters (Damoun Ahmadi et al 2011). In continuation of the work done in the past few decades on switching frequency applied to these multilevel inverters, Table 3.5 is formulated. By
comparing the switching frequency for the medium and high power applications, fundamental switching frequency is selected to be best suited one.

Table 3.5  Comparison between fundamental switching frequency and high switching frequency

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Modulation Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Fundamental Switching Frequency</strong></td>
</tr>
<tr>
<td></td>
<td><strong>High Switching Frequency</strong></td>
</tr>
<tr>
<td>Switching loss</td>
<td>Low due to fundamental frequency</td>
</tr>
<tr>
<td></td>
<td>High due to frequent ON and OFF</td>
</tr>
<tr>
<td>Harmonic content</td>
<td>Output harmonic content is low</td>
</tr>
<tr>
<td></td>
<td>Output harmonic content is very low</td>
</tr>
<tr>
<td>Implementation of Control Algorithm</td>
<td>Easy implementation since driver circuit is simple</td>
</tr>
<tr>
<td></td>
<td>Complex driver circuit is required</td>
</tr>
<tr>
<td>Modularization</td>
<td>Applicable</td>
</tr>
<tr>
<td></td>
<td>Not applicable</td>
</tr>
</tbody>
</table>

3.4.1  Space Vector PWM

Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference (Govindaraju & Baskaran 2010). In SVM, the reference signal is generated from its closest signals. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state. This feature is used to balance the capacitor voltages (Govindaraju & Baskaran 2010, Amit Kumar Gupta & Ashwin Khambadkone 2007). Multilevel SVM must manage this behavior to optimize the search for the modulating vectors and apply an appropriate switching sequence (Wenxi Yao et al 2008). A conceptually different control method for multilevel converters, based on the space-vector theory, has been introduced, which is called space vector control.
3.4.2 Selective Harmonic Elimination

The popular selective harmonic elimination method is also called fundamental switching frequency method which is based on the harmonic elimination theory. The multilevel fundamental switching scheme inherently provides the opportunity to eliminate certain lower order harmonics by varying the times at which certain switches are turned ON and turned OFF. A staircase output voltage waveform is generated by switching ON and OFF the switching devices in the multilevel inverters once during one fundamental cycle. This diminishes the switching losses in the devices. In this method, each switch is turned ON and turned OFF once in a switching cycle and switching angles are usually chosen based on specific harmonic elimination or minimization of THD in the output voltage. Two ways to eliminate lower order harmonics are;

i) By increasing the switching frequency of SPWM and SVM in case of two level inverters or in multicarrier based phase shift modulation for multilevel inverters.

ii) By computing the switching angles using SHE techniques.

The first method of eliminating low frequency harmonics is limited by the switching losses and the availability of the voltage steps (Govindaraju & Baskaran 2010). SHE techniques comprises the mathematical modelling of output waveform and solving them for switching angles based on the amplitude of the fundamental wave of the output voltage, the order and number of the eliminated harmonics (Vassilios Agelidis et al 2008). Thus, the lower order harmonics are either eliminated or minimised while the higher order harmonics are filtered out in selective harmonic elimination method. Multilevel inverter can produce a quarter wave symmetric stepped voltage waveform synthesized from several DC voltages as shown in Figure 3.10.
By applying Fourier series analysis, the output voltage can be expressed as

\[ V(\omega t) = \frac{4}{n\pi} \sum_{h}[V_1 \cos(n\theta_1) + V_2 \cos(n\theta_2) + \ldots + V_h \cos(n\theta_h) + \sin(n\omega t)] \]  (4.3)

where, \( n = 1, 3, 5 \ldots \)

‘h’ is the number of DC sources and \( V_1, V_2 \ldots V_h \) are the level of DC voltages. The switching angles must satisfy the condition \( 0 < \theta_1 < \theta_2 < \ldots < \theta_h < (\pi/2) \). However, if the switching angles do not satisfy the condition, this method no longer exists. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to \( h-1 \) harmonic contents can be removed from the voltage waveform. In general, the most significant low frequency harmonics are chosen for elimination by properly selecting the triggering or switching angles and high frequency harmonic components can be readily removed by using additional filter circuits.
The switching angles of the inverter are computed by solving the transcendental equations reflecting each harmonics. A proper starting value of modulation index and initial guess is necessary to solve these equations. Solving these transcendental equations with n number of unknowns is a tedious job. But the switching angles can be calculated offline to eliminate the specific low order harmonics and also switching takes place at the fundamental frequency and hence minimizes the switching losses (Jason et al 2007). In other words, only a few commutations take place in one cycle increasing efficiency and enabling air cooling. The computation of the switching angle increases with the increase in the voltage levels. With a limitation for the switching angles to be within (\(\pi/2\)), it provides a narrow range of modulation index. This method is limited to open-loop applications and low dynamic performance demanding applications (Cheng et al 2006).

The main challenge associated with SHE-PWM technique is to obtain the analytical solution of the system of nonlinear transcendental equations that contain trigonometric terms which in turn provide multiple sets of solutions (Krikor et al 2008). This has been reported in numerous research papers (Faete Filho et al 2011). Several algorithms have been reported in the technical literature, concerning methods of solving the resultant nonlinear transcendental equations, which describe the SHE-PWM problem (Surin Khomfoi & Leon Tolbert 2007, Ayoub Kavousi et al 2012). A sequential homotopy based computation and ant colony algorithm has been done to solve for the switching angles (Sundareswaran et al 2007). The theory of symmetric polynomial, theory of resultant polynomials and the resultant theory have been proposed to solve the polynomial equations obtained from the transcendental equations (John Chiasson et al 2003). With an increase in the number of H-bridges connected in series, the computation increases as the order of the polynomials become very high. In Newton Raphson method of solving these transcendental equations, the switching angles can be computed
with negligible computation effort for any initial guess. This method is
derivative dependent and may end in local optima. Further, a judicious choice
of the initial values alone will guarantee convergence.

### 3.4.3 Sinusoidal Pulse Width Modulation

Sinusoidal PWM method is also known as the triangulation, sub harmonic, sub oscillation method, Carrier Based Pulse Width Modulation (CB-PWM) is very popular in industrial applications (Mohamed Dahidah & Vassilios Agelidis 2008). The SPWM scheme is illustrated in Figure 3.11.

![Figure 3.11 Sinusoidal pulse width modulation](image)

In this, \( V_c \) is the peak value of the triangular carrier wave and \( V_r \) is the reference, or modulating signal. For realizing SPWM, a high frequency triangular carrier wave is compared with a sinusoidal reference of the desired frequency. The intersection of sinusoidal reference and triangular waves determines the switching instants and commutation of the modulated pulse. Operating with constant frequency of carrier signal concentrates on voltage harmonics around switching frequency (which is of double the carrier
frequency) and multiples of switching frequency. Carrier based modulation for more than two level inverters require more carrier signals. For $N_L$-level inverter, minimum $(N_L - 1)$ carrier signals are needed.

Each carrier signal is responsible for a pair of switches. Every leg has two switches, one switch is controlled directly by the comparator signal and the other is controlled by its inverting signal. Multiple carrier signals in multilevel inverters create various possibilities of mutual locations of those signals. Typical combinations for multi-carrier systems are,

- Phase Shifted Carriers (PSC)
- Level Shifted Carriers (LSC)
  - Phase Disposition (PD)
  - Phase Opposite Disposition (POD)
  - Alternative Phase Opposite Disposition (A POD)

### 3.4.3.1 Phase shifted carriers

This method of carrier signals placement is usually used in H-bridge and FLC converters. It can also be applied in all kinds of multilevel inverters. As in other types of sinusoidal modulation, PSC modulation requires $(N_L - 1)$ carriers shifted in phase by $360°/ (N_L - 1)$, where $N_L$ is the number of levels. Each carrier is responsible for a pair of switches in all legs of the converter (Samir Kouro et al. 2008).

In three phase system, two other phase voltages by comparison with the carriers are generating four more rectangular sequences for the remaining switches. Figure 3.12 presents carrier placement for three level inverter and one of the commanded voltages.
3.4.3.2 Level shifted carriers

Second type of sinusoidal modulation is PWM with level shifted carriers. Difference between those methods is rather small and gathered around the output voltage spectrum. In PD-PWM modulation technique, the major feature of the phase voltage spectrum is the significant first carrier harmonic. This carrier harmonic is a common-mode component across the phase voltages of a three phase inverter, and therefore gets cancelled in the output line voltage. This feature gives the PD-PWM to produce excellent line voltage performance. Consequently, with concentration of harmonics in the first carrier, the harmonic sidebands which of course do not fully get cancelled between the three phase legs have less energy. In POD-PWM control technique, the carrier signals which are above the zero level are in phase and the carrier signals which are below the zero level are in phase of each other and out of phase by 180° to the above signals.
For APOD, all carriers are in phase opposition by 180° from their respective adjacent carriers. Variants of this type of modulation take the names from mutual locations of the carrier signals as it is shown in Figure 3.13.

### 3.5 SUMMARY

In this chapter, operation of half bridge and full bridge inverters with their advantages and disadvantages are discussed. Detailed analysis of various multilevel inverters such as diode clamped, flying capacitor and cascaded H-bridge with their concepts are presented. Modulation techniques such as space vector PWM, selective harmonic elimination and sinusoidal PWM are presented. Investigation on their applicability for the different topologies is also discussed.