3.1. Introduction

In this chapter the analysis of the current source Inverter fed Induction motor (CSIIM) and its various modes of operation is described. Also the control strategy for slip regulated induction motor speed control as described in chapter 2 is presented with the hardware details of the control elements. Finally, the comparison of various control strategies for four quadrant operation is also presented.

In figure 3.1 the basic circuit configuration of a 6 pulse, 120 degree conduction, current source Inverter fed Induction Motor is shown (without any feedback loops). As is well established, the d.c. link choke or filter along with the controlled rectifier supplies a regulated constant current $I_d$ to a 3 phase induction Motor and the inverter switches on the thyristors sequentially in response to the firing order as supplied by the external firing command required by the operating frequency of the drive.
3.2 **Current Source Inverter (Conventional)**

The schematic block diagram of the current source Inverter fed Induction motor is shown in figure 2.4. Principally it consists of a controlled rectifier, a d.c. link filter choke and a current fed inverter. The current source, constituted by the controlled rectifier and the filter choke supplies a regulated d.c. current $I_{dc}$ to the inverter. Circuit diagram of the conventional CSIFIM is shown in figure 3.1(b). The inverter thyristors $T_1$ to $T_6$ are switched at a rate determined by the stator frequency of the motor. The commutation capacitors $C_1$ to $C_6$ serve the purpose of commutation capacitors from the load. The inverter thyristors are fired sequentially so that each thyristor conducts for one third of the cycle (120 degree conduction).

3.3 **Commutation Process in the Conventional Current Source Inverter**

The following assumptions are made in analysing one commutation cycle of the conventional CSI (Current Source Inverter):

i) The commutation Capacitor charges to more than the peak line to line load voltage;
FIG. 3.1(a) Schematic block diagram of a current source inverter.

FIG. 3.1(b) Current source inverter with induction motor load: (the dashed line shows the path of \( I_{dc} \))
11) The inverter is working at steady state;

iii) The load voltage does not change during commutation, that is, the commutation time is much smaller than the period of the inverter frequency.

iv) Commutation capacitors are equal \( C_1 = C_2 = \ldots C_6 = C \). The inverter thyristors are fired in the following sequence:

\[ T_1 - T_2 - T_3 - T_4 - T_5 - T_6 - T_1 - T_2 \ldots \ldots \]

The commutation takes place six times per cycle and commutation of a conducting thyristor takes place when an adjacent thyristor is fired. For the purpose of analysis the commutation period is divided into two intervals, linear charging interval and oscillating or resonant charging interval.

a) Linear Charging Interval \( t_1 \)

Figure 3.1 shows the initial condition just prior to commutation of thyristor \( T_1 \). Current from the current source flows through \( T_1 \), diode \( D_1 \), motor phases \( \hat{\phi}_A \) and \( \hat{\phi}_C \), diode \( D_2 \) and thyristor \( T_2 \) then back to the source. The equivalent circuit applicable to the above condition is shown in figure 3.2(a) and the initial condition at time \( t = 0 \) is shown in figure 3.3. To commutate Thyristor \( T_1 \), thyristor \( T_3 \) is fired at time \( t = 0 \), conduction of thyristor \( T_3 \) connects the charged capacitor bank \( C' \) \( (C' = 3C/2) \) across thyristor \( T_1 \) which gets reverse biased the
FIG. 3.2 (a) and (b) Equivalent circuit of conventional CSI during commutation
charge across it raising it to a voltage \( V_{co} \) (the initial voltage across \( C' \)). The current transfer from \( T_1 \) to \( T_3 \) occurs instantaneously. The equivalent circuit at this new state is shown in figure 3.2(b). The d.c. current \( I_d \) flows from the current source through thyristor \( T_3 \), capacitor \( C' \) diode \( D_1 \), motor phases \( A \) and \( B \), diode \( D_2 \) and thyristor \( T_2 \) and then returning to the source. Neglecting the reverse recovery time of thyristor \( T_1 \), the commutation capacitor current i.e. \( i_c(t) \) and voltage \( V_c(t) = V_{31}(t) \) waveforms can be sketched as shown in figure 3.3. Since \( I_d \) is constant throughout the commutation interval, the capacitor bank (comprising capacitor \( C_1 \) in parallel with two series connected capacitors \( C_3 \) and \( C_5 \)) of equivalent capacitance \( C' = (3C/2) \) is charged linearly till \( D_3 \) becomes forward biased. The linear charging interval \( t_1 \) is given by:

\[
T_1 = C'(V_{co} + E_{BA} \sin \theta - I_d R)/I_d \quad \text{(3.1)}
\]

where:

\[
E_{BA} = \text{Peak value of the load line to line voltage (volts)}
\]

\[
C' = (3/2)C \text{ is the total capacitance of the upper bank (Farads)}
\]

\[
V_{co} = \text{Initial voltage across } C \text{ (volts)}
\]

\[
I_d = \text{Amplitude of the quasi square wave current (amperes)}
\]
\( \theta \) = Displacement angle \( \text{(refer to figure 3.4) (radians)} \)

\( R \) = Load resistance per phase (ohms)

The time interval \( \tau \) (indicated in figure 3.3) which is the time offered by the commutation circuit to the thyristor \( T_1 \) to turn off is the interval between the instant of firing of \( T_3 \) to the instant at which the capacitor voltage becomes zero. The expression for \( \tau \) is given by:

\[
\tau = \frac{V_{oc} C'}{I_d} \quad \ldots \ (3.2)
\]

(b) Resonant Charging Period \( t_2 \)

Referring to figure 3.1, when \( D_3 \) conducts the linear charging period \( t_1 \) ends and the resonant charging period \( t_2 \) begins. The equivalent circuit during the resonant charging interval is shown in figure 3.2(c). The same shows a closed loop formed through \( C' \), \( D_1 \), \( \phi A \), \( \phi B \) and \( D_3 \). The capacitor \( C' \) is charged sinusoidally at a frequency determined by \( C' \), the load inductance \( L \) and the resistance \( R \). During this period the capacitor current \( i_c(t) \) is given by Appendix 3A.
FIG. 3.2 (c) Interval $t_2$

FIG. 3.2 (d) contd.
\[ i_c(t) = [(R \cdot I_d / \omega_1 L) \sin \omega_1 t + I_d (\omega_0 / \omega_1) \sin (\omega_1 t + \phi_1)] e^{-\alpha_1 t} \]  

\ldots (3.3)

where:

\[ \alpha_1 = R / 2L \quad \omega_0^2 = 1 / 2LC', \]

\[ \omega_1 = \omega_c^2 - \alpha_1^2 \quad \text{and} \quad \phi_1 = \tan^{-1} \left( \frac{\omega_c}{\alpha_1} \right) \]

The capacitor voltage \( V_c(t) \) is given by:

\[ V_c(t) = E_{BA} \sin \theta + 1 / C' \int_0^t [i_c(t) dt] - I_d R \ldots (3.4) \]

The variation of \( i_{D1}(t) \) diode current in diode \( D_1 \) with \( V_c(t) \) as a function of time \( t \) is shown in figure 3.3. Since the current in the diode cannot reverse, the oscillation ends when the oscillatory current \( i_c(t) \) becomes zero. Therefore the resonant charging period \( t_2 \) can be calculated by equating the expression for \( i_c(t) \) in (3.3) to zero by putting \( t = t_2 \) in the same. Doing so one gets:

\[ \sin \omega_1 t_2 = \left( \frac{\omega_c}{\omega_1} \right) \sin \left( \omega_1 t_2 + \phi_1 \right) \]  

\ldots (3.5)

The peak capacitor voltage \( E_{pc} = V_c(t_2) \) is given by:

\[ V_c(t_2) = R I_d \left[ 1 + \left( \frac{\omega_c}{\omega_1} \right) e^{-\alpha_1 t_2} \sin \left( \omega_1 t_2 - \phi_1 \right) \right] 
+ \left( I_d / \omega_1 C' \right) e^{-\alpha_1 t_2} \sin \omega_1 t_2 + V_{co} \ldots (3.6) \]

Where:

\[ V_{co} = E_{BA} \sin \theta - I_d R \]
$V_{T_1}$ - voltage across thyristor $T_1$

$V_c$ - capacitor voltage

$V_c = V_{31}$

$i_{D_1}$ - current through diode $D_1$

$V_{D1}$ - voltage across diode $D_1$

$i_{D_3}$ - current through diode $D_3$

$V_{D3}$ - voltage across diode $D_3$

$V_{BA}^l = E_{BA} \sin \theta - I_d R$

**FIG. 3.3** Voltage and current variation in conventional CSI during commutation
From the end of the resonant charging interval $t_2$, current $I_d$ flows through $T_3$, $D_3$, $\varphi_3$, $J_c$, $D_2$ and $T_2$, till next commutation starts. Since we have assumed that the peak capacitor voltage is more than the peak line to line voltage, there is no possibility for the capacitor to be charged further. The total commutation time $t_c$ is given by:

$$t_c = t_1 + t_2 \quad \ldots \quad (3.7)$$

For $R = 0$

$$t_c = \left(\frac{E_{BA} \sin \beta + (I_d/w_0 C')}{I_d} + \frac{A/2w_0}{...} \right) \quad (3.8).$$

The last term of (3.8) is a constant, but the first term is a function of load voltage, load current and the displacement angle $\beta$. The $t_c$ increases with $E_{BA}$ and $\beta$ but, decreases with $I_d$. Hence the maximum value of $t_c$ occurs when $E_{BA}$ is maximum and $I_d$ is minimum, that is at maximum speed and light load condition. Yasuoka and Tsurehiro [37] have given in detail the problems concerned with the instability introduced by $t_c$ exceeding one sixth of the cycle. They have also discussed the dependency of $t_c$ on slip frequency of the induction motor.

3.4. Voltage Ratings of Conventional CSI Components

In the previous section it has been assumed that the commutation capacitor has been charged to more than supply
voltage and that no further charging occurs after the end of commutation. Iida [39] has analysed the circuit for $\theta = 0$ degree to 360 degree operation and has given the conditions for further charging of the capacitors. In this section a simplified analysis of the inverter in $\theta = 0$ degree to 180 degrees range, as shown in figure 3.4 is explained.

3.4.1. **Capacitor Voltage Variation**

There are six commutations per cycle of which three occur in the upper rail (row) and another three in the bottom rail. Since the capacitors and thyristors are arranged symmetrically, analysis over one third of a cycle would be sufficient to determine the voltage across the capacitors over a cycle range.

i) **Linear Charging period**

The initial condition of the capacitors just prior to commutation of thyristor $T_1$ is shown in figure 3.1. Let the initial voltage at $t = 0$ be:

$$V_{13}(0) = X$$
$$V_{35}(0) = Y$$
$$V_{15}(0) = Z$$

During the linear charging period $t_1$ (refer figures 3.2 and 3.3), the capacitor voltages are given by:
FIG. 3.4 Voltage waveforms (firing angle $\theta = 120^\circ$) at various points of conventional C S I
\[ V_{13}(t) = X - I_{dc} t/C', \]
\[ V_{35}(t) = (I_{dc} t/2C') + Y \]
\[ V_{51}(t) = (I_{dc} t/2C') - Z \] \hspace{1cm} \ldots \ (3.10)

At the end of the linear charging period, that is for \( t = t_1 \)

\[ V_{13}(t_1) = -E_{BA} \sin \theta \]
\[ V_{35}(t_1) = \text{(Voltage change in } C1)/(2) + Y \]

that is:

\[ V_{35}(t_1) = [(X + E_{BA} \sin \theta)/2] + Y \]
\[ V_{51}(t_1) = (X + E_{BA} \sin \theta)/2 - Z \] \hspace{1cm} \ldots \ (3.11)

ii) **Resonant Charging Period for** \( t > t_1 \)

\[ V_{13}(t) = -E_{BA} \sin \theta - \int_{t_1}^{t} \left( [i_c(t - t_1)/C'] d(t - t_1) \right) \]

where:

\[ i_c(t - t_1) = I_{dc} \cos \omega (t - t_1) \ldots \text{(load resistance } R \text{ is assumed to be negligible)} \]

\[ V_{35}(t) = Y + \left[ \frac{X + E_{BA} \sin \theta}{2} \right] + 1/2 \left\{ \left[ i_c(t - t_1)/C' \right] d(t-t_1) \right\} \]
\[ V_{51}(t) = -Z + \left[ \frac{X + E_{BA} \sin \theta}{2} \right] + 1/2 \left\{ \left[ i_c z(t - t_1)/C' \right] d(t-t_1) \right\} \] \hspace{1cm} \ldots \ (3.12)
For \( t = t_2 \), let the current \( i_c(t) \) become zero, and since the current cannot reverse the charging of the capacitors stop, that is from equation (3.3):

\[
i_c(t) = I_{dc} \cos \omega_c (t_2 - t) = 0 \quad \text{and} \quad t_2 = \left( \frac{X}{2\omega_c} \right) + t_1 \quad \text{...(3.13)}
\]

At the end of the resonant charging interval \( t_2 \),

\[
V_{13}(t_2) = -E_{BA} \sin \theta - I_{dc}/\omega_c C' \\
V_{35}(t_2) = Y + \left[ \frac{X + E_{BA} \sin \theta}{2} \right] + (I_{dc}/2\omega_c C') \\
V_{51}(t_2) = \left[ \frac{X + E_{BA} \sin \theta + (I_{dc}/\omega_c C')} {2} \right] - Z
\]

\[
\text{...(3.14)}
\]

Since there is no further charging until next commutation equation (3.14) gives the initial voltages of the capacitors for the next commutation cycle.

\[
V_{13}(0) = V_{35}(t_2) \quad \text{...(3.15a)} \\
- V_{13}(t_2) = V_{15}(0) \quad \text{...(3.15b)} \\
V_{35}(0) = -V_{15}(t_2) \quad \text{...(3.15c)}
\]
From the equations (3.14) and (3.15b) and recalling from subsection (i) of section (3.4) that $V_{15}(0) = Z$, one gets:

$$z = E_{BA} \sin \theta + \left( \frac{I_{dc}}{\omega C} \right)$$

From equations (3.15c) and (3.9) one finds:

$$z = E_{BA} \sin \theta + \left( \frac{I_{dc}}{\omega C} \right)$$

Similarly equations (3.15c), (3.14) and (3.9) yield:

$$Y = \frac{\left[ X + E_{BA} \sin \theta + \left( \frac{I_{dc}}{\omega C} \right) \right]}{2} - Z$$

From equations (3.15a), (3.14) and (3.9) one again gets:

$$X = Y + \frac{\left[ X + E_{BA} \sin \theta + \left( \frac{I_{dc}}{\omega C} \right) \right]}{2}$$

that is:

$$X = V_{co} = E_{BA} \sin \theta + \left( \frac{I_{dc}}{\omega C} \right)$$

$$Y = 0$$

$$Z = X = V_{co}$$

The same analysis holds good when R is not negligible from equation (3.6):

$$X = V_{co} = R I_{dc} \left[ 1 + \left( \frac{\omega}{\omega_1} \right) e^{-\frac{\omega_1 t_2}{\omega}} \sin(\omega t_1) \right] \sin(\omega t_2 - \phi_1)$$

$$+ \left( \frac{I_{dc}}{\omega C} \right) e^{-\frac{\omega_1 t_2}{\omega}} \sin(\omega t_2) + E_{BA} \sin \theta - I_{d} R$$
where \( t_2 \) is substituted from equation (3.5) namely:

\[
\sin w_1 t_2 = (w_0 L/R) \sin (w_1 t_2 + \phi) \quad \ldots \quad (3.17)
\]

The variation of capacitor voltage over one cycle has been plotted in figure 3.4.

3.4.2 Voltage across thyristor

The capacitor voltage appears across the non-conducting thyristors through the conducting thyristors. From figure 3.1 when thyristor \( T_1 \) is conducting the forward voltages of thyristor \( T_2 \) and \( T_3 \) are equal to the capacitor voltages \( V_{13} \) and \( V_{15} \) respectively. When \( T_3 \) is triggered \( T_1 \) is reverse biased by \( V_{13} \) and \( V_{35} \) appears across \( T_5 \). That is, the thyristor voltages is the same as the accompanying capacitor voltage. The voltage variation across thyristor \( T_1 \) has been plotted in figure 3.4.

3.4.3 Voltage across diode

The reverse voltage across a diode is the sum of the capacitor voltage and the line to line voltage. From figure 13.4 the line voltages are given by:

\[
\begin{align*}
V_{BA} &= \sqrt{3}E_m \sin(wt + 4\pi/3) \\
V_{CA} &= \sqrt{3}E_m \sin(wt + \pi) \\
V_{CB} &= \sqrt{3}E_m \sin(wt + 2\pi/3)
\end{align*}
\quad \ldots \quad (3.18)
\]

where \( E_m \) is the peak value of phase voltage.
From figure 3.1 when diode $D_1$ is conducting, the reverse voltage across $D_3$ and $D_5$ are given by:

$$V_{R, D_3} = V_{13} + V_{BA}$$

$$V_{R, D_5} = V_{15} + V_{CA}$$

From the above analysis:

$$V_{13} = V_{15} = \frac{I_d}{\omega C'} + \sqrt{3}E_m \sin \theta \ldots (3.20)$$

$$V_{R, D_3} = \left( \frac{I_d}{\omega C'} \right) + \sqrt{3}E_m \left[ \sin \theta + \sin(\omega t + \theta + 4\pi/3) \right]$$

$$V_{R, D_5} = \left( \frac{I_d}{\omega C'} \right) + \sqrt{3}E_m \left[ \sin \theta + \sin(\omega t + \theta + \pi) \right] \ldots (3.21)$$

Differentiating the equations (3.21) w.r. to $\omega t$ and equating to zero, the value of $\omega t$ at which the peak inverse voltage occurs can be obtained. For diodes $D_3$ and $D_5$ the peak inverse voltage occur at:

$$\omega t = (-150 - \theta) = (210 - \theta) \text{ for } \theta \geq 90^\circ$$

and

$$\omega t = (270 - \theta), \text{ for } \theta \geq 150^\circ \ldots (3.22)$$

For $\theta = 120^\circ$ degree, the variation of reverse voltage of diode $D_1$ has been plotted in figure 3.4.
3.4.4. Maximum and Minimum value of Capacitor Voltage

a) Maximum Value: From equation (3.16) the capacitor voltage $V_c$ is given by $V_c(\theta) = \frac{I_d}{\omega C'} + \sqrt{3}E_m \sin \theta$ ...

Then for constant value of $I_d$, the maximum value of capacitor voltage $E_{pc}$ occurs at displacement angle $\theta = 90$ degree and is given by:

$$E_{pc} = \left[ \frac{I_d}{\omega C'} \right] + 3E_m$$ ...

b) Minimum Value: In the previous section it has been assumed that at the end of commutation the capacitors charge to more than peak line voltage and no further charging occurs outside the commutation intervals, but strictly, further charging takes place when more than one diode conducts. When the thyristor $T_1$ and diode $D_1$ are conducting the reverse voltage across $D_3$ and $D_5$ are given by equation (3.21). For the diodes to conduct:

$$V_R, D_3 < 0 \text{ and } V_R, D_5 < 0$$ ...

that is, $V_{13} < -V_{BA}$ and $V_{15} < -V_{CA}$

that is, $V_{13} < -\sqrt{3} E_m \sin (wt + \theta + 4\pi/3)$ ...

and

$$V_{15} < -\sqrt{3} E_m \sin (wt + \theta + \pi)$$
For $\theta = 0^\circ$, charging occurs through diode $D_3$ at $wt = \frac{\pi}{6}$ to the peak value of $V_{AB}$ and at $wt = \frac{\pi}{2}$, diode $D_5$ conducts and the capacitors charge to the peak value of $V_{AC}$. Thus throughout the range of $\theta = 0$ degree to 90 degrees (inversion mode operation), the minimum capacitor voltage is the peak value of line voltage. For 90 degree $\leq \theta \leq 180$ degrees (rectifying mode operation), no further charging occurs.

From the above analysis it is seen that the peak capacitor voltage (equation 3.17) causes high voltage stress on the thyristors and on the diodes. To reduce the voltage stress, large value of capacitors may be used but, this slows down the current transfer and causes commutation overlapping. So the conventional CSI has been modified with auxiliary circuit to reduce the commutation period and the peak capacitor voltage.

3.5 Control strategy for slip regulated Induction Motor Speed Control

The method described for single phase sine wave current generation can be extended to polyphase current generation for speed control of Induction Motor.

Neglecting the magnetising current, for small values of slip, the output of the motor is given by:
FIG 3.5 block diagram for three phase sine wave current generator for induction motor speed control
\[ P_0 \approx \frac{2}{s} I_s r' / s \] ... (3.26)

Where:

- \( P_0 \) = output per phase (watts);
- \( I_s \) = stator current per phase (amps);
- \( s \) = per unit slip (dimensionless);
- \( r' \) = referred rotor resistance per phase (ohms).

The slip \( s \), which is proportional to the load, is sensed, and the stator current is adjusted to balance the power demand. In the present scheme, the magnitude of the reference signal is controlled by the rotor slip and its frequency is determined by the speed setting voltage.

The block diagram of the scheme is shown in figure 3.5. The power circuit consists of a diode bridge rectifier which feeds the fixed voltage d.c. link. The L.C. filter supplies a ripple-free d.c. voltage to a high frequency inverter. The control circuit consists of a reference sine wave signal generator, a differential amplifier, a hysteresis comparator and thyristor firing circuits.

The deviation of the actual speed from the reference speed is amplified and applied to the reference sine wave generator to control the magnitude of the reference signal. The reference signal and the actual load current are compared and the
difference is amplified and applied to the hysteresis comparator. When the difference exceeds the hysteresis level, the comparator changes the state and the inverter is switched to decrease the difference.

The current waveform and the performance of the scheme explained above depend on the inverter configuration. The three phase inverter can either be three single phase inverters or three half bridge inverters shown in figure 3.6. The possible current waveforms produced by the half bridge inverter is shown in figure 3.7. From figure 3.7, it is seen that when half bridge inverter circuits are used, the load voltage can be either $+E_1/2$ or $-E_1/2$. Therefore, at near zero value of the reference wave the rise and fall time of the load current is nearly equal. But, at the maximum value of the reference wave the current falls very fast. The single phase inverter circuit has the flexibility of producing either $+E_1$, $-E_1$, or zero voltage. Within one half cycle period, the load is connected to the supply to raise the current; and to decrease the current the load voltage is made zero. Therefore, the rise time of the load current is the same as in the previous case but fall time is longer. When the load time constant is large, the load current may not follow the falling side of the reference wave. In such cases, the load current deviation can be detected and the load
FIG. 3.6 Inverter configurations

FIG. 3.7 Half bridge inverter output waveforms
voltage can be reversed to make the current to follow the reference wave.

The method described for reference wave adapted current requires only simple control circuits. Since the load current is continuously monitored and controlled, the fault currents are detected fast and the inverter is switched to limit the current. The load current has better sine waveforms with superposed high frequency harmonics.

3.6. **Closed loop control strategy for Four Quadrant Operation**

The schematic block diagram of the closed loop control strategy for the four quadrant operation of a CSIFIMD system is shown in figure 3.8. In this system the speed error \( (w_r^* - w_r) \) sets the slip frequency \( w_{sl} \) and the slip determines the required state current. The control strategy consists of a precision analog tacho which gives a voltage signal \( w_r \) proportional to speed. The ABS and Amp 1 circuit gives the absolute value of the speed voltage. A multiturn potentiometer is used to set zero voltage for zero speed and a positive voltage for reference speed \( w_r^* \). The slip regulator SR (proportional controller) regulates the slip \( w_{sl} \) depending on the polarity and magnitude of the speed error \( (w_r^* - w_r) \).
**Fig. 3.8** closed loop control strategy for four quadrant operation of CSI/IM drive.
The ABS and Amp 3 circuit determines the stator current $I$ depending upon the magnitude of the slip speed $\omega_{s1}$. A current $I_0$ is set to excite the motor at zero slip. The error of the actual current $I$ and the set current $(I + I_0)$ is the input to the PI controller and its output controls the converter firing angle. The sum of $\omega_{s1}$ and $\omega_f$ determines the stator angular frequency $\omega_s$. The absolute value of $\omega_s$ determines the frequency of $V_{co}$ in the inverter control module. The logic signal at the output point $X$ of the phase sequence control circuit determines the inverter phase sequence.

3.6.1. **Converter Control Circuit**

The cosine control circuit for the converter firing angle control is shown in figure 3.9. It consists of six analog comparators, six monostables, a synchronising transformer and a filter cum phase shifting network. The phase shifting network filters all the voltage spikes (including those which are generated during the converter thyristor switching) in the synchronising signal. A square wave voltage pulse of sufficient magnitude may be added to the filtered synchronising signal at $0$ degree firing angle. This provision ensures firing pulses to the thyristors at all time irrespective of the magnitude of the a.c. main voltage fluctuations.
FIG. 3:9 cosine wave firing angle circuit from the converter
3.6.2 Inverter Control Circuit

The inverter control circuit designed for the twelve step current waveform inverter is given in figure 3.10. It consists of a \( V_{CS} \), a 24 stage (left shift/right shift) shift register, a diode decoder and a few logic gates. The phase sequence control input determines the direction of shift of the shift register and hence the inverter phase sequence.

3.6.3 Slip Regulator SR

The slip regulator SR which is a PI Controller is shown in figure 3.11(a). The input to the SR is the speed error \( (w_r - w_f) \) and its output is the slip \( w_{sl} \) which is limited to \( S_{\text{Max}} \). The antiparallel diodes \( D_1 \) provide a threshold to the speed error. For the speed error higher than this threshold, the regulator has a higher proportional gain. Thus the regulator acts fast for higher speed errors.

3.6.4 Current Controller

The converter current controller which consists of a summer and a PI controller is shown in figure 3.11(b). The summer subtracts the actual current \( I \) from the set current \( (I - I_0) \). The Zener diode \( Z_2 \) at the output point of the controller limits the converter firing angle variation to 0° to 150° degree range. The breakdown voltage of Zener diode \( Z_1 \) determines the maximum level of the converter current. When the current exceeds this level, the
FIG 3.10 inverter control circuit
FIG. 3.11(a)  slip regulator

speed error
($\omega_r^* - \omega_r$)

$R_1 \ll R_2 \ll R_3$

FIG. 3.11(b) current controller

$R_1 \gg R_2$

to conv.
firing circuit
controller capacitor is discharged instantaneously, accelerating the action of the controller for over currents.

3.6.5 Starting the CSI

Since initially there is no charge on the commutation capacitors, they have to be charged before switching the inverter thyristors. The capacitors can be charged either by auxiliary circuits or by controlling the converter and inverter in a particular mode. In this section the latter method which reduces the cost of the system is explained.

The mode of control of the system during starting is explained with reference to the timing diagram given in figures 3.12(a) and 3.12(b). For the period $\delta_1$, the converter is controlled to deliver the maximum d.c voltage. During this period only two thyristors, one in the top row and another in the bottom row of the inverter are kept in the 'ON' state. The equivalent circuit is given in figure 3.13. Since there is no back e.m.f in the motor at stand still, $E_d$ (back emf) is zero. Neglecting the resistance in the circuit the capacitor voltage $V_c(t)$ is given by:

$$V_c(t) = \frac{[2L/(2L + L_f)]E_d}{(1 - \cos \omega_e t)} (3.27)$$

Where

$L_f = \text{filter inductance}$

$\omega_e ^2 = \frac{(2L + L_f)}{(2L L_f C')}$. 
FIG. 3.12  a. variation of converter control voltage during starting

FIG. 3.12  b. variation of inverter control voltage during starting
FIG. 3.13 equivalent circuits for CSI/IM drive during starting
The current through the load is given by:

\[ i_2(t) = \left[ \frac{E_d}{\omega_e (2L + L_F)} \right] [\omega_e t - \sin \omega_e t] \quad \ldots (3.28) \]

At \( \omega_e t = \pi \), the capacitor charges to \( E_{pc} \) which is given by:

\[ E_{pc} = \left[ \frac{4L}{(L_F + 2L)} \right] E_d \quad \ldots (3.29) \]

\[ i_2(\pi/\omega_e) = \frac{E_d}{[\omega_e (2L + L_F)]} \quad \ldots (3.30) \]

Since the capacitor is isolated by the diode, it cannot discharge through the load. At the end of period \( \beta_1 (\beta_1 = \pi/\omega_e) \), the converter is controlled in the inversion mode and the load current decreases to zero. The equivalent circuit during this state is shown in figure 3.13(b) and the load current \( i(t) \) is given by:

\[ i(t) = \left[ \frac{E_d}{\omega_e (2L + L_F)} \right] e^{-(2R + R_F)/(2L + L_F)} \quad \ldots (3.31) \]

After delay \( \beta_2 \) the converter output is increased slowly so that the load current increases gradually. Simultaneously the inverter is controlled at the maximum frequency. Since the capacitors have been charged these can commutate the gradually rising load current. After two to three cycles of operations the capacitors build up sufficient voltage to commutate maximum load current. At the end of period \( \beta_3 \) the starting circuit leaves the system control to the speed feedback loop. The starting circuit to start the inverter in the manner described above is explained.
3.6.6 Starting Circuit For CSI

Since the CSI Commutation Capacitors are not charged before energising the inverter, they have to be charged before switching the inverter thyristors. The starting circuit is shown in figure 3.14 and controls the converter and inverter in a particular manner so that the commutation capacitors are charged fully before high load current is supplied. This circuit directs the controlled rectifier (CR) to the rectifier mode and then to the inverter mode for a specified time shown in figure 3.12(a). The inverter is not switched until the commutation capacitors are charged. The starting circuit consists of three monostables, a comparator, a ramp generator, a few logic gates and switches. The monostables determine the delays $\delta_1 \rightarrow \delta_3$ and the delays are accounted from the instant of transferring the switch $S_1$ from the stop position to the start position. When $S_1$ is in the stop position the switch $S_2$ is connected to the comparator output (point A). The comparator output drives the controlled rectifier to the inversion mode. $S_2$ remains connected to the comparator output till the end of the delay $\delta_2$. During the period $\delta_2$ the clock to the ring counter is inhibited and only two thyristors, one in the top row and another in the bottom row, are in the 'ON' state.

The comparator output is in positive maximum as shown in
$V_{f \text{max}}$ - analog voltage for max freq.

$V_f$ - freq. control voltage $a_3 > a_2 > a_1$

**Fig. 3.14** Starting circuit for CSI
figure 3.12(a) for a period $\delta_1$ ($\delta_1 < \delta_2$), which controls the CR to full conversion. The equivalent circuit for the power circuit and the load during this state is given in figure 3.13(a). The commutation capacitors get charged as already explained. After the delay $\delta_1$ the comparator output goes to the negative maximum which drives the CR to full inversion mode and the link current is reduced. Monostable 3 connects the switches $S_3$ to $V_{f_{\text{max}}}$ (which sets VCO at its maximum frequency) and $S_4$ to $C$ for a period $\delta_3$ ($\delta_3 > \delta_2$).

At the end of the period $\delta_2$ the clock is connected to the ring counter. Hence the inverter is switched at the maximum frequency while the control voltage to the CR is increased gradually so that the d.c link current also is increased gradually. Since the commutation capacitors are already charged to certain voltage, they can commutate the gradually rising link current. After a few cycles of commutation the capacitors are charged to sufficient level to commutate the maximum d.c link current. At the end of the delay $\delta_3$, the switch $S_3$ is connected to $V_f$ (speed setting voltage) and switch $S_4$ is connected to the current error amplifier. Then onwards starting circuit remains idle and feedback loops take care of the system.

3.7 The Phase Sequence Control Circuit

The phase sequence control circuit shown in figure 3.15 consists of two comparators and a few logic gates. The output at point X
FIG. 3.15 phase sequence reversing circuit
determines the phase sequence as shown in figure 3.8, of the inverter. A logic '1' sets forward sequence and a logic '0' sets reverse sequence. The output at point Y controls the speed command. A logic '0' disconnects the transistor switch $SW_1$ as shown in figure 3.8, from the speed reference line and connects it to ground to set negative slip. If a speed reversing command occurs, the phase sequence control circuit sets zero speed reference to slow down the motor. At a low speed $N_o$, as shown in figure 3.16, the phase sequence is reversed and the set speed reference is restored. In figure 3.15, the input RS to the non-inverting zero comparator (NIZC) is the tacho generator output which is positive for forward rotation and negative for reverse rotation. Let the positive voltage be defined as logic '1' and the negative voltage as logic '0'. The direction setting command has logic '1' for forward rotation and '0' for reverse rotation. When the direction of rotation of the motor and set direction are different, the logic level at Y should be '0'. The truth table for a logic '0' at Y is given in table 3.1.
The logic expression for '1' output at $Y$ is given by

$$Y = RS \overline{SS} + RS \overline{SS} \quad \ldots \quad (3.32)$$

For the fast speed reversal, the phase sequence is changed at rotor speed $N = w_{sl} = S_{max} N_S$. The absolute value of the tacho signal to the non-inverting comparator $NIC$ is designated as $SL$ and its logic value is defined as:

$$\begin{align*}
SL &= 1 \quad \text{for } N > S_{max} N_S \\
SL &= 0 \quad \text{for } N < S_{max} N_S
\end{align*} \quad \ldots \quad (3.33)$$

Where $N_S$ is the synchronous speed of the motor at supply frequency (a.c. mains).

The phase sequence is changed when $SL = 0$ and $RS \neq SS$. 

---

### TABLE 3.1

**TRUTH TABLE FOR $Y$**

<table>
<thead>
<tr>
<th>$SS$</th>
<th>$RS$</th>
<th>$Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
In other words, when the direction of rotation of the rotor and the set direction are not the same and the rotor speed is less than the maximum slip speed, the phase sequence is changed. From the truth table given in Table 3.2, the expression for a logic '1' at X is given as:

\[ X = SS \overline{SL} + RS \overline{SL} \quad \ldots \text{(3.34)} \]

**Table 3.2**

**Truth Table for X**

<table>
<thead>
<tr>
<th>SS</th>
<th>RS</th>
<th>SL</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Since the circuit described above does not contain any memory element, it is free from malfunctioning.
3.B FOUR QUADRANT OPERATION

When the induction motor operates in the small slip range, the power $P_o$ developed in the rotor is given by:

$$P_o = \frac{I'_r r'_r}{S} \text{ (watts)} \quad (3.35)$$

where:

$I'_r$ = referred rotor current/phase (amps),

$r'_r$ = referred rotor resistance/phase (ohms),

$S$ (per unit slip) = $120 \left( \frac{f_s}{PN_s} \right) - \left( \frac{N}{N_s} \right) \text{ [Dimensionless]} \quad (3.36)$

where: $f_s$ = stator frequency (Hz),

$P$ = number of poles.

$N_s$ = rated synchronous speed

and $N$ = rotor speed (r.p.m)

Since $S$ is a function of $f_s$, $S$ can be controlled by controlling $f_s$. When the second term in (3.36) becomes greater than the first term, the slip changes sign. Power is transferred from rotor to stator and to the supply. The four quadrant operation of the induction motor is shown in fig. 3.16. Transfer of the operating point between quadrants I and IV and between quadrants II and III is obtained by controlling the stator frequency. Transfer of the operating point between quadrants I(III) and II(IV) can be obtained only by changing the stator phase sequence.
Figure 3.16 CSI/IM drive operating point travelling path during speed change.
The principle of the four quadrant operation of the CSI/IM is explained with reference to the block diagram shown in figure 3.8. When the motor is running at speed \( N_1 \) in the forward direction and if a speed reversal command occurs, the phase sequence control circuit selects a zero speed command which causes negative slip and regeneration takes place. When the rotor speed approaches zero, the phase sequence is reversed and the speed command is restored. Now, slip becomes positive and maximum torque is developed in the rotor until it reaches the set speed.

The movement of the operating point during speed reversal can be explained better with reference to the slip speed relation diagram shown in figure 3.16. Suppose the rotor is at standstill and a speed \( N_1 \) is set in the forward direction, the speed error \( (N_1 - 0) \) drives the slip regulator to the positive maximum value \( (S_{\text{max}}) \) which corresponds to the maximum torque. If the time constant of the slip regulator is neglected, the operating point moves along OAB. At point B the speed error becomes zero but, the kinetic energy stored in the rotor drives it beyond speed \( N_1 \). The speed error becomes negative which reduces the slip. Hence the torque also decreases, finally, setting the operating point at P.

From the following explanation the response of the system
can be understood. In the control panel there are two sets of speed selection potentiometers and direction selection switch. When one set is connected to the system, the other set will be free. Desired speed and direction is set in the standley set and is connected to the system, while the other set is disconnected from the system.

Let a speed \( N_2 \) in the direction opposite to the present direction of rotation be set. The phase sequence control circuit senses the change in the selected direction and sets the speed reference to zero value. The speed error becomes negative and the slip regulator drives the slip to a negative maximum. A regenerative torque develops in the rotor and it slows down fast. The operating point moves along PDEF, as shown in figure 3.16. At point E the rotor speed \( N = N_0 = \left( N_s \right) S_{\text{max}} \) and the stator frequency is zero. At this instant the phase sequence control circuit changes the phase sequence of the inverter. Since the stator frequency is zero, the rotor slows down. The absolute value \((w_r - w_s)\) controls the stator frequency. Since rotation of the phase sequence is opposite to the direction of rotation of the rotor, the slip remains at \( S_{\text{max}} \). At point F the rotor comes to rest and then starts rotating in the opposite direction. The phase sequence control circuit, senses the change in the direction of rotation of the rotor and restores the set
speed command. (From the instant of selection of the direction, the stator current is maintained in the maximum value, till the set speed command is restored. Then the speed error determines the stator current). The slip, which was hitherto negative maximum changes to positive maximum instantaneously. The operating point moves along $FAOK$ and finally settles at point $Q$ which corresponds to speed $N_2$.

3.9 Mode of Braking during Reversing the CSI/IM Drive

Since the CSI/IM drive is commanded for zero speed or for change of direction of rotation the system goes from motoring to regeneration, to slow down the rotor. The equivalent circuit for the power circuit during regeneration is given in figure 3.17. For maximum braking torque the d.c. link current $I_d$ is maintained at the maximum value throughout the braking mode.

Let $E_d$ be the negative voltage offered by the line commutated inverter and $E_b$ the average value of the d.c voltage produced at the d.c terminals of the CSI. The d.c link current $I_{dc}$ is given by:

$$I_{dc} = \frac{(E_b - E_d)}{(R_F + 2R)} \quad \ldots (3.37)$$

Power delivered into the a.c mains is $E_d I_d$ and power dissipated in the circuit resistance is $I_{dc}^2 (R_F + 2R)$. Thus the drive offers both the regenerative and dynamic braking. For high value of
FIG. 3.17 CSI/IM drive equivalent circuit during regeneration
slip:

\[ E_b \approx 1.35 V_L \]  \hspace{1cm} (3.38)

Where, \( V_L \) = r.m.s load line voltage.

Within the operating range of slip the stator voltage is directly proportional to the rotor speed. That is, \( V_L = K_1 N \). Therefore, \( E_b = K_2 N \), where \( K_1 \) and \( K_2 \) are constants.

From equation (2.37) for \( E_d = 0 \),

\[ E_b = I_d (R_F + 2R) = K_2 N \]  \hspace{1cm} (3.39)

Therefore, for \( N < \frac{[I_d (R_F + 2R)]}{K_2} \), the drive experiences only dynamic braking. Frequent speed reversals may heat up the motor unless better cooling is provided.

****