Abstract

Arithmetic and Logic Unit (ALU) is a critical component of any CPU. In ALU, adders play a major role not only in addition but also in performing many other basic arithmetic operations like subtraction, multiplication, etc. Thus realizing an efficient adder is required for better performance of an ALU and therefore the processor. Research started in late 1950s on designing efficient adder algorithms and their hardware implementation. Many designs based on serial and parallel structures have been proposed to optimize different parameters from time to time.

The first contribution of this thesis is the development of an efficient adder architecture that addresses the problems for higher bit operand lengths like fan-out, wiring complexity, etc.

Another important element in an ALU after adder is a multiplier. In multipliers, for reducing partial products and computing final result, multi-operand adders and fast adders are required. A special structure known as counters/compressors are typically used for designing multi-operand adders. Counters are multi-input, multi-output combinational logic circuits, which determine the number of logic 1’s in their input vectors, and generate a binary coded output vector that corresponds to this number. Large parallel counters like (15, 4), (32, 5), etc. can be constructed using this small counter and similar approach can be adopted in the case of compressors. The second contribution of the thesis is development of efficient counters and compressors for better performance of multiplier.

Apart from adders and multipliers in arithmetic units, elements like, incrementer/decrementer (INC/DEC) also play a major role in an ALU and also in address generation unit. A loop algorithm, for example, often needs a increment/decrement. These operations can be realized using adders but with a cost in terms of power and area. Therefore, standalone designs or unified designs for INC/DEC are required for low power applications. The third contribution of this thesis is the design of a multi-functional INC/DEC/2's complement/Priority encoder circuit. A design for binary INC/DECs is presented that is efficient in terms of speed without compromising on power.
The need to have hardware support for decimal arithmetic is increasing in recent years because of the growth in decimal data processing in commercial, financial and internet-based applications. To facilitate binary computations on the same hardware, a reconfigurable approach needs to be adopted. The fourth contribution of this thesis is the design of a new architecture for efficient Binary Coded Decimal (BCD) addition/subtraction that can be configured to perform binary addition/subtraction also. The architecture has been designed keeping in view the signed magnitude format where the adder logic itself detects the larger operand and carries out corresponding operations.

Finally, novel versions of two widely used arithmetic blocks i.e., multiplier and floating point adder, are designed. Efficient and proven basic functional units described above are used to implement these blocks. Simulations of these blocks have been carried out and comparisons made with existing designs that clearly demonstrate the efficiency of proposed units. Finally, a segment of a core of a processor is designed with incorporating all the above elements resulting in an efficient architecture.