Chapter 1

INTRODUCTION AND LITERATURE SURVEY

1.1 INTRODUCTION

Today modern life is impossible and meaningless without electronics gadgets like Personal Computer, high definition digital TV, high speed internet and mobile. These electronics tools are realized only because of striking progress in Ultra-Large-Scale Integration (ULSI) technology. The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) shown in Figure-1.1 [Domaradzki, 2006]; is the basic and fundamental building block of the modern ULSI integrated circuits (ICs). It is used in logic devices either to store charge or to perform the function of switching.

![Figure 1.1: Schematic diagram of the MOSFET](image)

The switching action of MOSFET is achieved through the use of a gate capacitor, either positive or negative charge is induced in the channel region along the bottom plate of the gate capacitor. This channel charge either connects or isolates the drain and source nodes depending on the type of carrier contained beneath the gate regions. Also in case of MOS capacitor the amount of charge (Q) induced in the channel region is given by the product of the gate oxide capacitance per unit area (C_{OX}) and the voltage drop across the gate capacitor (V):

\[ Q = C_{ox} V \]

... 1.1

Here C_{OX} can be modeled as a parallel plate capacitor and its value is given by:
$C_{ox} = K_{ox} \varepsilon_0 / t_{ox}$ \ldots 1.2

Where $K_{ox}$ is the relative dielectric constant of the material (3.9) for silicon dioxide, $\varepsilon_0$ is the permittivity of free space, $t$ is the thickness of the capacitor oxide insulator. Naturally, this is clear that reducing $t_{ox}$ increases $C_{ox}$ and hence the amount of channel charge. Also the drive current $I_{D, Sat}$ for a MOSFET can be written as: [Lojek, 2007];

$$I_{D, Sat} = \frac{W}{L} \mu C_{inv} \frac{(V_G - V_{th})^2}{2}$$ \ldots 1.3

Where $W$ is the width of the transistor channel, $L$ is the channel length, $\mu$ is the channel carrier mobility, $C_{inv}$ is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state, $V_G$ is the voltage applied to the transistor gate, $V_D$ is the voltage applied to the transistor drain, $V_{th}$ is the threshold voltage. The gate oxide thickness required for good MOSFET control actually depends on the capacitance of the film.

$$C = \frac{k \varepsilon}{t} \ldots 1.4$$

Where, $k$ is the dielectric constant, $A$ is the area and $t$ is the thickness. Prior to the discussion of scaling about device there are few device parameters which need to be considered are channel length $L$ and width $W$. Which also known as metal gate length, determines the number of transistors that can be placed on Si wafer. This is the area between source and drain beneath the gate, where the inversion layer is formed after applying threshold voltage to the gate. Which turn on the MOSFET. Also the oxide layer with certain thickness, $t_{ox}$ separates the gate and the channel. Further few more parameters, which determine the characteristics of MOSFETs are as follows:

- Oxide capacitance, $C_{ox}$, is the capacitance per unit area between the gate metal and the bulk surface.
- Gate-source voltage, $V_{GS}$, is the voltage applied between gate and source to control the operation of the transistor.
- Drain-source voltage, $V_{DS}$, is the voltage applied between drain and source.
• Threshold voltage, \( V_p \), is the minimum voltage that will induce inversion layer to turn on the transistor.

• Drain-source current, \( I_{DS} \), is the current that flow between drain and source through the inversion channel conducted beneath the gate when transistor is turned on.

In addition to this the operation of the MOSFET also depends on several properties of the gate dielectric material, SiO\(_2\). The wide band gap (\( E_g \)) of SiO\(_2\) electrically isolates the charges in the gate and channel regions. Also, the interface between SiO\(_2\) and the underlying Si substrate is electrically of very high quality, allowing electric field lines originating at the gate electrode to penetrate into the channel region to accumulate or invert the surface charge.

Though all these parameters affected by downscaling [Nowak, 2002];, even then the faster, smaller and less expensive MOS devices are always in demand. The transistors manufactured today are 25 times faster than those builds four decades ago. In the past half century the downsizing/scaling of MOSFET results to smaller device in smaller area, consumption of less power, and decrease in cost per transistor per function cost of integrated circuit. Gordon Moore’s observed that the number of components per chip increases every year as shown below in Figure-1.2 [ITRS, 2003]; He also predicted that the downscaling rate could be expected to continue.

![Figure 1.2: MOS channel length scaling and predication made by ITRS 2003](image-url)
So, in order to achieve smaller dimensions scaling of the transistor is required. This progress has been made by continual downscaling of MOSFET to smaller physical dimensions. This does not limit to physical length only. In order to produce a smaller transistor it is not sufficient to just shrink the transistors physical length and width shown in Figure-1.3, other dimensions must be shrunk as well as shown in Table-1.1. Shrinking gate lengths $L_g$, require thinner sidewall spacers $X_s$, shallower junctions $X_j$, and thinner gate oxides $T_{ox}$.

**Figure 1.3: Schematic diagram of the MOSFET for physical scaling**

The constraint for technology to scale insists that the total power consumption per unit area should remain constant. Further scaling beyond certain point, may melts the device. So to keep the transistor properly functional, the shrinking of the device parameters and dimensions should follow some rules. Constant field scaling method affects the Voltage, current, gate capacitance, channel resistance, transconductance, inversion charge, delay, power per circuit and power density of the present technology.

So for a 250 nm gate length MOSFET scaled by $\alpha = 1.4$, the new gate length will be 180 nm, the operating voltage will drop from 1.8 to 1.3 volts and the circuit delay becomes 0.7 times of what it was at 250 nm. Also operating frequency increases as circuit delay decreases, the operating frequency becomes 1.43 times whatever it was at 250 nm. If we assume a 800MHz frequency at 250 nm, then in theory 180 nm processing should yield 1.1 GHz.
1.1.1 MINIATURIZATION RULES FOR CMOS TECHNOLOGY

Leakage current is the major issue in CMOS technology. Further these current increases exponentially as oxide thickness reduced linearly. Literature survey states that downscaling the gate length and gate oxide thickness decreased only a factor of $10^2$, then supply voltage decreased only by $10$, also the available chip area increased by $10$ and power consumption generation increased by $10^5$, which may not increase under ideal scaling.

The Semiconductor Industry Association (SIA) expects to achieve the 22 nm technology at the end of 2018. So several set of rules illustrates in table-1.1 have proposed for finding alternate to the consequences occurs during downscaling of device size known as scaling rules for CMOS technology.

Further reduction in gate oxide thickness along with the channel length results to short channel effects (SCE) [Nowak, 2002]; It also results to smaller $V_{TH}$ at shorter $L_g$, and Drain induced barrier lowering (DIBL), smaller $V_{TH}$ at higher drain voltage ($V_{DS}$). In ULSI industry gate length can be defined by $L_g$, which must be $\sim 5L$, where $L$ is the characteristic length as given in equation1.5:

$$L = 0.1(X_j T_x T_{dep}^2)$$ … 1.5

As per above equation, vertical dimensions $(T_x, X_j, T_{dep})$ must be scaled together with $L_g$ to suppress SCE in bulk MOSFETs. As mentioned in table-1.1, if the gate length of the device shrinked by $1/\alpha$, then operating voltage may be reduced by $1/\alpha$, and also the circuit delay is also reduced by $1/\alpha$. This results to degradation of the device characteristics and performance as well. So the forthcoming devices may be related with lower technology nodes [Wong, 2004]; as shown in Table-1.2.

The limit was defined by photolithography and roughly presents the minimum channel length (smallest poly–Si/metal gate length) for a given process technology. The device less than 10 nm gate length would be extremely sensitive to the device physical dimensions and variations in material composition.

Table-1.1 [Wong, 2004] summarizes the major scaling factors, exclusively describes the limitation for each parameter and also provides the solutions for reliable
scaling.

<table>
<thead>
<tr>
<th>Microelectronics parameters</th>
<th>Scaling Factor</th>
<th>Limiting factor</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage $V_{dd}$</td>
<td>$1/\alpha$</td>
<td>Thermal Voltage/ quantum confinement</td>
<td>Low operating temp.</td>
</tr>
<tr>
<td>Electric Field</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel Length $L$</td>
<td>$1/\alpha$</td>
<td>Lithography</td>
<td>Double Gate structure (DG FET)</td>
</tr>
<tr>
<td>Drain Current</td>
<td>$1/\alpha$</td>
<td>Punch through</td>
<td></td>
</tr>
<tr>
<td>Gate capacitance per unit area, $C_{ox} = \varepsilon_{ox}/D$</td>
<td>$\alpha$</td>
<td>Physical thickness Limit</td>
<td>Oxynitride /high-K Atomic layer deposition (ALD)</td>
</tr>
<tr>
<td>Gate area, $A_g = L \times W$</td>
<td>$1/\alpha^2$</td>
<td>Non Scalabilities</td>
<td></td>
</tr>
<tr>
<td>Gate capacitance $C_g = \varepsilon_A/d$</td>
<td>$1/\alpha$</td>
<td>Leakage current</td>
<td></td>
</tr>
<tr>
<td>Parasitic capacitance $C_x$</td>
<td>$1/\alpha$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Carrier density in channel, $Q_{on} = C_o V_{gs}$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel resistance $R_{on} = 1/WQ_{on}$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate propagation delay $T_{pd}$</td>
<td>$1/\alpha$</td>
<td>Non Scalable $V_{dd}$</td>
<td></td>
</tr>
<tr>
<td>Maximum operating frequency, $f_o$</td>
<td>$\alpha^2$</td>
<td>Parasitic capacitance, EMI, interconnect R &amp; C</td>
<td>Low K-insulator Copper wire</td>
</tr>
<tr>
<td>Saturation current, $I_{ds}$</td>
<td>$1/\alpha$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current density, $J$</td>
<td>$\alpha$</td>
<td>Gate leakage current Frequency of transistor Over heating</td>
<td>Smart system power management Physical thicker gate dielectric High - k-dielectric</td>
</tr>
<tr>
<td>Switching energy per gate $E_g = I C_g (V_{DD})^2 / 2$</td>
<td>$1/\alpha ^3$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation per gate, $P_g = P_{gs} + P_{gd}$ Both $P_{gs}$ and $P_{gd}$ are scaled by</td>
<td>$1/\alpha^4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power speed product, $P_T = P_g T_d$</td>
<td>$1/\alpha^4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor per chip</td>
<td>$\alpha^2$</td>
<td>Yielding, complexity in interconnection</td>
<td>Serial signal communication</td>
</tr>
</tbody>
</table>

As it is clear from the Table-1.2 the gate capacitance targets for the 45 nm and 35 nm technologies require dielectrics with physical Equivalent oxide thickness (EOT) values of 1 nm and 0.8 nm, respectively. EOT is given by:
\[ EOT = \frac{k_{SiO_2}}{k_x} t_x \]

Where, \( k_x \) is the \( k \) value for the film of interest \( t_x \) is the physical thickness of the film of interest and \( k_{SiO_2} \) is the \( k \) value of silicon dioxide. In table-1.2 [Moore, 1997; Nowak, 2002; Wong, 2004; Doris, 2009, some other material]; expected growth technology node and the smallest poly-si/metal gate length are given with their starting years.

**Table-1.2: Gate Dielectric Layer Technology Requirements**

<table>
<thead>
<tr>
<th>Technology Node (nm)</th>
<th>Starting year</th>
<th>ITRS updates</th>
<th>( T_{inv} ) (nm)</th>
<th>EOT(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Year</td>
<td>Half pitch (nm)</td>
<td>Physical length(nm)</td>
</tr>
<tr>
<td>45</td>
<td>2007</td>
<td>2007</td>
<td>68</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2008</td>
<td>59</td>
<td>29</td>
</tr>
<tr>
<td>35</td>
<td>2009</td>
<td>2009</td>
<td>52</td>
<td>27</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2010</td>
<td>45</td>
<td>24</td>
</tr>
<tr>
<td>22</td>
<td>2011</td>
<td>2011</td>
<td>40</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2012</td>
<td>36</td>
<td>20</td>
</tr>
<tr>
<td>16</td>
<td>2013</td>
<td>2013</td>
<td>32</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2014</td>
<td>29</td>
<td>16</td>
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</tr>
</tbody>
</table>

Presently si-based devices with traditional oxide layer have been approaching to its fundamental scaling limit. Silicon dioxide (SiO\(_2\)) with 2nm only is representing 6 to 7 atomic layers oxygen [Bera, 2006];. But with 3-5 layers, SiO\(_2\) unable to behave like good insulator. So it is difficult to design low voltage devices with such parameters. Similarly leakage current density of 100A/cm\(^2\) at 1.5 V for 1.5 nm oxide thickness is undesirable for low power application.

So the significant consequence of aggressively scaling the gate oxide is the direct tunneling of carriers through the potential barrier presented by the insulator layer. From the study it is clear that when the thickness of the potential barrier becomes less than approximately 3 nm, substantial tunneling currents can flow through the conventional gate oxide (SiO\(_2\)), leading to large leakage current. In addition, the gate and channel regions are no longer isolated from each other. This also determines the fundamental limit to scaling of SiO\(_2\). Electron Energy Loss Spectroscopy (EELS) experiment demonstrated that the SiO\(_2\) thickness must have
two or three layers to show a full gap of 8.9 eV as shown in Figure-1.4.

![Figure 1.4: Bonding structure of SiO\(_2\) indicating the minimum thickness of the bulk oxide is about 7 Å [Iwai, 2006];](image)

This dielectric material greatly affects the operation of the MOSFET. Also, the interface between gate material and the underlying Si substrate is electrically of very high quality, allowing electric field lines originating at the gate electrode to penetrate into the channel region to accumulate the surface charge. So briefly it is clear that electric field strength in the device increases tremendously during downscaling and conventional dielectric may puncture.

Because of the immense costs associated with developing a replacement material for SiO\(_2\), several other reliability problems must be analyzed in advance. In practice, the extreme gate thickness length aspect ratio that would result from a very high-K value and hence a very thick insulator leads to fringing field effects which undermine the gate electrode’s ability to maintain control of the channel.

The industry requires a material which may fulfil the requirements for the upcoming technology nodes. So the introduction of high-k material can help solving most of the problems by using physically thicker high-k gate dielectric films. Hence there is a pressing need of high-k dielectric in order to meet the futuristic circuit requirements.
1.1.2 ROLE OF HIGH-K IN CMOS MINIATURIZATION

The material having dielectric constant greater than SiO$_2$ may be considered as high-k dielectric may be used in semiconductor manufacturing process. The implementation of high-k gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law [Bera, 2006]. To keep the trend downscaling of transistor, there is need to decrease the thickness of SiO$_2$ gate dielectric. But decrease in SiO$_2$ thickness increases the capacitance and degrade the device performance.

As the thickness scales below 2-3 nm, leakage currents due to tunneling increase drastically, leading to unwieldy power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-k material [cho, 2002; Chau, 2004] allows increased gate capacitance as shown in Figure 1.5:

![Comparison of conventional gate oxide with high-k material](image)

**Figure 1.5:** Comparison of conventional gate oxide with high-k material

Also the Conventional silicon dioxide gate dielectric structure compared to a potential high-k dielectric structure. A particularly important consideration is that the chosen high-k dielectric can be scalable to future technology generations.

So keeping in view the importance of leakage current thorough dielectric material a novel dielectric material is required [Cho, 2002]. So it is necessary to
investigate alternate material for the fabrication of futuristic CMOS devices. No doubt that Si MOSFET with high-k may be the promising candidates for next generation devices, because of its higher permittivity than conventional SiO$_2$. A detailed literature survey has been carried out for the selection of material.

### 1.1.3 NOVEL CONCEPT FOR ADVANCED GATE MATERIAL

In order to continue the scaling as per predication made by Moore an alternative material is required instead of conventional dielectric material. So now a day’s effort has been focused on the research and development of alternative high-K material. Replacement of SiO$_2$ is, however, not so simple as it may seem. As material will be used in extremely fine structures, so the requirements for new high-k materials are very stringent. The key guidelines for selecting an alternative gate dielectric are

- (a) permittivity, band gap, and band alignment to silicon,
- (b) thermodynamic stability,
- (c) film morphology,
- (d) interface quality,
- (e) process compatibility, and
- (g) reliability.

Many dielectrics appear favourable in some of these areas, but very few materials are promising with respect to all of these guidelines. Including these the bulk and interface properties of the new dielectric material must be comparable to the remarkable properties of SiO$_2$. There are wide variety of films with higher $k$ values, ranging from Si$_3$N$_4$ with a $k$ value of 7, up to Pb-La-Ti (PLT) with a $k$ value of 1,400 [Kingon; 2001].

Typically high-$k$ materials [Cho, 2002; Chui 2002]; under investigation are Al$_2$O$_3$, ZrO$_2$, HfO$_2$, Ta$_2$O$_5$, TiO$_2$, Er$_2$O$_3$, La$_2$O$_3$, Pr$_2$O$_3$, Gd$_2$O$_3$, Y$_2$O$_3$, CeO$_2$ etc. and some of their silicates such as Zr$_x$Si$_{1-x}$O$_y$, Hf$_x$Si$_{1-x}$O$_y$, Al$_x$Zr$_{1-x}$O$_2$ etc. But all of these materials are not stable thermodynamically on Si, also few other properties which need to care about are high breakdown voltage, low defect density, good adhesion, thermal stability, low deposition temperature, ability to be patterned easily and low charge states on silicon.

To find good substitutes for SiO$_2$, the high-$k$ materials must have several advanced features in addition to the high-$k$ value [Iwai, 2006]:

- They should be chemically stable with Si substrate and the gate electrode
- they should be thermally stable at temperatures no less than 500°C.
- they should have good interface properties with the Si substrate
• the structure can have low interface trap density,
• high channel mobility,
• low oxide trap density,
• large band gap, and large band off-set energies
• Low leakage current density (<1 A/cm² @ \( V_{GS} = V_{DD} \))
• Equivalent oxide thickness (E_{OT}) – 10 to 15Å
• High dielectric constant (10 < high-k < 50)

As high-k film can be physical thicker than pure SiO₂ layer by the ratio of its dielectric constant to that of SiO₂ with same gate capacitance as shown in Figure-1.6 and Equation1.7. Relationship between physical [Iwai, 2006]; thickness of SiO₂ and high-k gate oxide obtained by same gate capacitance value (\( C \)) is written as:

\[
C = \frac{\varepsilon_{\text{high-k}}}{t_{\text{high-k}}} = \frac{\varepsilon_{\text{SiO}_2}}{EOT} \quad \ldots 1.7
\]

where \( \varepsilon_{\text{high-k}} \) is the dielectric constant of high-k materials, \( t_{\text{high-k}} \) is the physical thickness of high-k gate oxide, \( \varepsilon_{\text{SiO}_2} \) is the dielectric constant of SiO₂ (= 3.9 equivalent oxide thickness) of pure SiO₂ layer which provide the same gate capacitance as high-k layers as shown in Figure-1.6. It is also clear that high-k dielectric constant 39 as shown below opens scope for further scaling on CMOS device, which were limited in case of conventional SiO₂:

\[
T_{EOT} = \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{high-k}}} \cdot T_{\text{phy}} \quad \ldots 1.8
\]

where \( T_{\text{phy}} \) is the physical thickness of gate oxide.

Next section explain the complex issues for the use of high-K material for gate dielectric applications and also to provide an update review on HfO₂, ZrO₂, TiO₂, Gd₂O₃ and some another high-K dielectric material shown in Table-1.3 and 1.5. Since an important function of the gate dielectric is to isolate the gate terminal from the current carrying channel region, it needs to be a good insulator.
Figure 1.6: Diagram of EOT for high-k and conventional dielectric material

A small energy band gap causes a small barrier height for the tunneling process in the MOSFETs. Therefore, before the selection of particular high-k insulator for semiconductor chip it is very important to know the band offsets between it and the semiconductor substrate.

For high-k dielectric band offset value should be greater than 10, whereas 25-30 is preferable [Choudhary, 2010]. However there is tradeoff between high-k value and band offset. It should be noticed that offset energy difference between oxide and silicon valance bonds \( \Delta E_v \), has same importance as \( \Delta E_c \) for the functioning of oxide in CMOS application. The value of \( \Delta E_v \) can be obtained by knowing the value of \( \Delta E_c \) from the equation

\[
E_{g_0} - (\Delta E_c + E_{g_{Si}})
\]

...1.9

where \( E_{g_0} \) and \( E_{g_{Si}} \) are the band gap values of the oxide and silicon respectively.

It has been observed that most high-K materials have smaller band gaps relative to SiO\(_2\) as shown in Figure-1.7.
Figure 1.7: Comparison of band gap and band offsets [Iwai, 2006; Choudhary, 2010]

Table-1.3 [Cho, 2002; Chai, 2004; Iwai, 2006; Choudhary, 2010]; illustrates the approximately inverse relation between band gap and dielectric constant for high-K dielectrics. This behavior is due to stronger polarizability implies weaker bonding, and weaker bonding implies a smaller separation between bonding and antibonding energies.

In addition to band gap and dielectric constant, the vibrational frequency of oxygen atoms is also main factor for the selection of high-k material to achieve the targeted dielectric constant. The lower vibrational frequency with oxygen bond is main concern in microelectronics applications. The tradeoff between dielectric constant and band gap limits the applicability of high-k materials in CMOS technology. The lower range of acceptable dielectric constants depends on the EOT requirements of a given technology node.
Table-1.3: List of Rapidly Expanding material in CMOS Technology

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant (K)</th>
<th>Band gap (Eg) (eV)</th>
<th>Conduction Band Offset $\Delta E_{c}$ (eV)</th>
<th>Valence Band Offset $\Delta E_{v}$ (eV)</th>
<th>Stability with Si</th>
<th>Crystal Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon dioxide (SiO$_2$)</td>
<td>3.9</td>
<td>8.9</td>
<td>3.5</td>
<td>4.4</td>
<td>yes</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Silicon nitride (Si$_3$N$_4$)</td>
<td>7.0</td>
<td>5.1</td>
<td>2.4</td>
<td>1.8</td>
<td>Yes</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Aluminum oxide (Al$_2$O$_3$)</td>
<td>9.0</td>
<td>8.7</td>
<td>2.8</td>
<td>4.9</td>
<td>Yes</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Gadolinium oxide Gd$_2$O$_3$</td>
<td>12</td>
<td>5.4</td>
<td>3.2</td>
<td>3.9</td>
<td>Yes</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Yttrium oxide (Y$_2$O$_3$)</td>
<td>15</td>
<td>5.6</td>
<td>2.3</td>
<td>2.6</td>
<td>Yes</td>
<td>cubic</td>
</tr>
<tr>
<td>Zirconia (ZrO$_2$)</td>
<td>25</td>
<td>7.8</td>
<td>1.4</td>
<td>3.3</td>
<td>Yes</td>
<td>Monoclinic, cubic, tetragonal</td>
</tr>
<tr>
<td>Tantalum pentoxide (Ta$_2$O$_5$)</td>
<td>26</td>
<td>4.4</td>
<td>0.3</td>
<td>3.1</td>
<td>No</td>
<td>orthorombic</td>
</tr>
<tr>
<td>Hafnia (HfO$_2$)</td>
<td>25</td>
<td>5.7</td>
<td>1.5</td>
<td>3.4</td>
<td>Yes</td>
<td>Monoclinic, cubic, tetragonal</td>
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<tr>
<td>Lanthanum (La$_2$O$_3$)</td>
<td>30</td>
<td>6</td>
<td>2.3</td>
<td>0.9</td>
<td>Yes</td>
<td>Hexagonal, cubic</td>
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<td>Titanium oxide (TiO$_2$)</td>
<td>80</td>
<td>3.5</td>
<td>1.2</td>
<td>1.2</td>
<td>Yes</td>
<td>Tetragonal</td>
</tr>
<tr>
<td>Strontium titanate (SrTiO$_3$)</td>
<td>300</td>
<td>?</td>
<td>?</td>
<td>?</td>
<td>yes</td>
<td>cubic</td>
</tr>
</tbody>
</table>

\[ EOT = T_{ox} + (K_{SiO_2} \cdot t_{high-k}) / (K_{high-k}) \]

where $T_{ox}$ and $K_{high-k}$ are the dielectric constant for the silicon oxide and high-K material $t_{high-k}$ is the physical thickness of high-K dielectric film.

From table-1.2 and table-1.4, it is clear that EOT values define the technology node for future generation devices. So it is believed that nitride SiO$_2$ with dielectric constants close to 4 will provide physical EOTs about to 1.6 nm and the Si$_3$N$_4$ (oxynitride) stacks with nitride with K values near 7 will provide physical EOTs up to 1.1 nm. While the pure metal oxides with dielectric constants in the range of 15 to 25 will provide physical EOTs down to about 0.6 nm. This providing a factor of four to six improvements over SiO$_2$. Equivalent oxide thickness of pure SiO$_2$ layer which provide the same gate capacitance as high-k layers.
So by considering the minimum EOT for pure nitride $K = 7.8$ can be thin as 0.35 nm which is thin enough for 18 nm technology node, also for mean $K$ oxinitride (5.8) then minimum thickness will be 0.47 which fulfill the need of 25 nm technology node requirement.

Table-1.3 to 1.5 summarizes the major characteristics, advantages, and disadvantages of oxides from those elements which were considered as potential high-k materials for MOS gate dielectric applications.

Process and device architecture technology nodes and the scaling of device dimensions with the predicted years of production are shown in Table-1.4 [Choudhary, 2010; some other sources]: In order to be able to shrink conventional MOSFETs beyond the 65-nm-technology node, innovations to new material may require in order following fundamental physical limits.

**Table-1.4:** Technology nodes, gate lengths and gate dielectrics for CMOS applications

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology node (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Physical gate length</td>
<td>37</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>EOT (nm) (physical)</td>
<td>1.0-1.2</td>
<td>0.8-0.9</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>EOT (nm) (electrical)</td>
<td>1.7-2.0</td>
<td>1.2-1.3</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
</tr>
</tbody>
</table>

Currently interest seems to be centered on films such as HfO$_2$, ZrO$_2$, and TiO$_2$ with k values of 30-40, 25 and 40-120 respectively. The leakage current of ZrO$_2$ and HfO$_2$ found to be 4-5 orders of magnitude lower than SiO$_2$ of equivalent gate oxide thickness. HfO$_2$ films behave reported quite similar to ZrO$_2$ because of similar fabrication chemistry and material properties.

Intel recently reported over five orders of magnitude reduction of leakage for high-k oxides based on HfO$_2$ and ZrO$_2$ versus SiO$_2$ for equivalent oxide thicknesses. In table 1.5 [Buchanan, 2000; Cho, 2002; Perkins, 2002; Dalapati, 2003; Gusev, 2003; Chai, 2004; Iwai, 2006; Bera, 2006; Choudhary, 2010]; comparison has been made on the recently used high-k materials i.e SiO$_2$, HfO$_2$, ZrO$_2$, TiO$_2$ and Gd$_2$O$_3$ in terms of structural, physical, optical and electrical characteristics.
### Table-1.5: Comparison between various parameters of High-k Dielectric materials

<table>
<thead>
<tr>
<th>Properties</th>
<th>SiO₂</th>
<th>HfO₂</th>
<th>ZrO₂</th>
<th>TiO₂</th>
<th>Gd₂O₃</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>Amorphous</td>
<td>Non-crystalline</td>
<td>Nanocrystal</td>
<td>Amorphous, Rutile</td>
<td>Amorphous</td>
</tr>
<tr>
<td><strong>Dielectric Constant</strong></td>
<td>3.9</td>
<td>20-25</td>
<td>22-26</td>
<td>22-40</td>
<td>23</td>
</tr>
<tr>
<td><strong>Band gap (eV)</strong></td>
<td>8.9</td>
<td>5.6</td>
<td>4.7-5.7</td>
<td>3.2</td>
<td>5.4</td>
</tr>
<tr>
<td><strong>Formation Temp.(°C)</strong></td>
<td>&gt;700</td>
<td>350</td>
<td>350</td>
<td>400</td>
<td>550</td>
</tr>
<tr>
<td><strong>Silicide formation</strong></td>
<td>NA</td>
<td>Yes</td>
<td>Yes</td>
<td>NA</td>
<td>No</td>
</tr>
<tr>
<td><strong>Thermal Stability</strong></td>
<td>1000</td>
<td>950</td>
<td>900</td>
<td>550</td>
<td>1200</td>
</tr>
<tr>
<td><strong>Interface trap density</strong></td>
<td>10¹⁰</td>
<td>10¹²</td>
<td>10¹²</td>
<td>10¹²</td>
<td>10¹⁰</td>
</tr>
<tr>
<td><strong>Oxide trap density</strong></td>
<td>10¹¹</td>
<td>10¹²</td>
<td>10¹²</td>
<td>10¹²</td>
<td>10¹¹</td>
</tr>
<tr>
<td><strong>Breakdown field</strong></td>
<td>10</td>
<td>&lt;4</td>
<td>&lt;4</td>
<td>&lt;4</td>
<td>3.5</td>
</tr>
<tr>
<td><strong>Capacitance (Cₓ₀)</strong></td>
<td>4.67×10⁻⁹</td>
<td>6.49×10⁻⁹</td>
<td>6.79×10⁻⁷</td>
<td>8.85×10⁻⁷</td>
<td>4.67×10⁻⁹</td>
</tr>
<tr>
<td><strong>Flat band voltage (Vₓ₀)</strong></td>
<td>4.15</td>
<td>0.85</td>
<td>.35</td>
<td>.25</td>
<td>.23</td>
</tr>
<tr>
<td><strong>Threshold Voltage (V₁)</strong></td>
<td>4.9</td>
<td>1.48</td>
<td>0.25</td>
<td>.86</td>
<td>.85</td>
</tr>
<tr>
<td><strong>Bulk Potential(Ǿ₁)</strong></td>
<td>.30</td>
<td>.30</td>
<td>.88</td>
<td>.30</td>
<td>.30</td>
</tr>
<tr>
<td><strong>EOT nm</strong></td>
<td>1100</td>
<td>35.45</td>
<td>33.99</td>
<td>31.15</td>
<td>33.74</td>
</tr>
<tr>
<td><strong>Low Leakage current density wrt SiO₂ (A/Cm²)</strong></td>
<td>10⁻⁴-10⁻⁵</td>
<td>10⁻⁴-10⁻⁵</td>
<td>10⁻¹-10⁻²</td>
<td>10⁻²-10⁻³</td>
<td></td>
</tr>
</tbody>
</table>

In Table-1.5, there is a comparison between main properties of hafnium, Zirconium, Titanium, Silicon Oxide and Gadolinium Oxide. The EOT has been calculated for 30 nm oxide films thickness. Electrical characteristics also been investigated by considering \( T = 300K \), standard physical constant \( (q, K, \varepsilon_0) \), and electrode area of about \( 1\times10^{-2} \text{ cm}^2 \).
In this study main emphasis is given on TiO$_2$, which exists in amorphous form and crystallizes in three distinct crystallographic structures as shown in Figure-1.8: two tetragonal phases, Anatase \( a = b = 3.785\text{Å}, \ c = 9.514\text{Å} \) and Rutile \( a = b = 4.587\text{Å}, \ c = 2.953\text{Å} \) and a third orthorhombic phase, Brookite \( a = 5.456\text{Å}, \ b = 9.182\text{Å}, \ c = 5.143 \text{Å} \). T Ohsaka et al [1978]; obtained the TiO$_2$ layers of anatase phase, well-adhered, homogenous, with good secularity and colored by interference of reflected light. The films thickness was in the range of 100 ± 500 nm.

In 1978 Pascual et al reported that TiO$_2$ films have successfully been used for photodecomposition of water and for environmental purification. He also suggested that these films were also successfully been used as gas sensor and antireflection coating, as ultraviolet (UV) light emitting devices, sensors, laser diodes and other high speed electronic devices.

![Figure 1.8: Unit lattice crystalline structure](image_url)

Therefore, TiO$_2$ has low energy band offset with respect to Si. As TiO$_2$ thin films could be applied in gate oxide in MOSFETs.

### 1.2 LITERATURE REVIEW

Scaling of conventional silicon based metal-oxide-semiconductor (MOS) transistors requires thinner and thinner SiO$_2$ films. However, the increase of leakage current through thinner SiO$_2$ films puts a fundamental limit on the existing MOS technology.
High dielectric constant (high-k) materials are natural substitutes for SiO$_2$ as insulators because they can maintain sufficient thickness to achieve desired capacitance. So keeping in view the importance of scaling, miniaturization and role of high-k following literature has been surveyed:

**Table 1.6: Literature Survey**

<table>
<thead>
<tr>
<th>Material</th>
<th>Literature Survey</th>
</tr>
</thead>
</table>
1.2.1 **SURVEY ABOUT SiO\(_2\)**

Dennard in 1974 suggested that by scaling device density can be increased at reduced cost. But Kooi et al [1976]; had focused on “Kooi pinch” effect because of thinned gate dielectric material. A significant solution came about from the lightly-doped-drain (LDD) device structure [Ogura et al 1980].

In early 1980s, half micron or quarter micron was considered as the limit because of the increased source/drain resistance, direct-tunneling through the thin gate oxide in the short channels. Those limits were mainly related to the technological issues and were overcome very soon. While in 1990, 100 nm was thought to be limit because of some physical parameter and increase of fundamental atomistic vibrations.

Liu et al [1993]; observed that the oxide thickness reached the atomic level further scaling was impossible in nanometer range. Particularly, it was found that the oxide thinner than the direct tunneling distances 3 nm can be used in MOS devices [Momose et al; 1994]. Also supply voltage of 1.1V and oxide thickness of 0.9 nm devices did not perform reliably because of large oxide field with further decrease in supply voltage. This happens because part of the applied voltage, dropped in inversion layer of the channel. Theoretical studies by Tang et al [1998]; showed that the band offset at the interface degraded substantially when the SiO\(_2\) layer was scaled to less than three monolayers. The large reduction in the band offset was attributed to a reduction in the SiO\(_2\) band gap and also suggested 0.7 nm as the scaling limit of SiO\(_2\).

Thompson and Rodder et al [1998]; suggested that conventional gate dielectrics would not meet the requirement and the introduction of novel gate dielectrics will be required in the near future. Muller [1999]; reported that SiO\(_2\), was used in CMOS integrated circuits and had many prominent advantages, including a low interface state density of the order of D\(_{it}\)~ low 10\(^{10}\) cm\(^{-2}\)eV\(^{-1}\), a good thermal stability in contact with silicon (Si), a large energy band gap and the large energy band offsets in reference to Si. Also Miller demonstrated that 3 nm is fundamental limit [Muller et al; 1999]. Using the scanning transmission electron microscope (STEM) probes and through detailed Electron Loss Spectroscopy (EELS) measurements they studied that device structure and chemical composition of the oxide layer as thin as 0.7-1.2 nm.
Schulz et al [1999] found that to ensure bulk like structure minimum three or four monolayer of SiO$_2$ were needed. A study by Kaneta et al [1999] proposed a mode, which directly computed the local energy gap at the interface of Si/ SiO$_2$. While the transition from bulk Si to bulk SiO$_2$ in their model was structurally abrupt, it was found that the full band gap of SiO$_2$ was not obtained until the second monolayer of SiO$_2$ was reached. Again, these calculations suggest that approximately 0.7 nm of SiO$_2$ is the minimum requirement for substantial band offsets to develop at the interface, indicating the formation of a large band gap.

The 10 nm was the latest limit being proposed for the major reason of the direct tunneling between source and drain. This restriction was again conquered by an experimental 6nm gate length MOS transistor, which is functional [Iwai; 2002]. It was found in the 10 nm device that the device performance is degraded and that the power consumption increases [Doris; 2002]. Device simulations have explored the impact of large $K$ values on threshold voltage roll-off and sub-threshold swing to determine the upper range of desirable dielectric constants, which generally is believed to be on the order of 30 to 50 [Lucovsky; 2002]. However, the downscaling of the MOS device must have an end. At least, it is not possible to make the MOS structure with a couple of atoms.

According to Chau et al. [2003, 2004]; found that when oxide was in nanometer range, even small non-uniformity either in chemical composition or even at surface fluctuation alter the device characteristics drastically. Iwai et al [2006]; observed that 25 percent reduction in oxide thickness i.e from 2nm to 1.5 nm, produced twice order of leakage current. So instead of continuing to scaling of SiO$_2$, recent effort had focused on development of alternative dielectric material, whose Si interface properties match the high quality of Si/ SiO$_2$ interface [Tse et al; 2007].

Therefore, as substitution of SiO$_2$, high-k dielectric materials have attracted extensive attention in the last decade due to their great potential for maintaining further down-scaling in equivalent oxide thickness (EOT) with a physically thicker film and a low dielectric leakage current. So with the help of high-k material may replace today's silicon dioxide technology not for 32 nm or 22 nm but can also be scaled to the end-of-the roadmap technology nodes. In the next section, extensive literature survey about high-k material has been given.
1.2.2 SURVEY OF HIGH-k MATERIALS

As SiO$_2$ has served as a perfect gate dielectric for CMOS technology, but now it has reached up to maximum scalable limit. Further reduction of SiO$_2$ led to exponential growth in the static power consumption, due to quantum mechanical tunneling through thinner SiO$_2$ gate dielectric. So there is pressing demand for high-k materials. In order to achieve this goal intensive efforts are needed to find an alternative to SiO$_2$. This material must be suitable to address all the problem i.e SCE and power consumption requirements. This material must be capable for the continuation of down scaling of MOS devices by Moore’s law.

Recently intensive global search is now in progress for new materials for these gate dielectrics. Now a days mainly Al$_2$O$_3$, ZrO$_2$, HfO$_2$, Y$_2$O$_3$, La$_2$O$_3$, Ta$_2$O$_5$ and TiO$_2$ high-k material are under investigation. A brief survey of these materials is given in next section.

Aluminum Oxide (Al$_2$O$_3$)

In 1999 Buchanan reported that Al$_2$O$_3$ have high permittivity, high bandgap, high band discontinuities, and good break down voltage. Moreover p-MOSFETs failed to function due to Boron diffusion through the Al$_2$O$_3$ layer to the Si channel. Al$_2$O$_3$ on Si showed a flat band voltage shift in the positive direction [Buchanan et al; 2000]. The degradation of mobility of the transistors has been observed at higher temperatures (~1000°C), due to Al diffusion into the channel [Guha et al; 2001]. This shift could arise from either damage associated with gate electrode deposition or further processing steps. Among the other candidate of high-k gate oxide, amorphous Al$_2$O$_3$ shows good stability at high temperature however it does not have sufficient high dielectric constant. Aluminum oxide (Al$_2$O$_3$) found to be with large fixed charge and interface trap density and with only a k value of about 10, which cannot meet our future requirements [Ludeka et al; 2001]

Zirconium Oxide (ZrO$_2$)

ZrO$_2$ is widely studied due to its dielectric constant ($\kappa \sim 25$) as well as higher band gap (~5.8 eV). It is also thermodynamically stable with Si. However the crystallization temperature is about 500°C, which is low for ULSI processing.
Lucovsky et al., has reported that transition temperature can be improved by adding impurities into the film [2001]. This is because the dopant atoms distort the original ordered structure and therefore increase the entropy which in turn suppresses the crystallization process. Elements such Si, Al, and N is reported as effective dopant for this purpose [Manchanda; 2000]. Chui et al., had obtained 6-10 Å EOT for ZrO$_2$ on the Ge p-MOSFET [2001].

**Hafnium Oxide (HfO$_2$)**

HfO$_2$ was also under research due to its high dielectric constant and large energy band gap with high band offset. It was found that operation voltages for n- (p-) MOSFETs are 0.8 V (–0.9V) for static Bias temperature instability (BTI), and 1.3 V (–1.7 V) for dynamic BTI at 1 MHz. It was possible to grow 1-2 nm HfO$_2$ by Atomic Layer Deposition with EOT –0.2-0.4nm. So far the thinnest EOT of HfO$_2$ is 0.6 nm [Koike et al; 2003]. Umezawa et al [200]; has reported that incorporation of N atoms reduce the leakage current by coupling with oxygen vacancies in HfO$_2$.

Incorporation of Fluorine (F) with HfSiON gate dielectric could effectively reduce the trap density and lower the threshold voltage [Inoue et al; 2005]. Therefore, adding different atoms such as F, Nitrogen (N), and Oxygen (O) etc with the Hafnium improve the performances. Recently Wana et al [2009] reported that like ZrO$_2$, HfO$_2$ on Si substrate suffers from low crystallization temperature (~ 500°C). This crystallization temperature could be increased by incorporating Al$_2$O$_3$ with the HfO$_2$ (Hf$_x$Al$_{1-x}$O$_1$y). There was an interfacial layer at HfAl$_2$O$_5$/Si interface which decreases the interface defects and eventually reduces the leakage current. By creating Ti capping layer on HfAl$_2$O$_5$, the interfacial layer could be removed partially. The Ti layer act as an O-gartering layer to remove the interfacial layer as well as the surface roughness of Ti/HfAl$_2$O$_5$/Si interfaces. Bias temperature instability (BTI) is very important for n-MOSFET.

**Yttrium Oxide (Y$_2$O$_3$) and Lanthanum Oxide (La$_2$O$_3$)**

Y$_2$O$_3$ was a good candidate for high-k dielectric oxide as it has higher band gap of 6eV, high dielectric constant 14~17 and good thermal stability up to 2325°C [Gurvitch et al; 1987]. Both Y$_2$O$_3$ and La$_2$O$_3$ had large dielectric constant ~18-30 [Mahalingam et al; 1981]; and energy band gap of 4.3 eV. But both of them had
unwanted interfacial layer due to reaction with silicon. Moreover, yttria and lanthana had highly intrinsic positive fixed charge that causes the mobility reduction. Yttrium oxide (Y$_2$O$_3$) had problem of high interface density >10$^{12}$ eV$^{-1}$cm$^{-2}$, low crystalline temperature, and formation of silicide and silicate.

Lanthanum oxide (La$_2$O$_3$) and Lanthanum aluminum oxide (LaAlO$_3$) having dielectric constant ~30 and band gap ~6 eV had thermal stability with temperature up to 850 °C with amorphous nature and main problem of moisture absorption. Wong et al recently reported that the incorporation of nitrogen gives rise to several favorable consequences for the improvement in interfacial properties of thin films [2010]. It reduced the amount of silicide bonds at the interface by forming La-N bonds and caused the interface oxidation to occur, which, in turn, significantly suppressed the interface trap density.

**Tantalum Pentoxide (Ta$_2$O$_5$)**

Ta$_2$O$_5$ was a potential high-k candidate as it had high dielectric constant of 25 and reasonable band-gap of 4.4 eV [Devoivre et al; 1998]. Among all high-k gate materials Ta$_2$O$_5$ had emerged as one of the most promising candidate in terms of its chemical and thermal stability and was widely used as an electrolytic capacitor dielectric [Lin et al; 1999]; [Lee et al; 2002]. Also because of its high-k value Ta$_2$O$_5$ found significant place in microelectronics. But due to poor thermal instability with Si and small electron band offset Ta$_2$O$_5$ was not popular for submicron MOSFET.

But incorporation of Hf with Ta$_2$O$_5$ reduces the fixed charge density as well as leakage current [Jagadeesh et al; 2008]. Addition of Zr with Ta$_2$O$_5$ increases the dielectric strength. In 2008 the use of high-K dielectrics was introduced for the first time, to address gate leakage issue. Planar silicon-on-insulator (SOI) technology showed promise for scaling beyond the planar bulk MOSFET limit.

Devices with gate lengths as short as 6 nm and channel thickness of 4.6 nm had been demonstrated recently [Doris et al; 2009]. Also demonstration of ultra-thin-body SOI MOSFETs with channel thickness less than 1nm, or only five atomic layers, showed the maturity of this technology. Recently 2009-2010 Intel corporation manufacturing transistors had set a record $I_{on}/I_{off}$ characteristic with different metal gates and high-k-dielectric material.
Most of the high-k amorphous dielectric tends to crystallize either during deposition or after heat treatment. In CMOS fabrication process 1000°C annealing temperature was required. Therefore the transition temperature of the amorphous oxide should be above 1000°C. However, some high-k candidates such as HfO_2 and ZrO_2 crystallized at a very low temperature of 500°C [Perkins et al; 2002]; [Gusev et al;2003]. By incorporating a third element into the amorphous dielectric the transition temperature could be increased [Lu et al; 2005]. Despite this high-k dielectric could not fully achieve 1000°C requirement. Further is has been observed that nitrogen reduce the diffusion of oxygen in the alloys and this also reduces the crystallization rate sufficiently.

In addition, the processing temperatures in the present CMOS technology is 800°C and above, but Ta_2O_5 was found to have a low crystallization temperature of about 400°C. So by considering the minimum EOT for pure nitride $K = 7.8$ can be thin as 0.35 nm which is thin enough for 18 nm technology node, also for mean $K$ oxinitride (5.8) then minimum thickness will be 0.47 which fulfill the need of 25nm technology node requirement. Si₃N₄ and SiO₂ interface with K value near 7 will provide physical EOT down to about 1.1 nm, pure metal oxides or pseudo-binary alloy of metal oxides with dielectric constant in the range of 15-25 would provide physical EOT down to 0.6 nm [Modes et al; 2005].

Westlinder [2004]; reported that a number of candidate high-k materials, for instance HfO₂ and ZrO₂ as well as their silicates and aluminates, both as mixed oxides and as nano laminate were under investigation. Note that 6 nm was the distance of only 17 atoms in the substrate [Wakabayashi et al; 2004]. Similarly, there was considerable interest in La₂O₃ and Y₂O₃ and their silicates and aluminates. For gate electrodes, Ta or TaN for NMOS and Ru for PMOS appeared promising [Skotnicki et. Al; 2005]. Nevertheless, continued research into new materials and new processes would be necessary in order to continue scaling of MOSFET devices to the 22 nm Technology node, corresponding to $L_g = 9$ nm [Intel Developer Forum; 2008].

Kuhn et al [2011]; reported that the transition from 45nm/40nm to 32nm/28nm will be possible only by the introduction of high-k materials and metal gates (HKMG). Also the INTEL will start volume production of chips using a 28 nm HKMG process later this year, followed by Global Foundries on that node in early 2012.
Also Al₂O₃ shows good stability at high temperature but problem of low dielectric constant. But the ZrO₂ crystallization temperature is about 500°C, which is low for ULSI processing. HfO₂ suffers from the problem of Bias temperature instability (BTI). Also Y₂O₃ and La₂O₃ both have unwanted interfacial layer due to reaction with silicon. Ta₂O₅ shows poor thermal instability with Si and small electron band offset, so Ta₂O₅ is not popular for submicron MOSFET. In the next section survey about TiO₂ is given.

1.2.3 Literature Survey about TiO₂

Now a days wide band gap semiconductor material, having good optical and electrical properties are in demand for futuristic devices. So the TiO₂ is the one which not only meets the requirement but also has the outstanding properties, like non toxicity and chemical stability in hostile environments, which makes it interesting for futuristic devices in microelectronics. The bandgap of the material was found to be 3.5 eV for amorphous films [Fuyuki et al; 1996]; and 3.2 eV for crystalline films by Pascual et al [1978]. These band gaps are good for semiconductor but higher bandgap is required to act as an effective insulator. Fuyuki et al also investigated that TiO₂ had EOT of less than 10Å with dielectric constant of 80 [1986]. Main efforts had been started in 1995 for the application of TiO₂ in microelectronics.

Yan et.al showed that the leakage current through TiO₂ was determined by the thermionic emission over a 1eV barrier (which is the conduction band discontinuity) [1996]. Hubbard et al. [1996]; proposed that the TiO₂ in anatase phase was crystallized in a metastable state at temperatures below 600°C, and it transformed to the rutile phase at higher temperatures. The transition temperature depends on pressure, stress, contaminants and oxygen deficiency. It has been reported in literature that EOT of 3.6 to 13 nm can be achieved when TiO₂ used as gate dielectric. Also the leakage current of the MOS capacitor reduced by almost two orders of magnitude and the breakdown field strength nearly doubled after incorporating the TiO₂ layer. Although having been widely used in discrete capacitors and also in the integrated memory capacitors.

Kittel et al. [1996]; observed that TiO₂ layers were transparent to visible light. It could also be used for photo electrochemical solar cells and was also a promising
material for quantum dot sensitized solar cells and optical brightener in wall colors. Also used in ingredient in sun cream and bone implants photo catalysis, electro devices and photovoltaic cells because of its biocompatibility [Kostlin et al; 1997]; thermal stability, strong oxidized stability, non-toxicity and long term photo-stability. Titanium dioxide (TiO$_2$) based gate insulators were seriously being considered for the applications of the next generation metal oxide semiconductor field effect transistors (for both logic devices as well as for memory devices).

Campbell et al [1997] reported that TiO$_2$ could be used as an alternative gate dielectric material for deep submicron MOSFET’s. For the first time Campbell et al., showed that the TiO$_2$ based MOSFETs, low field effective mobility about a three order lower than the mobility in SiO$_2$ based MOSFET’s. Transistors made with TiO$_2$ showed near ideal behavior but they had challenges with mobility. This mobility reduction was due to interface trap state and surface roughness at TiO$_2$/Si interface. The electron traps in TiO$_2$ was due to oxygen vacancy. But Gan et al. [1998]; reported that TiO$_2$ had a high refractive index. Babelon et al. [1998]; discussed the effect of growth parameters on different characteristics of TiO$_2$ thin films grown on 100 oriented Si. It was studied that the grain size increases from 30nm 450 °C to 50 nm at 550 °C. Binding energy at peak was reported approximately 500 eV and band gap around 5.7 eV. However, the channel mobility was found to be very low, probably due to the presence of large interface states.

In a comparison of SiO$_2$ and TiO$_2$ as FET gate insulators, thicker layers of TiO$_2$ were used for the same EOT. This prevents direct tunneling between the gate and substrate, but leakage current remained a concern because the band gap was reduced from approximately 9eV of SiO$_2$ to about 3.6eV of TiO$_2$. Meanwhile, the k value of the TiO$_2$ films may be too high that would result in a two-dimensional electric fringing field from the drain through the thick (physical) gate dielectric. The fringing field could lower the source-to-channel potential barrier and the threshold voltage [Robertson; 2000]. It the literature it was clear that the leakage current at moderate bias was determined by thermionic emission over a 1.0 eV barrier that was assumed to be the conduction band discontinuity [Gusev et al; 2000].

Ban David et al. [2000]; deposited thin films of titanium dioxide on conducting (100) silicon wafers by filtered arc deposition. The refractive index values of the
amorphous, anatase and rutile films were found to be 2.56, 2.62 and 2.72 at wavelength of 550 nm, respectively. The morphology of TiO₂ on silicon substrates changes from anatase to amorphous and then to rutile phase without auxiliary heating and, by using an appropriate substrate bias. The effect of surface morphology of the electrodeposited TiO₂ was studied by changing the precursor concentrations of the electrochemical bath. It could be a promising as a preparation method for industrial applications.

Erguchi et al; [2001] calculated high dielectric constant (~30 for Anatase phase and ~80 for Rutile phase. Also lide et al; [2001] reported appreciable conduction band offset of 1.2 eV with Silicon. The thicker layers that could be used prevent direct tunneling, but thermionic emission could be a serious concern, particularly if the band alignment was not favorable [Paily et al; 2002]. The TiO₂ films used in this study were deposited by Michael L. et al., [2002]; low pressure chemical vapor deposition (CVD) at various temperatures from 257°C to 400°C. Anatase peaks appeared at 144, 197, 397, 515 and 637 cm⁻¹ and Rutile peaks were found at 448 and 612 cm⁻¹. Rutile had a larger value of peaks than anatase, while refractive indices were found 2.57 for anatase and 2.74 for Rutile.

Kalikow N. et al. [2002]; reported the deposition of TiO₂ films on crystalline silicon by plasma impulse chemical vapor deposition (PICVD). The thickness of grown films was 20 to 510 nm with refractive indices of 2.20 to 2.54 at temperature between 50 and 350 °C. The deposition rate reported by this method was 50nm/min at 350°C. From the Table-1.3 it appeared that TiO₂ has possessing relatively less band gap (~3.6 eV) and also less conduction band offset (1.2 eV) compared to other potential high-K oxides, but according to the requirements of new gate oxide (to replace SiO₂) in terms of its band gap and conduction band offsets it was clear that ‘It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands [Lu at al; 2003].

Dalapati et al. [2003]; provided another possible synthesis route for forming Si₁₋ₓCx layer. Samples of rapid thermal were annealed in QUPLAS reactor under flowing nitrogen at 1046 °C for 30 s. In order to study the electrical characteristics of the TiO₂ films deposited on strained Si₁₋ₓCx layers, MIS structures were fabricated with Al gate (area: 1.96×10⁻³·cm⁻²). A separation of 5.6 eV between two peaks of Ti 2P
confirms the formation of TiO\textsubscript{2}. Inversion capacitance of the MIS capacitors was found to increase with the increase in carbon concentration due to an increase of donor like centers in the Si\textsubscript{1-x}C\textsubscript{x} layers. The value of $D_0$ was found to be $1.5 \times 10^{12}$ cm\textsuperscript{2}/eV for the continuum model. The current-voltage characteristics of the MIS capacitors were measured and observed that the current density ($J$) at 1 V is $10^5$ A/cm\textsuperscript{2} increases sharply with bias and then almost saturates.

Wakabayashi et al; [2004] studied the leakage current had been found to be dominated by the Schottky Emission (SE) at a low electric field, whereas PF emission takes over at higher electric field. So may be used for the next generation metal oxide semiconductor field effect transistors. According to Se et al it was the most promising material in photo catalytic application due to its strong oxidizing powder and high photo stability.

Electrical properties of ultrathin TiO\textsubscript{2} films deposited at 150\degree C on strained-Si heterolayers by microwave Plasma Enhance Chemical Vapor Deposition (PECVD) had been investigated by Chakarboty S et al. [2005]. The extracted values of $D_0$ were $1.19 \times 10^{12}$ eV\textsuperscript{-1}cm\textsuperscript{-2} and $3.36 \times 10^{11}$ eV\textsuperscript{-1}cm\textsuperscript{-2} for as-deposited and annealed samples, and the field oxide charge densities were $5.07 \times 10^{12}$ cm\textsuperscript{-2} and $4.01 \times 10^{12}$ cm\textsuperscript{-2}, respectively.

Bera et al; [2006] provided the solution for mobility and suggested that it could be increased by growing SiO\textsubscript{2}/TiO\textsubscript{2} gate dielectric stack on strained-Si/relaxed-SiGe heterostructure. In strained-Si, the tensile strain breaks the six-fold degeneracy of conduction band into two valleys. This conduction band split causes a very high mobility in the strained-Si layer. Bera et al also suggested that the device speed could be improved by 20-80\% at a constant gate length by using high mobility strained-Si at the channel region.

During the last few years it has been observed that a transparent Oxide Semiconductor having optical band gap wider than 3eV could be applied in microelectronic applications [Borkowska et al; 2006]; i.e. UV photodiodes, transparent transistor, transparent integrated circuits, transparent electrodes, optical radiation photo detectors, wave length selective devices and solar cells etc.
Chowdhury, et al. [2008], deposited thin film of titanium of thickness 15-20 nm using dc magnetron sputtering system on n-type Si substrate at room temperature. The growth of uniform TiO$_2$ films was reported using thermal oxidation of e-beam evaporated Ti films in O$_2$ ambient. It had been shown that it was possible to achieve the leakage current density of $1 \times 10^{-8}$ A/cm$^2$ for the films annealed at 550°C for 30 min. The flat band was estimated to be -0.6 V.

The oxide charge density $Q_i$, was estimated to be of the order of $2.35 \times 10^{12}$ cm$^{-2}$. The metal and semiconductor work function potential difference was found to be 0.35 V. At low temperature, Flower-Northiem tunneling of electron was observed to be dominating while SCLC current mechanism was found to dominant at higher voltages. Two main conduction mechanisms were invoked to explain the current transport in TiO$_2$ thin films, i.e., SE and F-N tunneling [Dalapati et al, 2003; Zhang et al, 2008].

The SE was a process occurring across the interface between a semiconductor (or metal) and an insulating film as a result of barrier lowering due to applied field. The leakage current was found to be dominated by the SE at a low electric field (<1 MV/cm) for both as deposited and annealed samples, whereas PF effect appears only for the deposited samples at moderate electric field (>1 MV/cm).

Zhang et al [2008]; discussed the TiO$_2$ anatase thin films of 1000 nm were deposited by dielectric barrier discharge enhanced chemical vapor deposition (DBD-CVD) method at 400°C for glass substrate under working pressures from 200 Pa to atmospheric pressure. The film surface was closely covered by small Particles with size about 20-50 nm but the TiO$_2$ film deposited at 2000 Pa with size about 100-200 nm. Depending on discharge conditions, different kinds of discharges could be generated, like glow-like discharge, corona- like discharge, or filamentary streamers. The glow like discharge could produce more homogeneous transient plasma and it normally appeared at lower pressure. Obviously it could not be useful for microelectronics application but suitable for display devices and photo detectors.

Ivan et al. [2009]; presented nanocrystalline titania thin films deposited at ambient temperature by DC magnetron sputtering, the triangular columnar grains of the order of 70-100 nm were obtained at 400°C with pressure of 32 m Torr. The anatase and Rutile films of thickness of the order of 500 nm were reported. The
refractive index of the films deposited at different O\textsubscript{2} partial pressure was between 1.8 and 2.25 in the dispersion free region. The optical band gap values to lie between 3.3 and 3.5 eV. The Band gap values for anatase TiO\textsubscript{2} was 3.20 eV and up to 3.70 eV had been reported for the amorphous phase. The results presented that the refractive index and crystallite size decreased with an increase in the percentage of oxygen in the sputtering environment.

The band gap increase with decrease in crystallite size, which was frequently deemed to indicate the onset of quantum confinement effects, light-emitting diode (LED) etc. These may be quite expensive when large-scale production is needed. It was one of the most promising gas-sensing materials due to its high temperature stability, harsh environment tolerance and catalytic properties.

Various thin film deposition techniques such as thermal/electron beam evaporation, pulsed laser deposition, Direct Current (DC)/Radio Frequency (RF) sputtering chemical vapor deposition and ion beam deposition had been widely used for the deposition of TiO\textsubscript{2} thin films. But every method has its merits and demerits in terms of quality of the deposited films as well as applications. Microwave heating required short times, low temperatures and was relatively inexpensive. TiO\textsubscript{2} films on conducting glass were used in new types of solar cells.

However, all above methods had high costs, and the preparation of films in a large area was technically difficult. Recently, wet processes such as sol-gel and electrochemical deposition had emerged as an alternative route for the preparation of the crystalline TiO\textsubscript{2} thin films. Thus, these alternative dielectrics are in the early stages of development and the deposition techniques as well as the process conditions need to be carefully optimized before they can be adopted as an alternative dielectric in MOS ULSI circuits.

1.3 GAP IN LITERATURE

The further downscaling below three atomic layers of about 7 Å is impossible because of limitations of leakage current, interface trap densities, fixed charge density and also the limitations of statistical parameters of fabrications.

Process engineers and technology developers are not able to resolve all the issues that arise as a result of sub-100-nm scaling. The problems are integration
complexities, fabrication and process control difficulties. The gate dielectric thickness is approaching towards atomic dimensions and at 1.2 nm in the 90 nm node. It is about five atomic layers of oxide with conventional SiO$_2$ gate dielectric.

So High-k material is required to address the challenges like Power thermal budget, material for insulation, physical and mechanical boundaries, technological problems and economic challenges. Various researchers are working on the feasibility of other alternative high-k dielectric (e.g. Al$_2$O$_3$, ZrO$_2$, Ta$_2$O$_5$, HfO$_2$, ZrSi$_x$O$_y$, Y$_2$O$_3$, Y$_2$O$_3$, and TiO$_2$) for submicron MOSFET. All these high-k materials have some practical limitations. Recently TiO$_2$ is the point of attraction as high-k dielectric.

Also it seems that the choice of high-k material may replace today’s SiO$_2$ technology not only for 32 nm but can also be scaled to the end of technology nodes. The scaling below 16 nm is attainable by alternate to replace Si and to find material for futuristic CMOS technology.

### 1.4 MOTIVATION AND OBJECTIVE OF RESEARCH

From the above literature survey, it has been found that the high-k materials, along with the right process recipe, may reduce gate leakage current density for delivering expected transistor performance. To achieve this milestone high-k material TiO$_2$ is chosen. Because of chemical stability with hostile environment, optical and electrical characteristics it seems to be the next alternate dielectric material for future ULSI technology. Further the present work attempts to explore the possibilities of using Sol Gel and DC Magnetron technique for deposition of titanium dioxide film as dielectric in MOS devices. Keeping in view the importance of TiO$_2$ following are the main objective of the research:

1. To study the alternate Dielectric for MOS devices technology and deposition methods
2. To grow high-k-dielectric films on Si/glass
3. Characterization will be carried out to find out
   a) Quality of dielectric film
   b) Thickness/composition/structure of dielectric film
   c) Dielectric constant (K)
d) C-V analysis  
e) Refractive index  
f) Crystallite Phase analysis  
g) Temperatures effects  
h) Interface trapped charge density  
i) Fixed charge density  
j) Flat band voltage

4. Comparison and evaluation of different deposition methods in terms of leakage current.

Here in this thesis we performed a thorough work on the fabrication and structural/electrical characterization of TiO$_2$ film deposited on Si substrate. In order to achieve the goal we have opted Sol-Gel spin coating method and DC sputtering method to deposit the thin TiO$_2$ films for its potential application to highly scaled MOSFET. All the motives from fabrication of high-k thin nanocrystalline films to their electrical characterization has been successfully achieved. It may seem that TiO$_2$ may be futuristic dielectric material in CMOS technology.

1.5 ORGANIZATION OF THE THESIS

The Chapter 1 presents the general introduction and limitations with down-scaling of MOSFETs. More emphasis has been given on the need for high-K gate dielectrics, also the importance of TiO$_2$ as a gate dielectrics, motivation and Gap in literature. In order to fill the gap in literature, various publications have been contributed, which seems to provide alternate dielectric material for futuristic CMOS devices.

Chapter 2 describes the deposition techniques of thin TiO$_2$ films as well as different characterization techniques used along with their advantages and disadvantages.

Chapter 3 presents the description of the experimental work for the deposition of thin TiO$_2$ films by Sol-Gel Spin Coating method. The principle of sol-gel process, introduction of sol-gel science and technology, sol-gel dip process and photo resist
spinning process are discussed here. The advantages, applications and limitations of sol-gel was also discussed in this chapter.

Chapter 4 is devoted to the experimental work that is carried out by DC Sputtering method and also the detailed analysis of the process parameters which effects the quality and thickness of the desired thin films.

Chapter 5 is aimed to discuss the experimental work carried out and the detailed analysis of the results. Moreover, dielectric properties of these have been analyzed by forming a MOS structure on Silicon wafer/glass. Further this chapter also investigates the influence of process parameters like deposition rate & molar ratio of solution, substrate temperature and annealing temperature on the electrical properties like maximum capacitance, dielectric constant, fixed charge, interface trapped charge and leakage current etc. The films have been characterized by using Atomic Force Microscope, Scanning Electron Microscope, X-Ray diffraction, Capacitance Voltage measurement, Ellipsometry, Raman spectroscopy, Differential Scanning Calorimetry (DSC) and Thermal Gravimetric Analyzer (TGA).

Chapter 6 gives the conclusions, recommendations and the scope for the future work.

1.6 ORIGINAL CONTRIBUTIONS

Followings are the outcomes publications emerged as contributions from this work.

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