ABSTRACT

Transistor downscaling has been the driving force for technology advancements in the semiconductor industry over the last 30 years. In order to mitigate short channel effects, the gate-oxide thickness and source/drain junction depth have been scaled along with the gate length. In the recent years significant progress has been made in the development of high-permittivity (high-κ) gate-dielectric materials and metal gate technology. Further this work has focused on fabrication and characterization of alternative gate high-k dielectric material. This work has presented the evaluation of TiO$_2$ as gate dielectric for their potential use in CMOS devices.

In CMOS technology, SiO$_2$ has been used as gate dielectric for more than few decades. It was also observed that the oxide thickness reaches the atomic level and further scaling is impossible in nanometer range. So introducing a high-k material can help solving most of the problems by using physically thicker high-k gate dielectric films. In order to find substitute for traditional gate oxide (SiO$_2$), few ‘high- k’ gate oxide materials under investigation are Al$_2$O$_3$, ZrO$_2$, Ta$_2$O$_5$, HfO$_2$, ZrSi$_x$O$_y$, Y$_2$O$_3$, Ya$_2$O$_3$ and TiO$_2$.

Aluminum oxide Al$_2$O$_3$, was found to have large fixed charge density (Q$_f$) and interface trap density (D$_i$) and has a low dielectric constant around 10, so cannot meet our future requirements. ZrO$_2$ is widely studied due to its dielectric constant (κ ~ 25) as well as higher band gap (∼5.8 eV). It is also thermodynamically stable with Si. However, the crystallization temperature is about 500°C, which is low for ULSI processing. Among all high-κ gate materials Ta$_2$O$_5$ has emerged as one of the most promising candidate in terms of its chemical and thermal stability and is widely used as an electrolytic capacitor dielectric. But due to poor thermal instability with Si and small electron band offset Ta$_2$O$_5$ is not popular for submicron MOSFET. HfO$_2$ has been extensively studied due to its high dielectric constant and large energy band gap with high band offset. ZrO$_2$, HfO$_2$ on Si substrate suffers from low crystallization temperature (∼ 500°C). Like Y$_2$O$_3$, La$_2$O$_3$ has relatively large dielectric constant ~18-30 and has an energy band gap of 4.3 eV. But both of them have unwanted interfacial layer due to reaction with silicon.
TiO$_2$ is very well known and well researched material due to its chemical stability in hostile environment, wide band gap semiconductor, optical and electrical properties, and have potential applications in catalysis, sensors, photodecomposition of water, photo catalyst and antireflection coating. TiO$_2$ thin films have been successfully used in sustainable energy source because of its high incident photon to electron conversion efficiencies.

In this work, we report on the characteristics of TiO$_2$ dielectrics with respect to equivalent oxide thickness (EOT), flat band voltage $V_{FB}$, leakage, work function and thermal stability. For CMOS devices, work function of gate electrodes must be near the valance band and conduction band edges of Si. Although several metal gate electrodes have been identified for SiO$_2$ dielectrics based on their work function, thermal stability and carrier concentration, their compatibility with high-k dielectrics is not fully understood. So the thermal stability of metals on high-k, Fermi level pinning and the performance are of great concern.

This work is aimed at the study of the influence of various process parameters like molar ratio of solution, deposition rate and annealing temperature on the electrical properties like capacitance, dielectric constant, fixed charge, interface trapped charge and leakage current etc. For making this analysis, we have used p type single crystal silicon <100> as substrate and employed Sol-Gel spin coating method and DC sputtering method for the deposition of TiO$_2$ Nanocrystalline thin films. For bulk CMOS devices, gate metals also have important role to affect the work functions. This thesis investigates the impact of different metal electrodes including thermal stability on high-k, work function values, Fermi-level pinning and performance.

Titanium isoproxide (TIP) was used as titian precursor. The sol was prepared by the hydrolysis and condensation of Ti(OC$_3$H$_7$O$_2$)$_4$ in C$_2$H$_5$OH in the presence of HCl. The acetic acid was used as additive chemical to control the reaction kinetic and to moderate the reaction rate. To obtain the hydrolysis the water was added gradually under magnetic stirring. The final mixture was maintained under magnetic agitation at 85$^\circ$C to 95$^\circ$C for 2 hours. To obtain the film, the substrate was placed on spinner and drops of the above mentioned solution were placed on the substrate. The substrate
was then allowed to spin for 1 to 5 minutes with spinning rate of 2000 to 4000 rpm. The sample was removed from spinner and baked for 20 minutes at 95°C. Successive spin coating cycle (sol-gel deposition plus heat treatment) of the substrate was carried out in the sol-mixture. After each spin coating cycle, the film is annealed in the dynamic air at 550°C for 30 minutes.

Further, in the DC reactive magnetron sputtering, Ar and O₂ with 99.9% purity were used as sputtering and reactive gas respectively. A rotary and diffusion pump combination was used to get the desired vacuum. After attaining the base pressure, the oxygen partial pressure was set at 10⁻³ mbar. Later continues flow of argon was let in with maintained sputtering pressure. Before each run the target was pre-sputtered in Ar atmosphere for 5-10 minutes, in order to remove the surface oxide layers of the target. All the samples were deposited at a pressure of 1×10⁻⁵ mbar.

The TiO₂ film thickness and optical characteristics were determined by Stylus Profilometer and Ellipsometry respectively. Scanning Electron Micrograph (SEM) were obtained using JEM-1200 EX JEOL model. The accelerating voltage was kept at 5 KV. The X-Ray diffraction analysis was done with Philips model PW 1729-X-Ray diffractometer. The target consists of copper metal, whereas nickel metal is used as β-filter. The accelerating voltage was kept at 30 KV. The tube current was kept at 15 mA.

To determine various peaks obtained in XRD spectrum Joint Committee Powder Diffraction Standards (JCDPS) files were used. The electrical measurements C-V (Capacitance Voltage) and I-V (Current Voltage) of the MOS capacitors structure Al/TiO₂/ Si, were taken by C-V Keithley 590 CV analyzer and Agilent model (4284A) LCR analyzer respectively in a probe station. Lab view software was used to interface L-C-R meter with computer for plotting data.

The capacitors were fabricated and electrically tested to characterize the material and to inspect the device performance. A physical mask was used to make (top electrode of Pt 500 nm and Al 800 nm) dots on the front side of TiO₂ film. Annealing treatment was given to the samples in vacuum at 300°C before the deposition of dots. For performing the bi directional Capacitance–Voltage scan on MOS capacitor an alternating voltage of 5mV amplitude is super imposed onto a DC
voltage, which is swept from accumulation region to inversion region (i.e. from \(-5\) voltage to \(+5\) voltage) and again from inversion to accumulation. Raman spectroscopic studies were carried out using WiTec CRM 2000 Raman spectrometer couples with high resolution confocal optical microscope.

The characterization of the samples was carried out at room temperature. The morphology of the deposited films was carried out by two dimensional AFM and SEM images. The film was sintered at 350°C, 450°C, 550°C, 650°C and 850°C, respectively under dynamic air for one hour. The obtained TiO\(_2\) films were usually in an amorphous state and the heat treatment determines the degree of crystallinity as well as the crystalline modifications.

The porous nature of the film was confirmed using XRD and SEM analyses. The raman spectra shows well defined peak and the absence of overlapping peaks confirms the well crystallinity of thin films with low number of imprefection sites. The six Raman peaks were analyzed at 145 cm\(^{-1}\), 199 cm\(^{-1}\), 397 cm\(^{-1}\), 516 cm\(^{-1}\) (doublet) and 637 cm\(^{-1}\) corresponding to active mode of anatase phase.

The C-V curve and obtained value of dielectric constant 58 shows that the TiO\(_2\) films may be used as high K-dielectric material in MOS devices to overcome the problem of tunneling in conventional thin oxide films. The maximum value of dielectric constant of the different samples deposited by Sol-gel and DC Sputtering method was found to be 58 and 39 respectively. The shifting in C-V curve has been noticed for as deposited films and when annealed in N\(_2\) atmosphere. It was also found that the dielectric constant of the films was seen to increase after annealing at higher temperature.

The best value of fixed charge density (\(Q_{it}\)), achieved by DC Sputtering method was found to be \(1.34\times10^{11}\) per cm\(^2\) at a deposition rate of 2.0 nm/minute and at 550°C annealing temperature. The ranges of \(Q_{it}\) values that we have obtained, are varied from \(1.0\times10^{11} - 1.0\times10^{12}\) per cm\(^2\) and the \(D_i\) value showed variation in the range of \(1.0\times10^1\) cm\(^{-2}\)eV\(^{-1}\) to \(7\times10^2\) cm\(^{-2}\)eV\(^{-1}\). The best value of Interface trap density (\(D_i\)) was obtained as \(0.8\times10^2\) cm\(^{-2}\)eV\(^{-1}\) for the sample deposited by sol-gel
method and annealed at 550°C. The minimum EOT observed was in the range of 10-16 nm, and the dielectric constant in the range of 19-60 was obtained.

Further, from the I–V characteristics, it has been found that the leakage current is following the Schottky emission characteristics at lower electric fields (<1 MV/cm) and is following the Fowler–Nordheim tunneling mechanism at higher electric fields. From the I–V analysis it also has been revealed, that the leakage current density is increasing with increasing annealing temperatures. Also leakage current density, of the order of 1V of 10 mA/cm², was obtained, which may be acceptable for fabricating high performance and low power logic circuits. It was also found that the formation of oxides and inter-diffusion at the interface between electrodes and TiO₂ causes change in potential barrier height. So the choice of the top electrode material may affect the C-V and I-V characteristics.

The leakage current density values obtained are higher than the required for the microelectronic devices, whereas the interface state density values and fixed charge density values are in the same range of values that are reported with this particular oxide and more care has to be taken to minimize these parameters. The EOT values we have achieved are also falling into the range of values that it actually takes as it was reported in the literature.

In the end, the conclusions drawn from the studies along with the recommendations for future work have been given. Additional study on the doping in TiO₂ including H₂ or D₂ gas annealing at high temperature will be required to improve interface states. Though it is still controversial, it will be able to improve the channel carrier mobility. Also the thermal stability of high K gate dielectrics needs to be improved. Further optimization of surface and interfacial nitridation is needed and other techniques, such as alloying with Zn, Mg and other metals can be studied.