Chapter 5

EXPERIMENTAL RESULTS AND DISCUSSIONS

5.1 INTRODUCTION

This chapter evaluates the various properties of the optimized titanium dioxide thin films deposited by Sol-Gel spin coating and DC sputtering method on P-type silicon wafer. The films are characterized by using Atomic Force Microscope, Scanning Electron Microscope, X-Ray diffraction, Capacitance Voltage measurement, Ellipsometry, Raman spectroscopy, Differential Scanning Calorimetry (DSC) and Thermal Gravimetric Analyzer (TGA).

5.2 RESULTS AND DISCUSSIONS

The experimental work is aimed at the preparation of TiO$_2$ thin films and to study the effect of fabrication method and other post deposition process parameters such as annealing temperature, effect of deposition rate and molar ratio in the sol and effect of top electrode on the electrical properties of the prepared films. In order to achieve all this surface morphology, optical and electrical characteristics have been analyzed.

5.2.1 SURFACE MORPHOLOGY OF SAMPLES BY AFM & SEM

Evolution of the surface morphology of the TiO$_2$ films has been examined by Atomic Force Microscopy (AFM) as shown in Figure-5.1, 5.2 and 5.3. The AFM (Model Pro 47, NT MDT) images have been acquired in the tapping mode. Also the scan area of $1\mu m \times 1\mu m$ has been taken for 2-D analysis of these images. The repulsive force between the AFM cantilever tip and the sample surface is kept constant at 1 nN.

The characterization of the obtained samples is carried out at room temperature. Figure-5.1 shows a large-scale two-dimensional (2D) AFM image of the TiO$_2$ thin film deposited under ambient conditions and annealed at 350°C.

Figure 5.1 illustrates a smooth surface having no indication of grains at 350°C. Whereas in Figure-5.2 sample annealed at 550°C shows granular structure. From the AFM images, it is evident that the surfaces of the films become smooth after annealing.
Figure 5.1: AFM images of TiO$_2$ film deposited by Sol-Gel method and annealed at 350°C

Figure 5.2: AFM images of TiO$_2$ film deposited by Sol-Gel method and annealed at 550 °C
Figure 5.3 reveals the 2-D AFM images of the TiO$_2$ thin films annealed at 850°C. In this figure bigger size of crystallites is clearly visible. So it can be concluded that the deposited TiO$_2$ films are usually in an amorphous state and the heat treatment improves the degree of crystallinity.

**Figure 5.3:** AFM images of TiO$_2$ film annealed at 850°C (scan area 1μm × 1μm)

In addition to this AFM images of TiO$_2$ film (50 nm thickness) deposited by DC Sputtering samples have also been taken. Two such AFM images are shown in Figure-5.4 and 5.5. The AFM images confirm that both the films are composed of small islands as reported in literature [Bera et al, 2006; Chudhary et al, 2008]
Figure 5.4: AFM image of TiO$_2$ film as deposited with oxygen flow rate of 7 sccm (scan area 10μm × 10μm)

The root mean square (rms) roughness as determined using AFM is ~3 nm. The grain size of the films is about 50 nm.

Further in Figure-5.5 it has been noticed that grain size decreases from 50 nm to 42 nm as the oxygen flow rate is increased from 7 sccm to 10 sccm and the same pattern has been revels for the oxygen flow rate of 15 sccm. It has been observed that the roughness obtained from the AFM images is the convolution of the shape and local roughness of the island. The rms roughness obtained for this film found to be 5.7 nm, revels better quality of deposited film at higher oxygen flow rate.
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Figure 5.5: TiO$_2$ film as deposited with oxygen flow rate of 10 sccm

Table 5.1 shows the variation of root square roughness and average roughness of the TiO$_2$ films with different oxygen flow rate. From this data it is clearly visible that $R_{\text{rms}}$ and $R_a$ values increases with increase in oxygen flow rate. This increase may be due to the fact that presence of oxygen acts as impurity in the film and it reduces the movement of titanium on the surface and hence the roughness of surface increases.

Table 5.1 The Average Roughness ($R_a$), Root Mean Square (RMS) roughness with different oxygen flow rates

<table>
<thead>
<tr>
<th>Oxygen flow rate</th>
<th>Grain size (nm)</th>
<th>$R_a$ (nm)</th>
<th>$R_{\text{rms}}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7%</td>
<td>50</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>10%</td>
<td>42</td>
<td>7</td>
<td>5.7</td>
</tr>
<tr>
<td>15%</td>
<td>33</td>
<td>9</td>
<td>8</td>
</tr>
</tbody>
</table>
Further Scanning Electron Micrograph (SEM) is done using (JEM-1200 EX) JEOL model. The accelerating voltage is kept at 5 keV. The nanocrystalline thin films deposited by Sol-Gel spin coating method on corning glass is shown in Figure-5.6.

Figure 5.6: TiO$_2$ thin film deposited on corning glass by Sol-Gel spin coating method and annealed at 350°C

Scanning Electron Microscopy analysis is also performed on the samples deposited by DC Sputtering method with different deposition rates as shown in Figure-5.7 and 5.8. The grain size calculated from the SEM images are found to be 26 nm to 56 nm respectively for the films deposited at oxygen flow rate of 7sccm and 15sccm respectively.
From the Figure-5.7 and 5.8 it is clear that the grain size improved with increased deposition rate. As the structure is the most responsible factor for physical properties of deposited films. Increase in grain size has been observed with increasing temperature and with the increasing oxygen flow rate as well. Though the annealing temperature of films affects the structure greatly, the result of increase in grain size, accompanied by a reduction in the actual number of grains, also shows the roughness of deposited films. These results to decrease total boundary area.

Figure 5.7: SEM images of TiO$_2$ thin films deposited by DC Sputtering method at oxygen flow rate of 7sccm and annealed at 550°C
Figure 5.8: SEM images of TiO$_2$ thin films deposited by DC Sputtering method at oxygen flow rate of 15sccm and annealed at 850°C

Also it is clear that the DC sputtering deposited films shows better stoichiometry condition than the films deposited by Sol-Gel spin coating method. Further sizes of crystallite and phases of TiO$_2$ thin films can be measured by X-Ray diffractions analysis.

5.2.2 X-RAY DIFFRACTION

X-ray diffraction techniques reveal information about the crystal structure, chemical composition and physical properties of thin films. These techniques are based on observing the intensity of diffracted X-ray beam hitting a sample.

The X-Ray diffractometer (Philips model PW 1729) analysis is used to know different phases presented in thin films. The target consists of copper metal, whereas nickel metal is used as β-filter. The accelerating voltage is kept at 30 KV. The tube current is kept at 15 mA. The target consists of copper metal whereas nickel metal is used as β-filter working with Cu Kα radiation of wavelength $\lambda = 1.54060$ Å. The Giono scan is performed at the scan rate of 0.01° sec$^{-1}$ with a fixed time scan and a time per
step of 4 sec. Joint Committee Powder Diffraction Standards (JCDPS) files are used to identify the various peaks obtained in XRD spectrum.

The XRD spectra of the films deposited by Sol-Gel spin coating method and DC sputtering method are analyzed. The horizontal axis represents the angle 2θ (in degrees) and the vertical axis represents the intensity of the diffracted X-Ray beam from the sample in arbitrary units. The crystallinity, crystal structure, and growth orientations are investigated by XRD.

In order to investigate the effect of the deposition temperature on the crystallinity and the average grain size, the full width at half maximum (FWHM) is calculated from the XRD spectra, and the average grain size can be deduced by the Scherrer’s formula. Figure 5.9 showing XRD spectrum of samples deposited by sol-gel method and annealed at 350°C. No peaks are observed at this temperature. The samples deposited by sol-gel and DC Sputtering method are annealed from 250°C to 950°C in air ambient.

![XRD pattern of Sol-gel deposited TiO₂ film deposited on silicon wafer and annealed at 350°C](image)

**Figure 5.9:** XRD pattern of Sol-gel deposited TiO₂ film deposited on silicon wafer and annealed at 350°C

The grain size is calculated using the Scherer’s equation: \( D = \frac{.89\lambda}{\beta_{1/2}\cos \theta} \), where \( \lambda \) is the X-ray wavelength, \( \beta_{1/2} \) is the full-width at half maximum (FWHM) of the diffraction line and \( \theta \) is the diffraction angle.
A smaller grain size increases the surface area to volume ratio that leads to an enhancement of surface processes. The grains of the titanium dioxide film are of the order of nanometers. The diffraction pattern for DC sputtering deposited samples displays the coexistence of both amorphous and crystalline TiO$_2$ regions by showing the simultaneous peaks in Figures 5.10.

Further the XRD spectra of the films deposited by sol-gel method and annealed at various temperature range of 250°C to 950°C are shown in the Figure 5.12 to 5.15. The diffraction pattern of TiO$_2$ film annealed at 250°C does not exhibit clear peaks indicating that the film is amorphous in nature. Higher annealing temperature results in appearance of new peaks which indicate better crystallinity at higher temperature as shown in Figure 5.10.

![XRD pattern of TiO$_2$ films as deposited and annealed at 250°C, 550°C & 950°C](image)

**Figure 5.10: XRD pattern of TiO$_2$ films as deposited and annealed at 250°C, 550°C & 950°C**

These film shows a predominant orientation of the anatase phase along the (004), (200), and the (211) directions. Figure 5.10 to 5.12 shows the X-ray diffraction spectra of TiO$_2$ films deposited DC Sputtering method at oxygen flow rate of 7 sccm, 10 sccm and 15 Sccm respectively. It clearly can be seen that various structural changes of the TiO$_2$ films are evaluated by X-ray diffraction (XRD) measurements in the 2θ mode.
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Figure 5.11: XRD pattern of TiO$_2$ film deposited on silicon wafer by DC Sputtering methods at oxygen flow rate of 7sccm

It is also clear from Figure-5.10 to 5.13 that grain size also affected from oxygen flow rate. The various structural parameters and the grain size, for the TiO$_2$ thin films as a function of O$_2$ flow rate is given in Table-5.2.

**Table 5.2: TiO$_2$ grain size variations at different O$_2$ flow rate**

<table>
<thead>
<tr>
<th>Oxygen flow rate</th>
<th>Grain size (nm) determined by XRD</th>
</tr>
</thead>
<tbody>
<tr>
<td>7%</td>
<td>54</td>
</tr>
<tr>
<td>10%</td>
<td>43</td>
</tr>
<tr>
<td>15%</td>
<td>35</td>
</tr>
</tbody>
</table>

The peaks are being indexed and found to be that of anatase TiO$_2$. The peak at $2\theta = 25.4$ degrees is the characteristic peak of anatase phase and corresponds to (101) direction. Diffraction peaks (112) and (200) corresponding to the anatase TiO$_2$ phase is also observed in the X-ray diffraction pattern of 550°C and 950°C annealed films. No peak corresponding to the rutile phase of TiO$_2$ is seen in the diffractogram suggesting clearly that only anatase phase has been formed.
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Figure 5.12: XRD pattern of TiO$_2$ film deposited on silicon wafer by DC Sputtering methods at oxygen flow rate of 10 sccm

Figure 5.13: XRD pattern of TiO$_2$ film deposited on silicon wafer by DC Sputtering methods at oxygen flow rate of 15 sccm

The results are well supported by the AFM analysis. The presence of small peaks in the X-ray diffraction pattern as deposited, annealed at 550°C and 950°C films reveal the formation of nanocrystalline TiO$_2$ films.

The peak positions and their relative intensities are consistent with the standard power diffraction pattern of anatase TiO$_2$. Grain size is found to increase with heat treatment temperature, deposition rates and with the flow of oxygen can be confirmed
from Figure-5.1 to 5.6 and from Figure-5.11 to 5.13. These results support the literature with well agreement.

The XRD patterns also shows that the TiO$_2$ thin films deposited under ambient conditions are amorphous and the films annealed at different temperatures are polycrystalline. It suggests that polycrystalline anatase TiO$_2$ films are obtained at these rates. From this analysis it may be concluded that near stoichiometric titanium oxide films have been deposited with DC sputtering method. In addition to morphological characteristics electrical characteristics, dielectric constant and threshold voltage are also investigated by C-V analysis.

### 5.2.3 CAPACITANCE-VOLTAGE (C-V) ANALYSIS

MOS capacitors are fabricated using physical mask with (top electrode of Pt 500 nm and Al 800 nm) dots on the front side of TiO$_2$ film. MOS capacitors are formed by thermal evaporation of aluminum through shadow mask having circular openings of 1 mm diameter. Then capacitors are electrically tested to characterize the material to inspect the device performance.

To MOS Capacitor (MOS-C) capacitance is measured from C-V curves. The MOS-C is typically connected to a C-V analyzer, such as the Keithley Model 590 or Agilent 4284A. The C-V analyzer applies a high frequency (1MHz or 100 kHz) drive signal to the backside of the substrate, via the chuck of a prober. The C-V curves are obtained in the voltage range from –5V to +5V range at 100 KHz frequency.

C-V measurements are performed using the Al/TiO$_2$/p-Si structure to determine the dielectric constant of the TiO$_2$ layer. The C-V analysis from Figure-5.14 to 5.19 shows clearly the regions of accumulation, depletion and inversions. The accumulation is observed during the negative bias voltage sweep because the TiO$_2$ had been deposited onto p-type silicon substrates.

The range of the DC voltage as well as the DC voltage step value is varied between different samples to get the best possible curves. The duration of each voltage step is set as 4sec. As the bias moved towards the positive side, a thin depletion region is formed between TiO$_2$, and the Si acted as a capacitor in series, causing a decrease in the total capacitance of Al/TiO$_2$/p-Si configuration.
The oxide capacitances \( \left( C_{ox} \right) \) as shown in Figure-5.14 and 5.15 are the high frequency capacitances when the device is biased for strong accumulation. In case of Pt top electrode the oxide capacitance is found to be \( \left( C_{ox} \right) 42 \text{ pF} \) as shown in Figure-5.14, whereas it is 55.4 pF in case of Aluminum top electrode as shown in Figure-5.15.

**Figure 5.14:** C-V Characteristics of TiO\textsubscript{2} thin film deposited by Sol-Gel method MOS structure of Si/TiO\textsubscript{2}/Pt (39nm)

Accumulation capacitance should be same because of same oxide thickness, whereas the capacitor with Al top electrode has higher accumulation capacitance value than Pt electrodes. As the heat of formation is more for Alumina than Ti, so Al atoms tend to react with oxygen of the underlying TiO\textsubscript{2}. This results in reduction of the effective oxide thickness (EOT) and also the capacitance is inversely proportional to the oxide thickness. In the inversion region the total capacitance per unit area \( \left( C_{a,\text{min}} \right) \) is the series combination of the oxide capacitance and the steady minimum depletion capacitance.
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Figure 5.15: C-V Characteristics of TiO$_2$ thin film deposited by Sol-Gel method
MOS Structure of Si/TiO$_2$/Al [Kumar M et al, 2010]

The variation of the capacitance (C) with gate voltage ($V_G$) ranging from -5.0V to +5.0 Volts with frequency 100 KHz is experimentally determined C-V data for TiO$_2$ dielectric as shown in Figure-5.15 and SiO$_2$ layer using SUPREM-III is shown in Figure-5.16 respectively.
Figure 5.16: MOS capacitors of Si/SiO$_2$/Al structure

The oxide capacitance ($C_{ox}$) of SiO$_2$ dielectric is found to be 5.202 pF as shown in Figure-5.16 and 46.4 pF for TiO$_2$ as in Figure-5.15. It can be appreciated that the curves for the MOS capacitors with TiO$_2$ dielectric present higher values of capacitance when compared with a MOS capacitors with SiO$_2$ with the same thickness, indicating
its higher dielectric constant value. The maximum dielectric constant obtained for TiO$_2$ deposited by DC sputtering method is 38 and for SiO$_2$ its value is found to be 2.3.

In Figure-5.17 to 5.19 C-V analyses of DC Sputtering samples has been discussed. A typical plot which is showing the simulated low frequency C–V curve along with the practically measured high frequency C–V curve are given in Figure-5.17 for the sample deposited at a deposition rate of 2.0 nm/minute with ambient substrate temperature.

![Figure 5.17: C-V Characteristics of DC Magnetron sputtering Structure Si/ TiO$_2$/Al (43nm)](image)

The C-V analysis of the film has been studied at various flow rates of oxygen keeping the argon flow rate constant. With increase in oxygen flow rate [i.e at flow rates of 7sccm and 15sccm] the oxide capacitance decreases as shown in Figure-5.18 and 5.19. The shifting in C-V curve has been noticed for as deposited films.
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Figure 5.18: C-V Characteristics of TiO$_2$ thin film deposited by Dc Magnetron sputtering Oxygen flow rate of 7sccm

Figure 5.19: C-V Characteristics of TiO$_2$ thin film deposited by Dc Magnetron sputtering Oxygen flow rate of 15sccm annealed in N$_2$ ambient
It is possible to observe that the curves for the devices do not present saturation of $C_{ox}$ (oxide capacitance), also the $C-V$ curves present a threshold voltage shift towards higher values of gate voltage (V), with increase in oxygen content, indicating the presence of a high effective charge density. The high effective charge density can be correlated with the presence of Ti–Ti bonds or/and oxygen vacancies.

Utilizing the oxide capacitance, determined from the $C-V$ curves and from the film thickness measured by ellipsometry the dielectric constant values are calculated as shown in Table-5.3 and 5.4. We have observed both kinds of charges in our study and the magnitudes of the fixed charge densities are calculated. Table-5.6 showing the electrical characteristics of Sol-gel samples annealed at 550°C.

**Table-5.3: Electrical Parameters calculated from Sol-Gel fabricated samples**

<table>
<thead>
<tr>
<th>Fabrication Method</th>
<th>Structure</th>
<th>Thickness (nm)</th>
<th>Dielectric constant</th>
<th>Oxide charge $Q_f$ (cm$^2$)</th>
<th>Flat Band Voltage (V)</th>
<th>Threshold Voltage (V)</th>
<th>Interface trap density ($D_{it}$) (1/cm$^2$ eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol-Gel</td>
<td>Al/Si/TiO$_2$/Al</td>
<td>37</td>
<td>56</td>
<td>$9.1 \times 10^{12}$</td>
<td>$-0.84$</td>
<td>$-1.78$</td>
<td>$1.2 \times 10^{13}$</td>
</tr>
</tbody>
</table>

**Table-5.4: Calculated parameters with the help of C-V curves for Sol-Gel samples**

<table>
<thead>
<tr>
<th>Deposition Method</th>
<th>Flat Band Voltage (V)</th>
<th>Threshold Voltage (V)</th>
<th>Dielectric Constant (K)</th>
<th>Interface Trap charge Density $D_{it}$ (cm$^2$ eV$^{-1}$)</th>
<th>Oxide charge density $Q_{it}$ (cm$^{-2}$ eV$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol-Gel Spin coating</td>
<td>$-0.84$</td>
<td>$-1.78$</td>
<td>55.6</td>
<td>$9.1 \times 10^{12}$</td>
<td>$1.2 \times 10^{13}$</td>
</tr>
<tr>
<td>Dc reactive Sputtering</td>
<td>$-0.53$</td>
<td>$-1.8$</td>
<td>38</td>
<td>$8.7 \times 10^{12}$</td>
<td>$1.2 \times 10^{14}$</td>
</tr>
</tbody>
</table>

The following parameters i.e Oxide thickness, flat band capacitance, dielectric constant, interface trap charge density and Flat band voltage that can be extracted from a high-
frequency C-V (HF-CV) curve:

The oxide capacitance \( C_{ox} \) is the high-frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS-C acts like a parallel-plate capacitor and the oxide thickness may be calculated from \( C_{ox} \) and the gate area using the following equation

\[
t_{ox} = A\varepsilon_{ox}/(1\times10^{-9})C_{ox}
\]

So by comparing the C-V characteristics of the capacitor in Figure-5.16 with the ideal simulated C-V curves, the flat band voltage (-0.83V) of the capacitors is calculated by formula

\[
C_{FB} = \frac{C_{ox}\varepsilon_sA/(1\times10^{4})(\lambda)}{(1\times10^{12})(C_{ox}) + \varepsilon_sA}/(1\times10^{4})(\lambda)
\]

(a) Where \( \lambda \) is the extrinsic Debye length, as calculated

\[
\lambda = \sqrt{\frac{\varepsilon_s kT}{q^2 N_x}}
\]

Where \( kT \) is thermal energy at room temperature

The inversion capacitance per unit area is calculated 46.17 pF as shown in Figure-5.18 for TiO\(_2\) by equation

\[
C_{a,min} = \left[ \frac{1}{C_{ox}} + \left( \frac{q\varepsilon_s N_d}{2(2\phi)} \right)^{1/2} \right]^{-1}
\]

Where \( C_{ox} \) oxide capacitance, electronic charge, \( \varepsilon_s \) is the permittivity of the substrate = 11.7×8.85×10\(^{-14}\), \( N_D \) is density of carrier concentration in the doped substrate, \( n_i \) is carrier concentration in intrinsic semiconductor. Now the flat band capacitance given as

\[
C_{FB} = \frac{C_{ox}\varepsilon_sA/(1\times10^{4})(\lambda)}{(1\times10^{12})(C_{ox}) + \varepsilon_sA}/(1\times10^{4})(\lambda) = 39.7 \text{ pF}
\]

Where \( \lambda \) is the extrinsic Debye length, as calculated

\[
\lambda = \sqrt{\frac{\varepsilon_s kT}{q^2 N_x}} = 1.279 \times 10^{-5}
\]
Where $kT$ is thermal energy at room temperature. Debye length indicates that how far an Electrical event can be sensed within the semiconductor. The flat band capacitance $C_{FB} = 39.7 \, \text{pF}$, $C_{ox}$ is the oxide capacitance $= 41.4 \, \text{pF}$ and $A$ is gate area $= 3.13 \times 10^{-6} \, \text{m}^2$. This $C_{FB}$ is less than the $C_{a,\text{min}} = 46.5 \, \text{pF}$.

The dielectric constant calculated by the CV curve shown in Figure-5.17 using the standard formula:

$$C = \varepsilon_0 \frac{K A}{d}$$

... 5.7

Where $\varepsilon_0 = 8.849 \times 10^{-12} \, \text{F/m}$; absolute permittivity

$K = \text{dielectric constant}$

$A = 3.14 \times 10^{-6} \, \text{m}^2$; area

$d = 4 \times 10^{-6} \, \text{m}$; thickness

The value of dielectric constant is observed from 7-60. The calculated dielectric constant of the different samples deposited by Sol-gel and DC Sputtering method are shown in the Table 5.5. The dielectric constant calculated is found to be 38 which are higher than the dielectric constant of HfO$_2$. By comparing the CV characteristics of the capacitor with ideal simulated CV curves, the flat band voltage of the capacitor can be estimated.

**Table 5.5: Dielectric constant of the high-k and conventional material deposited by sol-gel, DC Sputtering and thermal oxidation methods samples annealed at 350 °C to 850 °C**

<table>
<thead>
<tr>
<th>Deposition Method</th>
<th>Annealing Temp(°C)</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol-Gel TiO$_2$</td>
<td>550</td>
<td>55.6</td>
</tr>
<tr>
<td>Sol-Gel TiO$_2$</td>
<td>850</td>
<td>57</td>
</tr>
<tr>
<td>DC Sputtering TiO$_2$</td>
<td>350</td>
<td>29</td>
</tr>
<tr>
<td>DC Sputtering TiO$_2$</td>
<td>550</td>
<td>38</td>
</tr>
<tr>
<td>Thermal Oxidation SiO$_2$</td>
<td>550</td>
<td>2</td>
</tr>
</tbody>
</table>
It is assumed that the oxide films got transformed to anatase phase due to annealing. The maximum dielectric constant achieved is in the comparable range of the values for this parameter. The deposited TiO$_2$ thin films presented a dielectric constant value of approximately 56 as shown in Figure-5.15, many order of magnitude higher than the obtained for SiO$_2$ (2) in Figure-5.16. The capacitance of DC sputtering samples is found to be 560pF and 1200pF with oxygen flow rate of 7sccm and 15sccm as shown in Figure-5.18 and 5.19.

From the literature it is reported that the anatase phase of the titanium oxide samples will exhibit a dielectric constant of 11-180. The maximum dielectric constant of 39 has been observed for DC sputtering samples as shown below in Figure-5.20.

![Graph showing dependence of dielectric constant on annealing temperature.](image)

**Figure 5.20:** Dependence of the dielectric constant on the annealing temperature.

The dielectric constant variations from 18-39 has been observed for sputtering samples and it is found that the dielectric constant of the films increases after annealing at higher temperature as shown in Figure-5.20. This increase in the dielectric constant with annealing temperature is assumed to result from film densification and from crystallization of a minor amorphous phase in the as-deposited films during the heat treatment.

From the values it is clear that the dielectric constant of the oxide improved with annealing of the films over the samples that are deposited at a substrate temperature of maximum 400ºC. The improvement in the dielectric constants of the annealed films
over the un annealed samples is attributed to the improvement in the crystallinity of the titanium oxide samples with temperature.

The oxide charge density \(Q_i\) of the capacitor can be calculated using the formula, \(C_{ox}(W_{MS} - V_{FB})/A\) Here \(C_{ox}\), \(W_{MS}\), \(V_{FB}\) and \(A\) are oxide capacitance, metal semiconductor work function difference, flat band voltage and area. The average interface trapped charges density that is present in the titanium dioxide gate dielectrics has been measured using the analytical technique given by Jakubowski and Iniewski [1985]. In this technique we need to find out the capacitance values from the corresponding high frequency C–V curve and we need to use the following formula to find out the amount of interface charge density \(D_{it}\).

\[
D_{it} = C_{max} \left( \Delta U_{G} - \Delta U_{G} \right) \left( qA\Phi_F \right) \text{ cm}^{-2} \text{ eV}^{-1} \quad \ldots 5.8
\]

Where

- \(A\) = area of the MOS capacitor
- \(\Phi_F\) = Fermi potential of the P-type Si.
- \(C_{max}\) = maximum Capacitance from the C–V graph
- \(\Delta U_{G}\) = difference of the gate voltages corresponding to the surface potentials of \((1 + \Phi_F/2)\) and \((1 + 3\Phi_F/2)\).
- \(\Delta U_{G}\) = difference of the gate voltages corresponding to the surface potentials \((1 + \Phi_F/2)\) and \((1 + 3\Phi_F/2)\) calculated from the curve.

Table 5.6: Parameters calculated from Capacitance-Voltage data from Figures- 5.19 and 5.21

<table>
<thead>
<tr>
<th>Fabrication Method</th>
<th>Structure</th>
<th>Dielectric constant</th>
<th>Oxide charge (Q) (cm(^2)eV(^{-1}))</th>
<th>Interface trap density (D_{it}) (1/cm(^2) eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol-Gel</td>
<td>Al/Si/TiO(_2)/Al</td>
<td>56</td>
<td>(9.1 \times 10^{12})</td>
<td>(1.2 \times 10^{13})</td>
</tr>
<tr>
<td>DC Sputtering</td>
<td>Al/Si/TiO(_2)/Al</td>
<td>38</td>
<td>(8.7 \times 10^{12})</td>
<td>(1.2 \times 10^{12})</td>
</tr>
</tbody>
</table>
The interface trap density \( (D_{it}) \) is calculated using relation \( (1 \times 10^{12}) C_{it}/Aq \) here 
\( C_{it} \) is the interface state capacitance. The calculated values of dielectric constant, oxide charge density \( (Q_i) \) and interface trap density \( (D_{it}) \) are shown in Table-5.6:

The range of \( D_{it} \) values we have obtained are in the range of \( 1−9 \times 10^{13} \) cm\(^{-2}\)eV\(^{-1}\). The best value of \( D_{it} \) we have obtained is \( 1.0−10^{12} \times 10^{2} \) cm\(^{-2}\)eV\(^{-1}\) for the sol gel deposited sample and with substrate temperature of 550ºC.

- **Flat band Voltage \( (V_{FB}) \)**

The flat band voltage is the most important parameter for a MOSFET because it is the factor that decides the threshold voltage and also the amount and polarity of the fixed charges present in the gate oxide. Various other parameters like thickness of the Titanium dioxide film, metal–semiconductor work function difference value \( (\Phi_{ms}) \), substrate doping concentration \( (N_s) \), area of the capacitor \( (A) \) and also the dielectric constant \( (K) \) values obtained from the experimentally measured curve. An error of ±5pF in the accumulation region capacitance is achieved when we compare the simulated plot to the experimentally measured plot of Capacitance vs. Voltage. This has given a confirmation that the area of the capacitor and the substrate doping concentration and also the dielectric constant we have obtained are accurate. The range of the DC voltage as well as the DC voltage step value is varied between different samples to get the best possible curves.

\[
V_{TH} = \left[ \frac{A}{C_{ox}} \sqrt{4E_s q N_{\text{Bulk}}} | \varphi_B + 2 | \varphi_b | \right] + V_{FB} \quad \text{... 5.9}
\]

\[
V_{TH} \text{ calculated is 2 V.}
\]

By comparing the C-V characteristics of the capacitor with the ideal simulated C-V curves, the flat band voltage of the capacitors is calculated 2V. The oxide charge density of capacitor is calculated by \( Q_i = C_{ox}(W_{MS} - V_{FB})/A \) where \( C_{ox}, W_{MS}, V_{FB} \) and \( A \) are oxide capacitance, metal semiconductor work function difference, flat band voltage, and electrode area \( A \). The analytical flat band voltage is the difference in metal and semiconductor work function, which in our case is −0.87V. Various flat band voltages that we have obtained for our samples showing decreasing behavior and in turns trying to approach to the analytical value for the films deposited at higher
deposition rates. Also the values decreasing with increasing temperature within each set of samples which are deposited at same deposition rate and with same molar ratio samples. The lowering of flat band voltage and its approach towards the analytical value is believed to be because of the decrease in $Q_f$ values at high substrate temperature.

- **Equivalent Oxide Thickness (EOT)**

The EOT values for the best set of samples are shown in the Table 5.7. The minimum EOT that we have achieved is 13nm and is in the range of possible EOT values for TiO$_2$ gate dielectrics, which is reported in the literature [Yang et al.; 2006]. The EOT value of 13nm corresponds to the film that is annealed at 850ºC in N$_2$ atmosphere for DC Sputtering sample, while it is almost same 14nm for Sol-Gel deposited samples shown in Table 5.7.

<table>
<thead>
<tr>
<th>Fabrication Method</th>
<th>TiO$_2$ Thickness (nm)</th>
<th>EOT (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol-Gel</td>
<td>37</td>
<td>14</td>
</tr>
<tr>
<td>Sol-Gel</td>
<td>56</td>
<td>21</td>
</tr>
<tr>
<td>DC Sputtering</td>
<td>35</td>
<td>13</td>
</tr>
</tbody>
</table>

This particular value is lying in the range of the values reported in the literature. Since the dielectric constant obtained corresponding to these samples are 18 and 53 obtained for DC sputtering and sol-gel sample respectively, it is assumed that this could be due to polycrystalline (anatase) nature of the TiO$_2$ film.

$W_{MS}$ (metal semiconductor work function difference ) it is found to be (-1.025 V) using the relation

\[
W_{MS} = W_M - [W_S - \Phi_B + 0.5E_G] \quad \ldots 5.10
\]

Interface Charge is $1.02 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$. using the relation $1 \times 10^{12} \frac{C_u}{A_g}$. The effective oxide charge ($Q_{EFF}$) represents the sum of the oxide fixed charge ($Q_F$), the mobile charge ($Q_M$), and the oxide trapped charge ($Q_{OT}$). The calculation of $Q_{EFF}$ is
CHAPTER 5

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based on the assumption that the charge is located in a sheet at the silicon to TiO$_2$ interface. Its value is found to be $12.9 \times 10^{-8}$ Coulomb cm$^{-2}$ using the relation

$$Q_{\text{EFF}} = C_{\text{it}} (V_{FB} - W_{MS})$$  \hspace{1cm} \text{... 5.11}

And the effective oxide charge concentration ($N_{\text{EFF}}$) is computed using the equation

$$N_{\text{EFF}} = Q_{\text{EFF}} q^{-1}$$  \hspace{1cm} \text{... 5.12}

and is found to be $8.06 \times 10^{11}$ unit/cm$^3$.

The value of oxide charge density for structure Si/TiO$_2$/Al ($Q_{it}$) $7.48 \times 10^{12}$ and interface trap density ($D_{it}$) $4.32 \times 10^{13}$ eV$^{-1}$ cm$^{-2}$ are slightly higher than the values reported in literature [Linsebigler et al.; 1995 and Georgia et al.; 2006]. MOS capacitors are fabricated and it presented a leakage current density of 10 mA/Cm$^2$, acceptable for high performance logic circuits (maximum of 100 A/cm$^2$) and low power circuits (10 mA/cm$^2$) device.

5.2.4 CURRENT–VOLTAGE (I–V) ANALYSIS

For electrical measurements of the structure Al/TiO$_2$/Si MOS capacitor, C-V (Capacitance Voltage) is obtained by Keithley 590 CV analyzer. The current-voltage characteristics of the MIS capacitors are measured and observed that the current density ($J$) at 1 V is $10^{-5}$ A/cm$^2$ increases sharply with bias and then almost saturates.

![Figure-5.21: Leakage current of fabricated MOS capacitor with Pt and Al top electrodes by sol-Gel method for 40 nm films](image)

The leakage current has been found to be dominated by the SE at a low electric field, whereas PF emission takes over at higher electric field. It is clear that
the capacitor with Pt top electrode is having minimum leakage current because of higher resistivity with oxygen of underlying TiO₂ shown in Figure-5.21. In case of Al top electrodes, the Ti ions in the TiO₂ substrate underneath reduced, and long range order of the substrate is lost. So Al layer is oxidized.

The oxide film is continuous to grow a heterogeneous mixture of the aluminum created on top of the oxygen TiO₂ substrate and results to more leakage current. So the choice of the top electrode material affects the C-V (Figure-5.14 and 5.15) and current voltage (I-V) (Figure-5.21) characteristics.

I-V characteristics of TiO₂ thin films have been studied with Al/TiO₂/Si MOS capacitor structure. The input voltage is swept from 0 to ±6 V and the gate leakage current is determined. The current-voltage characteristics are shown below in Figure-5.21. Gate voltage is considered positive when top electrode (Al) is more positively biased then ohmic contact of MOS structure. The electrical properties of TiO₂ films as the gate bias are also investigated. It can be noted that the as deposited film showed a relatively low leakage current (J_L) of about \(10^{-6}\) A/cm² at zero bias and \(5.32 \times 10^{-5}\) A/cm² at a gate bias of +1V as shown in Figure-5.22.

![I-V characteristics of TiO₂ film with Al top electrode deposited by DC Sputtering method](image)

**Figure 5.22:** I-V characteristics of TiO₂ film with Al top electrode deposited by DC Sputtering method

For higher gate voltages two prominent leakage current mechanisms are invoked namely SE and PF tunneling which are similar to reported values elsewhere. The I-V relationship for the SE emission can be expressed as
Experimental Results and Discussions

\[ J = A_{th}T^2 \left[ \exp \left( -\frac{qW_{MS}}{k_BT} \right) \right] \exp \left[ \frac{q}{k_BT} \left( \frac{qV_B}{4\pi\varepsilon_0\varepsilon_r d_{ox}} \right)^{\frac{1}{2}} \right] \] \quad \ldots \quad 5.13

Where \( A_{th}, W_{MS}, \varepsilon_r, \varepsilon_0 \) and \( d_{ox} \) are the Richardson-Dushmann constant, metal work function, relative dielectric constant, vacuum permittivity and oxide thickness respectively.

Figure 5.23 shows the Current (I) versus \( \sqrt{V} \) plot in semi-log scale of the observed data in the voltage range of 0.2 to 0.7 V. It is clear that the current is linear with applied electric field confirms the SE process at lower biases <1 MV/cm. The conduction mechanism at lower biases region is dominant by thermally excited carriers known as hopping mechanism which can confirmed by Figure 5.26.

![Figure 5.23: S-E plot of measured I-V data (Sol-Gel and DC sputtering)](image)

As the bias is increased, the current increases exponentially confirm the SE behavior. It can be observed that hopping conduction mechanism is dominant below gate voltage <1 volt while further increasing the gate bias, the conduction is invoked by F-N relationship as shown in Figure 5.25. F-N tunneling can be expressed by as
$J_{FN} = A_{FN} v^2 \exp\left(-\frac{B_{FN}}{V_B}\right), \quad \ldots \text{5.14}$

$B_{FN} = \frac{8\pi \sqrt{2m^*m_0} (qW_{MS}^{3/2}) d_{ox}}{3qh}, \quad \ldots \text{5.15}$

where $A_{FN}$ and $B_{FN}$ are constants.

Electrical characteristics of our Sol-Gel deposited TiO$_2$ thin films are compared with those of layer grown by other fabrication methods reported in the literature. Figure-5.24 shows the leakage current through similar MOS capacitors fabricated by different techniques.

![Figure 5.24: The comparison of the I-V characteristics grown by Sol-Gel spin coating (39nm) with other methods](image)

The leakage current not only influenced by the depletion region but also depends on the fabrication methods as well. It has been also observed that the leakage current in the Sol-Gel method is linear at lower bias and saturate at higher bias voltages. It is known that titanium oxide layer deposited by PECVD and Plasma exhibits high leakage current and post deposition treatments that have been performed at 750°C for PECVD, 700°C for E-beam and 550°C for thermally grown films [Chong et al, 2006]. Even the leakage current is higher than thermal reported methods whereas the pre deposition at higher temperature increases budget and complexity.
The F-N plot of MOS capacitor is shown in Figure-5.25 with conduction band offset value of 0.87eV while theoretically it should be 1.02 eV.

![Figure 5.25: F-N tunneling for TiO$_2$ gives conduction band offset 0.83 eV. The upper inset shows the current-voltage plot in the range of 0 to ±6 V (DC Sputtering)](image)

In case of Al top electrode, Ti ions in the TiO$_2$ film is reduced due to oxidation of Al. Thus aluminum oxide film continuous to grow a heterogeneous mixture of the aluminum created on top of the TiO$_2$ and results to change in conduction offset value. This effect on lattice structure can be confirmed with XRD analysis and also by DSC-TGA graph as shown in Figure-5.26. The crystalline temperature ($T_c$) is 310°C.

This transition from amorphous solid to crystalline solid is an exothermic process, and results in a peak in the DSC signal as shown in Figure-5.28. Thermal characterization has been performed on DSC/TGA instrument with heating rate of 5°C/min in N$_2$ atmosphere. In the TGA curve (between the temperature ranges of 100°C to 400°C) a considerable weight loss of (17%) is observed which is imputing the loss of
water and transformation of Ti-peroxide to TiO$_2$. DSC shows endothermic at 250°C and exothermic peaks at around 450°C & 800°C.

![DSC-TGA analysis of TiO$_2$ thin films](image)

**Figure 5.26: DSC-TGA analysis of TiO$_2$ thin films**

Table 5.8 shows measured and calculated data about TiO$_2$. Electrical characteristics by considering $T=300^\circ K$, standard physical constant ($q$, $K$, $\varepsilon_0$), and electrode area $1\times10^{-5}$ cm$^2$. 
## Table 5.8: Parameters observed from DC Sputtering C-V graph from Figure-5.19

<table>
<thead>
<tr>
<th>Dielectric constant</th>
<th>Bandgap (eV)</th>
<th>Formation temp. (°C)</th>
<th>Thermal stability (°C)</th>
<th>Interface trap density (eV/cm²)</th>
<th>Oxide trap density (eV/cm²)</th>
<th>Break-down field (MV/cm)</th>
<th>Capacitance (Cox) F/Cm²</th>
<th>Flat band voltage (Vfb) V</th>
<th>Threshold voltage (Vt) V</th>
<th>Bulk potential (ß)</th>
<th>Breakdown current density wrt SiO₂ (A/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22-40</td>
<td>3.6</td>
<td>500</td>
<td>550</td>
<td>1×10⁻²⁻²</td>
<td>8.9×10⁻²⁻²</td>
<td>&lt;4</td>
<td>5.85×10⁻⁸</td>
<td>.37</td>
<td>1.2</td>
<td>.35</td>
<td>10⁻¹⁻²⁻²</td>
</tr>
</tbody>
</table>

Table-5.9 summarizes the major electrical and technological characteristics for various deposition methods.

The further improvements in deposition process are required to make thin films suitable for MOS devices. The grain sizes of the TiO₂ film are 23nm to 54 nm. XRD results indicate that the grain size in all of the phases have been increased after annealing at higher temperature.

The C-V curve and obtained value of dielectric constant shows that the titanium dioxide film may be used as high K-dielectric material in MOS devices to overcome the problem of tunneling in conventional thin oxide films. The maximum dielectric constant as calculated using Capacitance-Voltage measurement is found to be 38 and 56 for Sputtering and Sol-Gel samples respectively.

Several conduction mechanisms of leakage current occur across SiO₂ MOS devices i.e. Fowler–Nordheim (F-N) tunneling, space charge limited current (SCLC) mechanism, Schottky emission (SE) and Poole-Frenkel (PF) conduction, etc. But, whatever the mechanism, the electric filed is common and basic parameter which determines the amount of leakage current. A similar effect has been observed in TiO₂ MOS devices.
Table 5.9: Comparison of parameters of existing deposition methods versus our samples

<table>
<thead>
<tr>
<th>Electric field (MV/Cm)</th>
<th>Thermal (12 nm)</th>
<th>E-beam (15 nm)</th>
<th>Sputtering (13.6 nm)</th>
<th>PECVD (15 nm)</th>
<th>sol-gel spin (52 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>3.16 × 10⁻⁶</td>
<td>3.16 × 10⁻⁶</td>
<td>1.00 × 10⁻⁴</td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>3.16 × 10⁻⁶</td>
<td>1.00 × 10⁻⁶</td>
<td>1.25 × 10⁻⁵</td>
<td>3.98 × 10⁻⁷</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>3.16 × 10⁻⁶</td>
<td>1.00 × 10⁻⁶</td>
<td>1.58 × 10⁻⁵</td>
<td>6.30 × 10⁻⁵</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>3.98 × 10⁻⁶</td>
<td>3.16 × 10⁻⁴</td>
<td>1.99 × 10⁻⁴</td>
<td>7.94 × 10⁻⁵</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>6.30 × 10⁻⁶</td>
<td>3.98 × 10⁻⁴</td>
<td>5.01 × 10⁻³</td>
<td>1.00 × 10⁻⁴</td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td>1.58 × 10⁻⁵</td>
<td>6.30 × 10⁻⁴</td>
<td>6.30 × 10⁻³</td>
<td>1.25 × 10⁻⁴</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>5.01 × 10⁻⁵</td>
<td>1.00</td>
<td>7.94 × 10⁻³</td>
<td>1.58 × 10⁻⁵</td>
</tr>
<tr>
<td></td>
<td>3.5</td>
<td></td>
<td>1.00</td>
<td>1.99 × 10⁻⁴</td>
<td>1.99 × 10⁻⁴</td>
</tr>
<tr>
<td>Refractive index</td>
<td>2.2–2.5</td>
<td>2.1</td>
<td>2.53–2.72</td>
<td>2.12–2.56</td>
<td>2.33</td>
</tr>
<tr>
<td>Optical dielectric constant</td>
<td>4.84–6.25</td>
<td>4.41</td>
<td>6.4009</td>
<td>4.4944</td>
<td>5.428</td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>3.2–3.5</td>
<td>2.69</td>
<td>3.0</td>
<td>3.25</td>
<td>3.4</td>
</tr>
<tr>
<td>Heat treatment °C</td>
<td>550–750</td>
<td>600</td>
<td>700–1000</td>
<td>300–450</td>
<td>400–550</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>15–40</td>
<td>23</td>
<td>15–25</td>
<td>20–35</td>
<td>26–80</td>
</tr>
<tr>
<td>Merits/application</td>
<td>can be used as gate dielectric material</td>
<td>best photocatalystics material, junction based devices</td>
<td>microelectronic materials, enhance mobility MOSFET</td>
<td>solar cell, insulating memory devices, fiber optical sensors</td>
<td>next generation high-k dielectric material for MOS, chip</td>
</tr>
<tr>
<td>Drawbacks</td>
<td>higher leakage current</td>
<td>5 nm roughness in surface, leakage current</td>
<td>fabrication is expensive</td>
<td>fabrication is expensive</td>
<td>higher silicon/dielectric interface density</td>
</tr>
</tbody>
</table>
5.2.5 OPTICAL CHARACTERISTICS

In order to obtain refractive index, structural complexity at the surface of deposited films and crystalline phases of grains can be obtained from spectroscopic Ellipsometry and from Raman analysis.

Spectroscopic Ellipsometry analysis has been performed on all the samples with a thickness of 35–50 nm within a measurement accuracy of 1.2 nm. The refractive index has been measured using Spectroscopic Ellipsometry operating over the wavelength range of 250 nm to 1000 nm for deposited TiO₂ thin films as shown in Figure-5.27 & 5.28.

The refractive index is found to be 2.34 for the samples deposited by DC sputtering method. This is based on measurement of changes in polarization state after reflection from the sample surface. From these data the refractive index (n) and the film thickness is obtained using dispersion law. The obtained refractive index value 2.4 supports the reported values in the literature [Djaoved at al.; 2002].

![Graph showing refractive index vs wavelength]

**Figure 5.27: The different layers present in the sample deposited by Sol-Gel Method**

The thickness and refractive index of layers is varied shown in Figure-5.29, 5.28 and 5.29. The thickness of the deposited film is confirmed using profiler AMBIOS-XP1 model.
Figure 5.28: The $\psi$ and $\Delta$ of the measured and simulated curves

The refractive index of the TiO$_2$ film deposited by sol-gel method, has been measured by Ellipsometry and found to be 2.33 and optical dielectric constant can be determined from the refractive index of TiO$_2$ $\varepsilon_{opr} = \varepsilon_0^2 = 2.33^2 = 5.4389$. The refractive index as a function of O$_2$ flow rate for the DC Magnetron deposited titanium oxide films is presented. The obtained refractive index values are found to vary from (2.42) and (2.53) with change in oxygen content.

Table-5.10 gives the thickness and refractive index of the Titanium Dioxide thin films deposited by various deposition methods. It shows data for the samples prepared by DC sputtering method at the deposition rate of 2.0 nm/minute and Sol-Gel with different molar ratios with the annealing temperature of 550 °C.

<table>
<thead>
<tr>
<th>Deposition Methods</th>
<th>Thickness (nm)</th>
<th>Refractive index(n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol Gel (molar ratio of 1:0.8:0.2)</td>
<td>50 ± 1</td>
<td>2.08</td>
</tr>
<tr>
<td>DC Sputtering 2(nm/minute)</td>
<td>50 ± 5</td>
<td>2.12</td>
</tr>
<tr>
<td>Sol Gel (molar ratio of 1:0.9:0.1)</td>
<td>35 ± 2</td>
<td>2.33</td>
</tr>
<tr>
<td>DC Sputtering 1(nm/minute)</td>
<td>39 ± 2</td>
<td>2.53</td>
</tr>
</tbody>
</table>
Further the absorption spectra of thin TiO$_2$ film has been recorded over the wavelength range of 300 nm to 1000 nm using Spectrophotometer is shown in Figure-5.29.

![Absorption Spectra](image)

**Figure 5.29:** The absorption spectra of TiO$_2$ thin film Deposited by DC Sputtering Method

In this spectrophotometer analysis peak absorbance has been obtained at 345 nm. So the band gap has been calculated 3.6 eV by using equation $\varepsilon = \frac{hc}{\lambda}$, $\varepsilon$ is photon energy, $c$ speed of light and $\lambda$ cut-off wavelength by the help of Spectrophotometer.

The calculated value is in the range of values reported in literature. The band gap value of thin dielectric film may be used for fabrication of memory device in microelectronics applications.

- **Raman Spectroscopy**

  Raman spectroscopy studies has been performed using WiTec CRM 2000 Raman Spectrometers, employing a single mode Ar-ion laser for excitation ($k = 488$ nm) at a power of ~4.4 mW. The particle size has also been determined using a Philips TECNAI F20 High Resolution Transmission Electron Microscope. The Raman spectra of the prepared anatase TiO$_2$ thin film annealed at 550°C. The results of X-ray diffraction analysis are supported by the Raman spectra of TiO$_2$ thin film. Raman spectroscopy is capable of elucidating the titania structural complexity as peak from each crystalline phase is distinct and clearly appears as peaks separated in frequency and therefore the anatase and rutile phases are easily distinguishable.

  The Raman spectra as shown in Figure-5.30 & 5.31 confirm that the films are well crystallized with low number of imperfect sites.
Anatase TiO$_2$ are having six Raman active modes: $A_{1g} + 2B_{1g} + 3E_g$ for Sol-Gel sample as shown in Figure-5.30. Five distinct peaks are being observed having bands centered at 142.5 cm$^{-1}$ ($E_g$), 195.2 cm$^{-1}$ ($E_g$), 394.8 cm$^{-1}$ ($B_{1g}$), 513.3 cm$^{-1}$ ($A_{1g}$) and 635.1 cm$^{-1}$ ($E_g$).

![Raman spectrum of TiO$_2$ thin film deposited by Sol-Gel Method and annealed at 550$^\circ$C](image)

**Figure 5.30:** Raman spectrum of TiO$_2$ thin film deposited by Sol-Gel Method and annealed at 550$^\circ$C

The absence of peaks corresponding to the rutile phase in the Raman spectra confirms the formation of purely anatase TiO$_2$. From Figure-5.30 it is clear that the TiO$_2$ nanocrystalline film shows three Raman peaks at 143, 196 and 639 cm$^{-1}$ and three Raman peaks are being observed at 397 cm$^{-1}$ and 516 cm$^{-1}$, doublet of the $A_{1g}$ and one for $B_{1g}$ mode. The similar peaks have been obtained for DC Sputtering samples as shown in Figure-5.31. In Figure-5.31 three raman peaks at 145, 199 and 637 cm$^{-1}$ are assigned to the $E_g$ mode of active Anantase phase, which supports the result of literature. The peak at 397 cm$^{-1}$ is obtained corresponding to $B_{1g}$ mode and 516 cm$^{-1}$ for the $A_{1g}$ and $B_{1g}$ modes. So TiO$_2$ deposited by DC Sputtering method are showing six Raman active modes $A_{1g} + 2B_{1g} + 3E_g$.

This statement agrees with the results of Djaoved et al. [2002], as they have observed only the typical bands of anatase in the spectra of TiO$_2$ films calcinated at 700$^\circ$C. The Raman spectra shows well defined peaks and the absence of overlapping peaks confirms the well crystallinity of thin films with low number of imperfection sites.
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5.3 CONCLUSION

In this work, the films have been deposited by Sol-Gel and DC sputtering methods. The structural properties are studied by XRD and surface morphology was studied by AFM & SEM. Electrical characteristics were obtained by Keithley CV analyzer and IV setup. Also Comparison has been made for leakage current densities of the Sol-Gel grown TiO$_2$ thin films, with oxide layer grown by other fabrication techniques. The thickness of the deposited film is measured by stylus profiler meter and found to be few tens of nanometers. The refractive index of the films has been found 2.16 to 2.42 by Ellipsometry. A maximum dielectric constant (K) of 39 has been achieved for the films deposited by DC magnetron Sputtering method and 58 for the Sol-gel deposited samples. The values flat band voltages ($V_{\text{FB}}$), interface trap density ($D_{\text{it}}$) and fixed oxide charges ($Q_{\text{f}}$) are being evaluated from the C-V studies.

It has been reported that EOT of 13-21 nm is achieved with TiO$_2$ as gate dielectric and also reduced leakage current by two orders of magnitude is achieved. The studied TiO$_2$
films presents acceptable properties such as low leakage current density of $1 \times 10^{-5}$ A/cm$^2$ at 1 V and band gap of 3.6 eV. The leakage current has been found to be dominant by the Schottky emission at lower electric field, while Flower-Nordheim (F-N) tunneling occurs at higher biasing voltages. may be used as high-k dielectric material as gate oxide for MOSFET. The XRD and RAMAN analysis indicates the presence of anatase TiO$_2$ phase in film.

The films deposited at higher temperature are being showing better crystallinity. So much more research is to be performed in order to clarify the relationship between microscopic aspects (interfaces, structure, and bonding) and macroscopic features and properties (crystalline, texture, etc.). The understanding of such connections is essential for establishing defined and reproducible processes. So it can be concluded that in order to improve the acceptability of TiO$_2$ in MOS devices post deposition annealing along with the right process recipe are required to reduce the gate leakage current, for delivering expected transistor performance. The conclusions, recommendation and future scope of work is given in chapter-6.