CHAPTER 4

DYNAMIC THRESHOLD - LEAKAGE
CONTROL TRANSISTOR (DT-LECTOR)

4.1 INTRODUCTION

This chapter presents DT-LECTOR, a robust method which is equally effectual for static power control in CMOS VLSI circuits for System on Chip (SoC) applications in deep submicron technologies. DT-LECTOR is a combined structure of Dynamic Threshold MOS (DTMOS) and LEakage Control TransistOR (LECTOR) techniques. Compared to the leakage savings obtained individually for DTMOS and LECTOR respectively, the combined structure DT-LECTOR gives more savings in terms of leakage with reduced delay. First the structure and working of DTMOS and LECTOR is discussed to give better understanding about the combined structure DT-LECTOR. Finally DT-LECTOR is explained with simulation results.

4.2 DTMOS

The DTMOS is formed when the gate and body of a MOSFET is tied together as shown in Figure 4.1. Because of the body effect, the threshold voltage of MOSFETs can be changed dynamically during different modes of operation. When the device is OFF, the leakage is low and the leakage is high when the device is ON. When $V_{gs} = 0$, the threshold voltage $V_{th}$ is high resulting in low leakage current (Assaderaghi 1994) (Assaderaghi 1997).
However, the current drive is high when the gate voltage is raised for low $V_{DD}$ values. The threshold voltage $V_{th}$ increases when the body to source reverse bias $V_{bS}$ is made larger. By connecting the gate to the body, a forward bias is achieved between body to source forcing the threshold voltage $V_{th}$ to drop resulting in high performance. The DTMOS with lower threshold voltage does not come at expense of higher off-state leakage. The DTMOS and a regular device have the same threshold voltage when $V_{bS} = V_{gs} = 0$.

![Cross section of an SOI - NMOSFET with body and gate tied](image)

**Figure 4.1 Cross section of an SOI - NMOSFET with body and gate tied**

### 4.3 LECTOR

LECTOR (Narender H. 2004) is an adaptation of the technique of effective stacking of transistors in order to reduce leakage power. Figure 4.2 shows the generic block diagram of a LECTOR CMOS circuit. Two Leakage Control Transistors (LTs), LT1 and LT2, are introduced between PUN and PDN. These LTs act as self-controlled stacked transistors. The LTs are sized accordingly and are high $V_{th}$ when compared to other transistors in the circuit.
This wiring configuration ensures that one of the LTs is always near its cut-off region, irrespective of the input vector applied to the CMOS circuit. The introduction of LTs increases the resistance of the path from $V_{DD}$ to ground, thereby reducing the leakage with additional area and delay penalty.

![Generic LECTOR](image)

**Figure 4.2** Generic LECTOR

### 4.4 DT-LECTOR LEAKAGE REDUCTION

The DT-LECTOR method employs two self controlled stacked Leakage control Transistors (LTs) for every CMOS gate in the path $V_{DD}$ to ground. This method is based on the observation that stacking of transistors results in low leakage as the resistance offered by the OFF transistors is very high (Sirichotiyakul 2002). The gate of each LT is driven by the source of the other LT which ensures that one of the LT is always near its cut-off, offering high resistance in the path $V_{DD}$ to ground. However a significant delay is encountered due to the two additional Leakage control Transistors (LTs) connected in series in the output path. The LT’s are modified to operate as DTMOS when the floating body and gate of the respective LT’s are tied together.
The gate and body of the LT’s are held at the same potential as shown in Figure 4.3 in case of a general CMOS gate with the proposed method. The additional delay introduced due to the leakage control transistors is reduced as the threshold voltage is lowered by DTMOS as given by the Equation (4.1) without need for sizing the LTs.

\[
\text{Delay} \propto \frac{V_{dd}}{(V_{dd} - V_{th})^2}
\]  

(4.1)

Figure 4.3 Generic structure of DT-LECTOR CMOS

Table 4.1 shows the voltage values at nodes ‘a’ and ‘b’ in Figure 4.3 for a two input NAND gate using DT-LECTOR. This voltage levels ensures the proper operation of LTs.
Table 4.1 Nodal voltage matrix of two input NAND gate in DT-LECTOR

<table>
<thead>
<tr>
<th>Transient Time (ns)</th>
<th>Voltage @ Node a (V)</th>
<th>Voltage @ Node b (V)</th>
<th>Transient Time (ns)</th>
<th>Voltage @ Node a (V)</th>
<th>Voltage @ Node b (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>105.267m</td>
<td>287.610u</td>
<td>16</td>
<td>97.684m</td>
<td>285.665u</td>
</tr>
<tr>
<td>1</td>
<td>0.960</td>
<td>0.954</td>
<td>17</td>
<td>100.602m</td>
<td>297.734u</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0.957</td>
<td>18</td>
<td>101.674m</td>
<td>291.608u</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0.961</td>
<td>19</td>
<td>102.468m</td>
<td>282.752u</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0.962</td>
<td>20</td>
<td>103.261m</td>
<td>273.895u</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0.962</td>
<td>21</td>
<td>0.949</td>
<td>0.902</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0.962</td>
<td>22</td>
<td>1</td>
<td>0.915</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0.962</td>
<td>23</td>
<td>1</td>
<td>0.962</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0.962</td>
<td>24</td>
<td>1</td>
<td>0.963</td>
</tr>
<tr>
<td>9</td>
<td>348.668m</td>
<td>207.999m</td>
<td>25</td>
<td>1</td>
<td>0.963</td>
</tr>
<tr>
<td>10</td>
<td>46.748m</td>
<td>500.982u</td>
<td>26</td>
<td>1</td>
<td>0.963</td>
</tr>
<tr>
<td>11</td>
<td>59.5399m</td>
<td>268.889u</td>
<td>27</td>
<td>1</td>
<td>0.963</td>
</tr>
<tr>
<td>12</td>
<td>73.242m</td>
<td>272.260u</td>
<td>28</td>
<td>1</td>
<td>0.963</td>
</tr>
<tr>
<td>13</td>
<td>82.731m</td>
<td>272.570u</td>
<td>29</td>
<td>339.267m</td>
<td>200.843m</td>
</tr>
<tr>
<td>14</td>
<td>90.701m</td>
<td>265.801u</td>
<td>30</td>
<td>46.618m</td>
<td>480.469u</td>
</tr>
<tr>
<td>15</td>
<td>94.766m</td>
<td>273.596u</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

The state of the transistors for all possible combinations of input vectors for the proposed NAND gate is tabulated in Table 4.2. Thus, the introduction of LTs increases the resistance of the path from to ground. This also increases the propagation delay of the gate. To reduce this hostile effect, Dynamic Threshold MOS concept for the transistors LT makes the propagation delay equal to its conventional counter part. Hence the leakage control transistors (LTs) modified in to DTMOS offers very less leakage and reduced delay.
Table 4.2 State table of proposed two input NAND gate for 90nm process

<table>
<thead>
<tr>
<th>Transistor Label</th>
<th>Input Vector (A,B)</th>
<th>(0,0)</th>
<th>(0,1)</th>
<th>(1,0)</th>
<th>(1,1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td></td>
</tr>
<tr>
<td>LT1</td>
<td>Near Cut-Off</td>
<td>Near Cut-Off</td>
<td>Near Cut-Off</td>
<td>On</td>
<td></td>
</tr>
<tr>
<td>LT2</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Near Cut-Off</td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Near Cut-Off</td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td></td>
</tr>
</tbody>
</table>

Figure 4.4 shows a two input NAND gate implemented with the proposed method. The LTs and other logic gate devices are standard $V_{th}$ devices. The DC characteristics for a basic two input NAND gate and proposed two input NAND gate using HSPICE is shown in Figure 4.5, with input A fixed in 1 volt and input B varied from 0 to 1 volt. The exact output logic level is maintained in the proposed method without any degradation of the voltage levels. Figure 4.6 shows the transient curves obtained by HSPICE at various nodes of the DT-LECTOR based NAND gate simulated for 90nm technology at 1V supply voltage. It can be observed from the curves that the DT-LECTOR based NAND produces exact output logic levels.

**Figure 4.4** Two input NAND gate with proposed method
Figure 4.5  (a) DC characteristics for a basic two input NAND gate  
(b) DC characteristics for proposed two input NAND gate

Figure 4.6  Input-Output logic for proposed NAND gate
4.5 SIMULATION RESULTS

The similar simulation setup discussed in section 3.3.1 was used for evaluating DT-LECTOR. The experiments reported in section 3.3.5 were carried out for worst case power and delay measurements for all the cases. The following three different circuits were used for evaluating the performance of DT-LECTOR.

- Two input NAND gate
- Cascaded chain of three two input NAND circuit
- Benchmark circuits

All the circuits were implemented and simulated using BPTM 90nm process technology at 25° C. The supply voltage used was $V_{DD} = 1V$ and all the devices are of standard threshold voltage. The transistor sizing for LECTOR, Sleepy-pass gate and other techniques used for comparison are done as mentioned in section 3.3.4.

All other PMOS and NMOS transistors in PUN and PDN including DT-LECTOR are sized as width $W_P = 3.0\mu m$ for PMOS and $W_n = 1.5\mu m$ for NMOS with constant length of $L = 0.090\mu m$ (90nm). Figure 4.7 and Figure 4.8 shows the NAND gate layout with DT-LECTOR and Sleepy-pass gate techniques.
Figure 4.7 Layout for NAND gate with DT-LECTOR technique

Figure 4.8 Layout for NAND gate with Sleepy-pass gate technique
4.5.1 Results of Two Input NAND Gate

Initially a two input NAND gate was implemented and simulated in base CMOS, LECTOR, Sleepy-pass gate techniques reported in Chapter 3 and DT-LECTOR. Table 4.3 comprises the results of two input NAND gate at 90nm process technology.

From Table 4.3 the following points are inferred:

- Column 2 to 5 gives the leakage power obtained for a two input NAND gate for all the possible input combinations. This shows that the leakage power is input dependent and could be effectively reduced by forcing the minimum leakage causing input vectors during standby operation.
- Column 6 and column 7 provides the average leakage power and dynamic power obtained respectively. It is interesting to note that the DT-LECTOR and Sleepy-pass gate techniques provide considerable reduction in leakage compared to the base case value. When compared to CMOS base case, the increase in dynamic power is due to additional transistors introduced.
- The most important parameter propagation delay is listed in Column 8, which proves that DT-LECTOR gives less delay than other leakage reduction techniques. Column 9 and column 10 depicts an optimized Power Delay Product (PDP) for dynamic and static power respectively.
- Figure 4.9 and Figure 4.10 shows that dynamic power and propagation delay for DT-LECTOR are less compared to other techniques and slightly higher than base case due to additional transistors.
### Table 4.3 Power, delay and PDP for two input NAND gate

<table>
<thead>
<tr>
<th>NAND Gate Type</th>
<th>Leakage Power Dissipation (W) for Input Vector</th>
<th>Average Leakage Power (W)</th>
<th>Dynamic Power (W)</th>
<th>Delay (ps)</th>
<th>PDP_dynamic (J)</th>
<th>PDP_static (J)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(0,0)</td>
<td>(0,1)</td>
<td>(1,0)</td>
<td>(1,1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Basic CMOS</td>
<td>4.7335 E-09</td>
<td>4.1155 E-10</td>
<td>3.2691 E-10</td>
<td>1.0979 E-11</td>
<td>1.3707 E-09</td>
<td>5.7733 E-06</td>
</tr>
<tr>
<td>LECTOR</td>
<td>4.1964 E-09</td>
<td>3.5796 E-10</td>
<td>2.6498 E-10</td>
<td>0.5876 E-10</td>
<td>13.3254 E-10</td>
<td>4.9376 E-06</td>
</tr>
</tbody>
</table>
Figure 4.9 Dynamic power dissipation comparisons for two input NAND

Figure 4.10 Propagation delay comparisons for two input NAND gate
4.5.2 Results of Cascaded Chain of Three Two Input NAND Circuit

A cascaded chain of 3 two input NAND circuit was implemented and tested using 6 techniques namely CMOS base case, sleep, stack, zigzag, LECTOR and DT-LECTOR for power and delay performances. Table 4.4 gives the power and delay profile comparison for the cascaded circuit at 90nm process technology. Column 1 of Table 4.4 gives the techniques in which the cascaded structure is implemented. Column 2 shows that CMOS base case has the smallest dynamic power compared to other techniques. Column 3 gives the leakage power measured in standby mode with impressive leakage savings compared to CMOS base case. From Column 4 it is inferred that DT-LECTOR produces less delay comparable to base case than other leakage reduction techniques. Figure 4.11, 4.12 and Figure 4.13 shows the dynamic power, leakage power and propagation delay in graphical view for chain of NAND gates simulated.

Table 4.4 Power and delay Profile for cascaded chain of 3-two Input NAND circuit @ 90nm with $V_{DD} = 1$ V

<table>
<thead>
<tr>
<th>Approach</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dynamic Power (W)</td>
</tr>
<tr>
<td>Base Case</td>
<td>1.147E-05</td>
</tr>
<tr>
<td>Sleep</td>
<td>8.690E-06</td>
</tr>
<tr>
<td>Stack</td>
<td>1.280E-05</td>
</tr>
<tr>
<td>Zigzag</td>
<td>2.939E-05</td>
</tr>
<tr>
<td>LECTOR</td>
<td>1.490E-05</td>
</tr>
<tr>
<td>DT-LECTOR</td>
<td>1.261E-05</td>
</tr>
</tbody>
</table>
Figure 4.11 Dynamic power dissipation for chain of NAND gates

Figure 4.12 Leakage power dissipation for chain of NAND gates
4.5.3 Results of Benchmark Circuits

The DT-LECTOR technique is applied to various generic logic circuits to show that the DT-LECTOR technique is applicable to general logic design. We choose three benchmark circuits:

(i) D-Latch

(ii) Schmitt Trigger Slow and Fast and

(iii) Full adder

Table 4.5 gives the results for the benchmark circuits using base case, LECTOR and DT-LECTOR techniques. Since LECTOR and DT-LECTOR have similar structures, only 3 methods are considered for comparison. DT-LECTOR proves to be efficient than LECTOR and shows on an average of 51.5% of leakage savings compared with CMOS base case. Figure 4.14 shows the percentage of leakage power savings on Benchmark circuit obtained by DT-LECTOR compared to base case.
<table>
<thead>
<tr>
<th>Benchmark Circuit</th>
<th>Base Case</th>
<th>LECTOR</th>
<th>DT-LECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>D Latch</td>
<td>1.757 E-05</td>
<td>5.784 E-05</td>
<td>1.251 E-05</td>
</tr>
</tbody>
</table>

Figure 4.14 Leakage Power savings for benchmark circuits by DT-LECTOR
4.6 SUMMARY

The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. With deep-submicron and nanometer technologies, the leakage current becomes more critical in portable systems where battery life is of prime concern. This chapter presented an efficient design methodology for reducing the leakage power in CMOS circuits. Unlike other leakage control techniques, DT-LECTOR does not need any control circuitry to monitor the states of the circuit. Hence, DT-LECTOR avoids the sacrifice of obtained leakage power reduction in the form of dynamic power consumed by the additional circuitry to control the overall circuit states and area penalty.