CHAPTER 8

CONCLUSION AND FUTURE SCOPE OF THE WORK

8.1 CONCLUSION OF THE RESEARCH WORK

The experimental analyses of various architectures were proposed for the efficient implementation of lifting based DWT. The architectures are analyzed in terms of hardware and timing complexity involved with the given size of the input image and the required levels of decomposition, improving the operating speed compared to the other existing architectures.

The line based direct mapped and folded architectures for the lifting based DWT are simulated and synthesized for the given image coefficients. The simulation results show that the hardware implementation of the lifting algorithm outperforms its software counterpart. The minimum input arrival time before clock in the folded architecture is increased due to the critical path delay. The direct mapping of the input image coefficients is done for the processing element, computing the predict and update coefficients in a single clock. The folded architectures are suited for latency critical applications with improvement in hardware requirements. The architecture is further optimized by using the programmable clock gating technique for multipliers in the idle state, thereby reducing the dynamic power consumption. The latch based Clock gating is used to reduce the switching activity of multipliers in the idle state for low power implementation of the Lifting DWT.
The systolic array architecture is used to achieve high degree of parallelism, capable of handling multiple blocks of input image coefficients to implement the lifting DWT. The implemented results show that the architecture achieves a high speed with a lower accessing time, and reaches a speed performance suitable for real time low power embedded multimedia applications. The row processor consists of processing elements arranged in a systolic manner, and for column processing the lifting steps are computed concurrently, by mapping the coefficients to the same systolic arrays, by using the cyclic symmetry property of the block of input image coefficients. This improves the hardware utilization of the architecture. The advantage of the discussed architecture is that, it does not require additional memory for storing the intermediate coefficients.

The latency can be further reduced, by using the Non separable lifting DWT by combining the row and column operations. The Non-separable architecture proposed contains floating point multipliers and adders based on IEEE 754 single precision format. It is suitable for handling parallel block of 4×4 input image coefficients at each level for achieving higher speed and dynamic accuracy. The floating point multipliers and adders are implemented to give higher dynamic accuracy suitable for handling real time images. The speed is improved by combining the row-column filters with reduced memory and lifting steps. The Non separable architecture proposed achieves higher compression for images with improved performance in the quality of the displayed images suited for high speed, and low power multimedia applications.

The architectures discussed have a critical path delay of $T_m+2T_a$, where $T_m$ and $T_a$ are the computation time of multiplier and adder in the processing element respectively. The implemented results show that the architecture achieves high speed, and low power with reduced hardware
complexity, suited for real time low power embedded multimedia applications. The architectures proposed can be used to provide image/video compression and feature extraction algorithms, suited for Digital cameras, mobile phones, digital cinema etc.

8.2 FUTURE SCOPE OF THE RESEARCH WORK

The architectures proposed can be extended to multilevel 2-D DWT architectures, taking into consideration the optimization factor of reduced computing time of the lifting coefficients and hardware complexity. The architectures can be extended to varying block sizes, with overlapped scanning of the image coefficients, reducing the accessing time and memory for storing the intermediate coefficients. More details about the scheduling of row and column computation, and the necessary memory requirement can be incorporated for implementing the lifting DWT in hardware. The architectures proposed can be extended, and are scalable for the 3-Dimensional lifting DWT, suited for low power real time embedded multimedia applications.