ABSTRACT

Field effect transistors are playing an important role in the development of microelectronics and its applications. Role of MOSFETs is inevitable for powerful VLSI circuits. Smaller size, higher speed and lesser power consumption are always a demand from consumer side. Scaling down of such devices keeping other parameters unchanged is always a challenge for device scientists. Devices at nanoscale such as Double Gate (DG) MOSFET, DG Tunnel FET, FinFET and Silicon nanowire transistor (SNWT) are successfully meeting the requirement of today. Utilizing these devices at higher radio frequency is another challenge. Device has to be stable at those frequencies. The stability study of single gate MOSFET was done long back.

This thesis presents the RF stability performance of nanoscale field effect transistors. For DG MOSFET, the developed stability model provides hint for optimizing the device for better RF stability performance. The bias conditions such as gate and drain bias along with geometrical parameters such as silicon body thickness and spacer length are optimized using numerical simulation. The characteristic frequencies $f_t$ and $f_{\text{max}}$ and RF stability are studied for DG Tunnel FET. The impact of process variation such as silicon body thickness, gate oxide thickness, gate contact alignment and doping concentration on characteristic frequencies and stability of DG Tunnel FET are studied in detail. The developed RF stability model of FinFET shows how critical frequency can be achieved by varying parasitic capacitances. The bias dependency on stability of FinFET were studied and found significant in nanoscale FinFET. The geometrical parameters such as spacer length, fin height and fin thickness along gate metal work function are varied to obtain better stability performance. The stability model for SNWT is developed and the impact of silicon nanowire radius, gate contact alignment and bias conditions on RF stability performance are studied in detail. The optimized device design guidelines are provided to operate DG MOSFET, DG Tunnel FET, FinFET and SNWT for RF applications.