Chapter 4

Radio Frequency Stability Performance of Double Gate Tunnel FET

4.1 INTRODUCTION

Conventional planar metal-oxide-semiconductor field-effect transistors (MOSFETs) are approaching the scaling limit as transistor size continues to shrink. Short channel MOSFETs is facing various issues such as leakage currents and Short Channel Effects (SCEs) due to less controllability of gate over the channel (Won H.S.P, 2005). In order to have better controllability of the channel multi gate structures such as DG MOSFET, FinFET, Silicon Nanowire Transistor and DG Tunnel FET were introduced. These devices provide better performance in terms of $I_{on}/I_{off}$ ratio. In recent years, Tunnel FETs have received much attention because of its lower $I_{off}$, hence it can be used for mobile electronics applications which require low-standby-power (LSTP) operation active devices as reported by ITRS (ITRS, 2005). Tunnel FETs act as field effect transistor but use band-to-band tunneling for carrier transport. When the device is turned on, the carriers tunnel through the barrier so that current can flow from source to drain. When the device is off, the presence of the barrier keeps the off-current extremely low, hence leakage current reduces drastically. High-k gate dielectric increases the current of Tunnel FET and also added with bottom gate to double the current (Boucart K and A.M. Ionescu, 2007). Many works were carried out to study the fabrication and dc characteristics of Tunnel FET (Bjork M.T. et al, 2008, Moselund K.E et al, 2009, Moselund K.E et al, 2011). Similarly, many group worked on RF Performance of single gate SOI-MOSFET, SOI-DG MOSFET, and Silicon Nanowire FET (Eminente S et al, 2004, Sivasankaran K et al, 2012, A Cerdeira et al, 2010). The impact of process variation on RF performance of FinFET and Silicon Nanowire Transistor was also studied (Hwang C et al, 2010, R.Wang et al, 2007), but DG Tunnel FET has not received attention for the similar kind of study. In this chapter, the impact of process variation on RF and stability performance of DG Tunnel FET is investigated.
4.2 DEVICE STRUCTURE AND SIMULATION SETUP

Figure 4.1 shows the schematic structure of DG Tunnel FET of physical channel length ($L_{ch}$) of 50nm and gate oxide thickness ($t_{ox}$) of 3nm. The device has a $p^+$ source region, an intrinsic $p$-type channel region, and $n^+$ drain region with uniform doping concentration of $2 \times 10^{20}$ cm$^{-3}$, $1 \times 10^{17}$ cm$^{-3}$ and $2 \times 10^{20}$ cm$^{-3}$ respectively. A high-$k$ material ($\text{HfO}_2$) is used as gate oxide material to reduce the gate leakage current. The sources to intrinsic and intrinsic to drain junctions are considered to be abrupt. Band to Band Tunneling (BBT) Kane model with Fermi-Dirac statistics along with constant mobility and Shockley-Read-Hall recombination model used for numerical simulation (ATLAS Manual, 2012). The work function of source, drain and gate electrode is 4.17eV and gate leakage are neglected in simulations. The numerical simulation uses very fine mesh in the tunneling region so that energy band profiles are accurately determined to calculate the current in that energy range. The threshold voltage ($V_t$) and subthreshold slope for the DG Tunnel FET are obtained from dc characteristics and found to be 0.65V and 38mV/decade respectively. The small signal ac analysis is performed to obtain intrinsic and extrinsic parameters of DG Tunnel FET. The $f_{max}$, $f_t$ and stability factor are calculated using extracted parameters. The device simulations are performed using 2-D device simulator Silvaco ATLAS TCAD.

![Figure 4.1: Schematic structure of DG Tunnel FET](image-url)
4.3 SMALL SIGNAL MODELING OF DG TUNNEL FET

The small signal equivalent circuit is shown in Figure 4.2. In the circuit, $C_{gs}$ and $C_{gd}$ are intrinsic gate to source and gate to drain capacitances, $R_{gs}$ and $R_{gd}$ are gate to source and gate to drain resistances which contribute to channel distributed resistance. $C_{sdx}$ is source to drain capacitance which varies with larger drain bias on short channel devices. $g_m$ and $g_{ds}$ are transconductance and source-drain conductance respectively.

$R_{gd}C_{gd}$, $R_{gs}C_{gs}$ and the time constant $\tau$ are responsible for the time delay of the charges in the tunneling region. The effect of time constant can be formulated using non-quasi small signal model shown in Figure 4.2. The Y-parameters are extracted from the intrinsic non-quasi static small signal equivalent circuit (Tsividis Y, 1999) after neglecting extrinsic parameters and are represented as

\[
Y_{11} = \frac{j\omega C_{gs} + \omega^2 R_{gs} C_{gs}^2}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2}
\] (1)

\[
Y_{12} = \frac{-j\omega C_{gd} - \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2}
\] (2)

Figure 4.2: Small signal non-quasi static model of MOSFET (intrinsic and extrinsic part)
\[
Y_{21} = \frac{g_m - j\omega g_m \tau}{1 + \omega^2 \tau^2} - \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2}
\] (3)

\[
Y_{22} = \frac{g_{ds} + j\omega g_{ds} R_{gd} C_{gd} + j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}}
\] (4)

Using the real and imaginary parts of \( Y \) parameter, the values of device parameters can be extracted as

\[
C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega}
\] (5)

\[
C_{gs} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{12})}{\omega}
\] (6)

\[
R_{gd} = -\frac{\text{Re}Y_{12}}{\omega^2 C_{gd}^2}
\] (7)

\[
R_{gs} = \frac{1}{C_{gs}^2} \left( \frac{\text{Re}(Y_{11})}{\omega^2} - R_{gd} C_{gd}^2 \right)
\] (8)

\[
g_m = \text{Re}(Y_{21}) |\omega|^2 = 0
\] (9)

\[
g_{ds} = \text{Re}(Y_{22}) |\omega|^2 = 0
\] (10)

\[
\tau = -\frac{1}{g_m} \left( \frac{\text{Im}(Y_{21})}{\omega} + C_{gd} \right)
\] (11)

\[
C_{sdx} = \frac{\text{Im}(Y_{22})}{\omega} - C_{gd}
\] (12)

The above mentioned parameters were extracted at necessary bias conditions applied to gate and drain terminal of the device. From equation (5) - (12), the intrinsic small signal parameters were calculated using \( Y \)-parameters and the model describes the behavior of DG Tunnel FET at \( f_r \).
In order to model the RF behavior over a wide frequency range, it is necessary to calculate the intrinsic capacitances of the DG Tunnel FET. The extracted $C_{gs}$ and $C_{gd}$ are shown in Figure 4.3 as a function of gate voltage ($V_{gs}$) at 1GHz. The $C_{gd}$ is alone responsible for total gate capacitance ($C_{gg}$) as $C_{gs}$ exponentially decreases as $V_{gs}$ increases because of the presence of device potential barrier at the source side and $C_{gd}$ increases with increase in $V_{gs}$ due to reduction of the potential barrier at the drain side. Hence the contribution of $C_{gd}$ is more significant in $C_{gg}$.

The extrinsic parameters $r_g$, $r_d$ and $r_s$ can be calculated using extracted Z-parameters from the device operated at $V_{gs}=V_{ds}=0V$. The equations for the extrinsic parameters of the model are (David Lovelace et al, 1994)

\[
Re(Z_{11}) = r_g + r_s
\]

(13)

\[
Re(Z_{22}) = r_d + r_s
\]

(14)

\[
Re(Z_{12}) = Re(Z_{21}) = r_g
\]

(15)

![Figure 4.3: Extraction of $C_{gs}$ and $C_{gd}$ as a function $V_{gs}$ for $V_{ds}=1V$.](image)
4.3 RF STABILITY PERFORMANCE OF DG TUNNEL FET

The RF performance of DG Tunnel FET is evaluated by extracting $f_t$, $f_{\text{max}}$, $g_m$, $g_{ds}$ are known as Figures of Merit (FOM). It is necessary to observe response of these FOM to understand its behavior at high frequency ranges. The $f_t$, $f_{\text{max}}$ are the two parameters mainly responsible for estimating the high-frequency performance of RF device and can be defined as

$$f_t = \frac{g_m}{2\pi C_{gg}}$$  \hspace{1cm} (16)

$$f_{\text{max}} = \frac{f_t}{\sqrt{4R_g(8ds + 2\pi f_tC_{gd})}}$$  \hspace{1cm} (17)

Figure 4.4 shows extracted $f_t$ and $f_{\text{max}}$ as a function of gate voltage. The value of $f_t$ decreases when the total gate capacitance increases and this is more significant in small channel dimension of DG Tunnel FET. The $f_t$ is extracted when current gain is unity $|Y_{21}/Y_{11}| = 1$ and it is found to be 350 GHz. From Equation (16) it is observed that $f_t$ increases as transconductance increases and for DG Tunnel FET, the $f_t$ is higher because of higher transconductance. This shows the capability of DG Tunnel FET operating at higher frequencies. The $f_{\text{max}}$ is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the maximum available power gain, obtained under power-matching conditions at both the input and output ports drops to unity. The obtained $f_t$ and $f_{\text{max}}$ values of DG Tunnel FET are higher as compared to bulk MOSFET (Boucart K and A M Ionescu, 2007).

Stability of a device is determined by its stability factor ($K$), which describes the instable oscillations due to input or output impedance of the transistor. The stability parameter, $K$, gives an indication whether a device conditionally/unconditionally stable.
It must satisfy the condition $K > 1$ for a device to be unconditionally stable (Eminente S et al, 2004). The stability factor in terms of Y-parameter can be expressed as (Gonzales G, 1997)

$$K = \frac{2 \text{Re}(Y_{11}) \text{Re}(Y_{22}) - \text{Re}(Y_{12} - Y_{21})}{|Y_{12} - Y_{21}|}$$

(18)

Figure 4.5 shows the extracted stability factor over the frequency range from 1 GHz to 101 GHz and it is found that $K > 1$ from 11GHz onwards. When device is unconditionally stable from 11GHz onwards, it indicates that additional stabilization circuits are not required for RF amplifier when operating above this frequency, which reduces the circuit complexity. Hence the DG- Tunnel FET structure shown in Figure 1 can be operated in high frequency and high speed applications without oscillation. However, below 11GHz DG Tunnel FET will be conditionally stable, hence device small signal parameters can be chosen so that device will operate in stable region at a particular frequency.
4.4 IMPACT OF PROCESS VARIATION ON RF STABILITY PERFORMANCE OF DG TUNNEL FET

4.4.1 IMPACT OF BODY THICKNESS VARIATION

The silicon body thickness ($t_{si}$) becomes important when devices are fabricated on thin substrates to achieve better gate control and to reduce capacitive effects. The impact of silicon body thickness on RF performance of DG Tunnel FET is found significant. Figure 4.6 shows the fluctuation on $f_t$ and $f_{max}$ for variation in $t_{si}$ of DG Tunnel FET. The silicon thickness variation ($\Delta t_{si}$) is considered as $\pm 1\text{nm}$, $\pm 3\text{nm}$, and $\pm 5\text{nm}$ for thickness from 10nm to 25nm. The impact of $\Delta t_{si}$ at $\pm 1\text{nm}$ and $\pm 3\text{nm}$ is around 10% of $f_t$ and $f_{max}$ fluctuation ($\Delta f_t / f_t$ and $\Delta f_{max} / f_{max}$). The $f_t$ and $f_{max}$ fluctuation increases as $\Delta t_{si}$ reaches $\pm 3\text{nm}$ which is predominant for smaller $t_{si}$. At silicon body thickness of 20nm and above, the $f_t$ and $f_{max}$ fluctuations are less as compared to smaller $t_{si}$, however, as per ITRS requirements the silicon body thickness should be 7 nm in 2013 for high-performance logic (ITRS, 2009). Hence, it is suggested to keep $t_{si}$ as 15nm which is comparable to ITRS requirement and restricting $\Delta t_{si}$ within $\pm 3\text{nm}$ for better RF performance.
Figure 4.6: Impact of silicon body thickness variation on $f_i$ and $f_{max}$ of DG Tunnel FET

The critical frequency ($f_k$) for various silicon body thicknesses is shown in Figure 4.7. It is evident that for silicon body thickness of 10nm, the $f_k$ fluctuations for $\Delta t_{si}$ of $\pm$1nm, $\pm$3nm, and $\pm$5nm. The impact of $\Delta t_{si}$ is less for large silicon thicknesses. However, in order to take the advantage of double gate and to achieve stability of DG Tunnel FET at smaller frequency, it is suggested to have $t_{si}$ around 15nm and to keep $\Delta t_{si}$ within $\pm$3nm.

Figure 4.7: Impact of silicon body thickness variation when $K=1$ of DG Tunnel FET
4.4.2 IMPACT OF OXIDE THICKNESS VARIATION

The impact of gate oxide thickness variation on device performance is significant in nanoscale devices. The gate oxide provides capacitive coupling between gate and channel which control the drain current of DG Tunnel FET. The gate oxide thickness variation (Δ\text{t}_{\text{ox}}) can cause fluctuation in DG Tunnel FET dc characteristics (Boucart K et al., 2010). Figure 4.8 shows the impact of gate oxide thickness variation on \(f_t\) and \(f_{\text{max}}\) fluctuations. The \(f_t\) and \(f_{\text{max}}\) fluctuations are less than 10\% for Δ\text{t}_{\text{ox}} of ±0.2nm, however, as Δ\text{t}_{\text{ox}} increases to ±0.6nm, the fluctuation is higher because gate capacitance varies with different oxide thicknesses. The RF performance of DG Tunnel FET will not be affected if Δ\text{t}_{\text{ox}} is within ±0.2nm. Hence, it is suggested to control the process variation by better oxidation process and to keep Δ\text{t}_{\text{ox}} less than ±0.2nm.

Figure 4.9 shows the critical frequency for different \text{t}_{\text{ox}}. The \(f_k\) fluctuation for smaller oxide (at \text{t}_{\text{ox}} = 1nm) thickness is less as compared to larger oxide (at \text{t}_{\text{ox}} = 4nm) thickness for Δ\text{t}_{\text{ox}} of ±0.2nm and ±0.6nm. When \text{t}_{\text{ox}} is 1nm the DG Tunnel FET is unconditionally stable at critical frequency of 0.5 GHz, this shows the thinner gate dielectric is preferable to operate DG Tunnel FET for better stability under RF range.

![Figure 4.8: Impact of gate oxide thickness variation on \(f_t\) and \(f_{\text{max}}\) of DG Tunnel FET.](image)

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4.4.3 IMPACT OF GATE CONTACT ALIGNMENT

In DG Tunnel FET, controlling the source-intrinsic region leads to increase in device speed and reduced fringing field, this can be achieved through gate contact alignment ($L_{gca}$). Figure 4.1 shows self aligned gate structure, the top and bottom gate of DG Tunnel FET can be underlap (negative gate contact alignment) or overlap (positive gate contact alignment) on the source-intrinsic region to improve RF performance as shown in Figure 4.10. Figure 4.10 (a) shows overlap gate structure and Figure 4.10 (b) shows underlap gate structure.

![Figure 4.10: (a) Overlap (b) underlap gate contact alignment of DG Tunnel FET](image)

Figure 4.9: Impact of gate oxide thickness variation when $K=1$ of DG Tunnel FET.
Figure 4.11: Impact of gate contact alignment variation on $f_t$ and $f_{max}$ of DG Tunnel FET.

Figure 4.11 shows the impact of gate contact alignment variation ($\Delta L_{gca}$) on $f_t$ and $f_{max}$ for under-lap (negative alignment values) and overlap (positive alignment values) structures. For $\Delta L_{gca}$ of ±0.6nm, the $f_t$ and $f_{max}$ fluctuation crosses 10% and fluctuation is more for both under-lap and overlap structures as $\Delta L_{gca}$ increases. It is recommended to keep the $L_{gca}$ within 10% of channel length and $\Delta L_{gca}$ less than ±0.2nm to obtain better RF performance of DG Tunnel FET.

Figure 4.12: Impact of gate contact alignment variation when $K=1$ of DG Tunnel FET
The critical frequency is plotted for various $L_{gca}$, and shown in Figure 4.12. It is found that the K value reaches 1 at lower frequencies for gate under-lap structure as compared to gate overlap. The gate contact alignment at -10nm and -15nm shows good stability performance. But these alignments cannot provide good dc characteristics (Boucart K et al, 2010, A.Vandooren et al, 2012) and will make the fabrication process difficult. Therefore, we suggest that the optimal position for gate contact should be within 5nm for gate under-lap for better stability condition.

4.4.4 IMPACT OF DOPING CONCENTRATION

The source doping concentration ($N_D$) has the impact on the device performance since the intrinsic to source region built in potential is depend on the source doping level (Sandow C et al, 2009). The impact of source doping variation ($\Delta N_D$) on $f_t$ and $f_{max}$ is shown in Figure 4.13. At each exponential order of $N_D$ such as $1 \times 10^{17}$ cm$^{-3}$, $1 \times 10^{18}$ cm$^{-3}$, $1 \times 10^{19}$ cm$^{-3}$ and $1 \times 10^{20}$ cm$^{-3}$ the variations are considered as $\pm 0.3 \times 10^0$, $\pm 0.6 \times 10^0$ cm$^{-3}$ and $\pm 1.0 \times 10^0$ cm$^{-3}$. The drain doping concentration is assumed as $2 \times 10^{20}$ cm$^{-3}$. The $f_t$ and $f_{max}$ fluctuation crosses 10% for concentration variation of $\pm 0.6 \times 10^0$ cm$^{-3}$, hence it is suggested to follow the careful deposition mechanism for source and drain doping.

![Figure 4.13: Impact of source doping concentration variation on $f_t$ and $f_{max}$ of DG Tunnel FET](image-url)
The critical frequency is plotted for various N_D, and shown in Figure 4.14. It is found that the K value reaches 1 at lower frequencies for highly doped source as compared to lower doped source region. When N_D is higher, the DG Tunnel FET shows good stability performance if ΔN_D is within ±0.3×10^0 cm^3. Therefore, we suggest that the optimal doping concentration for source would be in the order of 1×10^{20} cm^3 and ΔN_D is within to ±0.3×10^0 cm^3 for better stability condition.

4.5 SUMMARY

The RF stability performance of DG Tunnel FET is presented using numerical simulation. The small signal parameters of device are extracted through ac analysis. The cut-off frequency and the maximum oscillation frequency obtained were found to be accurate. The results show good RF performance at 50nm channel length but the impact of process variation is also found obvious on RF Stability performance at this length. From the result we can observe that variation within ±3 nm on silicon body thickness, ±0.3 nm on oxide thickness, ±0.2 nm on gate contact alignment and ±0.3×10^0 cm^3 on doping concentration show good RF and stability performance. The optimized parameter
values to operate DG Tunnel FET under RF range are silicon body thickness of 15nm, oxide thickness of 1nm, source and drain doping in the order of $1 \times 10^{20}$ cm$^{-3}$ with gate contact alignment of 10% of channel length.