Chapter 3

Radio Frequency Stability Performance of DG MOSFET

3.1 INTRODUCTION

The downscaling of conventional MOSFETs down to sub 50nm regime lead to increase in leakage currents and short channel effects (SCEs) which causes severe problems in switching operations. In order to have better performance, DG MOSFET were proposed which has better SCEs suppression capability, higher current drive capability, lower leakage current and better scaling capability (Wong H.S.P, 2005 and Cristoloveanu Sorin et al, 2003). In recent years, DG MOSFETs have become popular for analog and RF applications due to the volume inversion effect at low gate bias (Abhinav Kranti, 2005 and J.Liang et al, 2008). The impact of structural parameter fluctuation on RF performance of DG MOSFET was studied and device design guidelines are reported by Liang J et al, (2008). The impact of gate engineering and channel engineering on RF performance of DG MOSFET were studied by Mohankumar N et al, 2010 and they have shown that dual material (DM) work function for the gate has better RF performance as compared to halo-doped channel DG MOSFET. Similarly, Angusuman Sarkar et al, (2012) studied the effect of triple-material (TM) with three different work functions double gate SOI DG MOSFET on RF performance characteristics. Recently, the graded channel (GC) technology, gate stack engineering (GS), DM work function gate and the combinations of these technologies i.e., GCGSDG and GSDMDG were studied for analog and RF performance (Rupendra Kumar Sharma et al, 2011). The optimized DG MOSFET design using DM and GC requires additional effort in processing steps like metal wet etch process, metal inter diffusion process, and selective implantation for maintaining dual work function for DM devices. Selective tilted ion implantation is required for GC devices. However, the studies on the RF stability performance of DG MOSFET have not received attention which is one of the important parameters for Radio Frequency Integrated Circuit (RFIC) design. This chapter presents stability model and detailed study on bias and geometry optimization procedure for RF stability performance of DG MOSFET.
3.2 DEVICE STRUCTURE AND SIMULATION SETUP

Figure 3.1 shows cross sectional view of symmetric DG MOSFET of physical channel length ($L_{ch}$) of 22 nm and gate oxide thickness ($t_{ox}$) of 1.6nm as per ITRS (ITRS, 2005). DG MOSFET has n$^+$ source and drain with doping concentration of 2×10$^{20}$ cm$^{-3}$ and channel doping of 10$^{15}$ cm$^{-3}$. Si$_3$N$_4$ is used as spacer material for mechanical strength to gate and protects source and drain region from fringing field. HfO$_2$ is used as gate dielectric which reduces gate tunneling leakage current and the gate electrodes work function is considered as 4.15eV. Electric field dependent carrier mobility with velocity saturation, band gap narrowing, Lombardi Constant Voltage and Temperature (CVT) along with concentration dependent mobility model were activated for simulation. Fermi-Dirac statistics, Shockley Read Hall and auger recombination for minority carrier recombination are used along with density gradient quantum correction model for inversion layer quantum effects for simulation (Atlas User Manual, 2012). The ac characteristics are performed to extract two port Y and Z parameters. The extracted parasitic resistances and capacitances from device simulation are used to calculate the $f_t$ and $f_{max}$ of DG MOSFET. The device simulations are performed using Silvaco ATLAS Device Simulator.

Figure 3.1: Cross-sectional view of symmetric DG MOSFET
3.3 STABILITY MODELING

DG MOSFETs are said to be unconditionally stable at any operating frequency above critical frequency \( f_k \). The \( f_k \) is obtained as frequency at which stability factor \( K=1 \). The device will not oscillate independently from any passive termination network at the transistor’s input and output when it is unconditionally stable (Schwierz F and Liou J J, 2001). However, operating frequencies below \( f_k \), the transistor is said to be conditionally stable and certain termination conditions can cause oscillations. Hence, device must satisfy the condition \( K > 1 \) to be unconditionally stable (Gonzales G, 1997). The stability factor is calculated using Y-parameters at different frequencies of operation for the DG MOSFET. The stability factor in terms of Y-parameter can be expressed as (Rollet J M, 1962)

\[
K \approx \frac{2 \text{Re}(Y_{11} \text{Re}(Y_{22}) - \text{Re}(Y_{12} Y_{21}))}{|Y_{12} Y_{21}|} \quad (1)
\]

The symmetric DG MOSFET has three terminals, source, drain and gate. Here both the gates are tied to form a single gate terminal. The Y-parameters are considered with intrinsic small signal parameters of symmetric DG MOSFETs as (Cho, S et al, 2011).

\[
Y_{11} \approx \omega^2 R_{gd} C_{gd}^2 + j \omega (C_{gs} + C_{gd}) \quad (2)
\]

\[
Y_{12} \approx -\omega^2 R_{gd} C_{gd}^2 + j \omega C_{gd} \quad (3)
\]

\[
Y_{21} \approx g_m - \omega^2 R_{gd} C_{gd}^2 - j \omega (C_{gd} + \tau g_m) \quad (4)
\]

\[
Y_{22} \approx g_{ds} + \omega^2 R_{gd} C_{gd}^2 + j \omega C_{gd} \quad (5)
\]

These Y parameters can be used in Equation (1) to simplify further as
\[
K = \frac{\omega (R_{gs} g_{ds} C_{gs}^2 + 2 R_{gd} g_m C_{gg} C_{gd} + C_{gg}^2)}{C_{gd} \sqrt{2 \omega^2 g_m C_{gg}^2 + g_m^2}}
\]  

(6)

where \( C_{gs} \) is total gate-to-source, \( C_{gd} \) is total gate-to-drain and \( C_{gg} \) is total gate capacitance (\( C_{gg} = C_{gs} + C_{gd} \)), \( g_m \) is transconductance, \( g_{ds} \) is drain to source conductance, \( R_{gs} \) is gate-to-source resistance and \( R_{gd} \) is gate-to-drain resistance.

The Equation (6) is extended to obtain \( f_k \) by substituting \( K=1 \) and by making approximation \( \omega^4 R_{gd}^2 C_{gd}^4 \ll 1 \), \( \omega^4 R_{gs}^2 C_{gs}^4 \ll 1 \) and \( \omega^2 \tau_m^2 \ll 1 \)

\[
f_k = \frac{f_t N}{\sqrt{g_{ds} g_m R_{gs} M^2 + N M (g_m R_{gd} + 1)}}
\]  

(7)

where \( M = \frac{C_{gs}}{C_{gg}} \), \( N = \frac{C_{gd}}{C_{gg}} \) and \( f_t = \frac{g_m}{2 \pi C_{gg}} \)

The total \( C_{gs} \) and \( C_{gd} \) without considering overlap capacitance and external fringing capacitance can be calculated as (Angsuman Sarkar, 2012)

\[
C_{gs} = C_{gsi} + C_{fint}
\]  

(8)

\[
C_{gd} = C_{gdi} + C_{fint}
\]  

(9)

\[
C_{fint} = \left[ \frac{W_{sl}}{3 \pi} \ln \left( 1 + \frac{t_{si}}{2 t_{ox}} \sin \left( \frac{\pi \varepsilon_{ox}}{2 \varepsilon_{si}} \right) \right) \right] \times e^{-((V_{gs}-V_{FB}-2\phi_f-V_{ds})/(3/2)\phi_f)^2}
\]  

(10)

where \( \varepsilon_{si} \) and \( \varepsilon_{ox} \) are dielectric constant of silicon and oxide. \( W \), \( t_{si} \), and \( t_{ox} \) are the width, thickness of silicon body and gate oxide thickness respectively. \( V_{FB} \) and \( \phi_f \) are the flat band voltage and Fermi potential respectively. Equation (7) describes the relation between \( f_k \), intrinsic small signal parameters and \( f_t \) which also gives hint for optimization.

It is clear from Equation (7) that M and N values can be adjusted to reduce \( f_k \) without \( f_t \).
degradation. But N is almost independent parameter on stability model with respect to \( f_t \).
The optimization begins with the study of factors related to M and N, especially \( C_{gs} \), \( C_{gd} \)
and \( C_{gg} \). Equation (8)-(10) shows the bias and geometry dependence on \( C_{gs} \) and \( C_{gd} \)
of DG MOSFET. By adjusting the applied gate and drain bias and geometrical parameters
such as \( t_{si} \) and spacer length \( (L_{spac}) \), the DG MOSFET can be optimized for better stability
performance.

3.4  BIAS OPTIMIZATION OF DG MOSFET FOR RF STABILITY

3.4.1  OPTIMIZATION OF GATE TO SOURCE VOLTAGE

The stability factor is calculated from extracted Y-parameters for various applied
gate bias \( (V_{gs}) \) with drain bias \( (V_{ds}) \) of 0.8V which are shown in Figure 3.2. It is evident
from Figure 3.2, the DG MOSFET attains unconditionally stable condition at earlier
frequency for higher \( V_{gs} \). Further increase in gate voltage leads to increase in total gate to
source and gate to drain parasitic capacitances. Also \( f_t \) decreases due to \( g_m \) because of
mobility degradation at higher gate bias. Equation (7) shows the dependency of \( f_t \) and
parasitic capacitance on \( f_k \).

![Figure 3.2: Extracted stability factor for different \( V_{gs} \) at \( V_{ds}=0.8V \)](image)

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3.4.2 OPTIMIZATION OF DRAIN TO SOURCE VOLTAGE

Figure 3.3 shows the extracted stability factor for various $V_{ds}$ at $V_{gs} = 1.2V$. As $V_{ds}$ increases the stability performance degrades due to degradation in $C_{gd}$ and also at higher $V_{ds}$ Drain Induced Barrier Lowering (DIBL) affects the device performance. Hence smaller drain bias is preferred to operate the DG MOSFET in RF range.

Figure 3.4: Critical frequency as a function of gate voltage

![Figure 3.4: Critical frequency as a function of gate voltage](image-url)
Figure 3.4 shows the critical frequency \(f_k\) as a function of gate voltage \(V_{gs}\). The \(f_k\) reduces with increase in gate bias and further reduce with smaller applied \(V_{ds}\). This shows that at smaller drain bias and higher gate bias, DG MOSFET exhibits better RF stability performance.

3.5 GEOMETRY OPTIMIZATION OF DG MOSFET FOR RF STABILITY

3.5.1 OPTIMIZATION OF GATE SPACER LENGTH

The spacer length \(L_{spac}\) has a significant impact on RF stability performance of DG MOSFET. Figure 3.5 shows the extracted stability factor and \(C_{gd}\) for different spacer lengths. The fringing capacitance increases with thinner \(L_{spac}\) which causes oscillation at higher frequency. The variation of \(L_{spac}\) causes both extrinsic parasitic resistance and fringing capacitance both in source and drain regions. The transconductance decreases with increase in \(L_{spac}\) which leads to degradation in \(f_t\). The DG MOSFET becomes stable at \(f_k = 4\) GHz for \(L_{spac}\) of 20nm as \(C_{gd}\) decreases with \(L_{spac}\). Further increase in \(L_{spac}\) does not effect the stability because \(C_{gd}\) saturates at larger \(L_{spac}\).

![Figure 3.5: Extracted stability factor and \(C_{gd}\) for different spacer length.](image-url)
Equation (7) shows the relation between $f_k$ and small signal parameter which gives us guideline for optimizing suitable value of spacer length without affecting device performance.

3.5.2 OPTIMIZATION OF SILICON BODY THICKNESS

The silicon body thickness also has a significant impact on RF Performance of DG MOSFET. Figure 3.6 shows the extracted stability factor and $C_{gd}$ for various silicon body thicknesses ($t_{si}$). It is evident that for thinner $t_{si}$, the stability reaches at earlier frequency as compared to thicker $t_{si}$, since $C_{gd}$ decreases with thinner $t_{si}$. However, $t_{si}$ cannot be reduced further because it leads to increase in device oscillation at higher frequency. The parasitic source and drain resistances increase with thinner $t_{si}$ which also increases the SCEs. The optimized $t_{si}$ for better RF stability is 10nm which is comparable to ITRS requirement (ITRS, 2005) for ultra thin silicon body thickness. The silicon body thickness to gate length ratio ($t_{si}/L_g$) is chosen as 0.45 to improve stability performance.

![Figure 3.6: Extracted stability factor and $C_{gd}$ for different silicon body thicknesses.](image-url)
Equation (7) – (10) show the impact of $t_{si}$ on capacitance through fringing capacitance which provides design guidelines for optimized value of silicon body thickness to operate DG MOSFET at RF range with improved stability performance.

3.6 OPTIMIZED DOUBLE GATE MOSFET FOR RF STABILITY

We have optimized the value of $t_{si}$, $t_{ox}$, $L_{spac}$ in the previous section and found that DG MOSFETs exhibit better stability performance at $t_{si}$=10nm, $t_{ox}$=1.6nm and $L_{spac}$=20nm. Figure 3.7 shows the extracted stability factor for the optimized structure. It is evident that $K$ reaches to 1 at 7.5 GHz which shows that the device can be operated unconditionally stable. This indicates that DG MOSFET does not require additional stabilization circuit when operated from 7.5 GHz onwards in RFICs. However, at below $f_k$, DG MOSFETs are potentially or conditionally stable. A suitable device parameter can be chosen to make the device to be stable at a particular frequency.

![Figure 3.7: Extracted stability factor for optimized DG MOSFET at $V_{gs}$=1.2V and $V_{ds}$= 0.8V.](image)

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The characteristic frequencies $f_t$ and $f_{\text{max}}$ provide information to device engineers about the capability of DG MOSFETs operating at RF range. The cut-off frequency $f_t$ is evaluated as the frequency for which the magnitude of short circuit gain drops to unity. The $f_t$ is expressed as

$$f_t = \frac{g_m}{2\pi C_{gg}}$$

$f_{\text{max}}$ is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the maximum available power gain drops to unity. It is expressed as

$$f_{\text{max}} = \frac{f_t}{\sqrt{4(R_c+R_g+R_l)(g_{ds}+2\pi f_tC_{gd})}}$$

Figure 3.8 shows the variation of $f_t$ and $f_{\text{max}}$ with drain current for the optimized DG MOSFET. The bias and geometry optimized structure has $f_t$ of 520GHz due to the improved $g_m$ and $f_{\text{max}}$ of 700GHz, which shows that the proposed DG MOSFET structure is suitable for high speed switching and high frequency applications.

Figure 3.8: Variation of $f_t$ and $f_{\text{max}}$ with drain current for optimized DG MOSFET at $V_{gs}=1.2V$ and $V_{ds}=0.8V$. 

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3.7 SUMMARY

The RF Stability model is developed for DG MOSFET and its stability characteristics are analyzed using numerical simulation. The device stability is studied for various bias and geometry conditions, and observed that $C_{gd}$ and $C_{gs}$ are responsible for degradation in $f_k$. The proposed optimized geometry and bias condition show excellent stability performance. There is no additional circuit required as the device is unconditionally stable from 7.5 GHz onwards.