2.1 FIGURE OF MERIT OF RF TRANSISTORS

RF transistors are active devices capable of amplify signals at RF frequency range. The RF transistors can operate as low-noise and power amplifiers, mixers, oscillators, frequency converters, etc. RF transistors in general can be divided into two groups: small-signal low-noise transistors and power transistors. For low-noise transistors, low noise and high operating frequency are desired, while power transistors are designed for high output power at high operating frequency.

The capabilities and performance of RF transistors can be assessed through Figures of Merit (FOM). It is the number or quantity which provides information to device designers for evaluating the device performance and to compare the advantage of different types of transistors. In this section we have presented some of RF FOM

a. Stability

RF Transistors are said to be unconditionally stable at any operating frequency above the critical frequency ($f_c$). The $f_c$ is obtained as the frequency at which stability factor, $K=1$. The device will not oscillate independently from any passive termination network at the transistor’s input and output when it is unconditionally stable. However, operating frequencies below $f_c$, the transistor is said to be conditionally stable and certain termination conditions can cause oscillations. The stability behavior of transistor can be described by the stability factor $K$ as introduced by (Rollett J.M, 1962)

$$K = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}$$  (1)
where $Y_{11}$, $Y_{12}$, $Y_{21}$, $Y_{22}$ are frequency dependent Y parameters of the transistor and ‘Re’ denotes the real part. If $K > 1$, the transistor is unconditionally stable, and for $K < 1$, it works in the region of conditional stability where unintended oscillations may occur.

b. Cut off frequency ($f_t$)

$f_t$ is defined as the cut off frequency at which small signal current gain drops to unity $|Y_{21}/Y_{11}| = 1$. It is a measure of the maximum useful frequency of a transistor when it is used as an amplifier. $f_t$ can be easily obtained by

\[
f_t = \frac{g_m}{2\pi c_{gg}} \tag{2}\]

c. Maximum Oscillation Frequency ($f_{max}$)

The $f_{max}$ is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the unilateral power gain drops to unity. The $f_{max}$ is expressed as

\[
f_{max} = \frac{f_t}{2\sqrt{g_{ds}(R_g+R_c)+2\pi f_t R_g c_{gd}}} \tag{3}\]

Unilateral Gain = \[\frac{1|\begin{vmatrix} S_{21} \\ S_{12} \end{vmatrix}|^2}{K|\begin{vmatrix} S_{21} \\ S_{12} \end{vmatrix} - \text{Re}(\begin{vmatrix} S_{21} \\ S_{12} \end{vmatrix})|} \tag{4}\]
2.2 THEORY OF RF STABILITY FACTOR

2.2.1 STABILITY

Figure 2.1 shows that oscillation is possible if either input or output port impedance has a negative real part; this would then imply that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, where $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are the input and output reflection co-efficient. Because $|\Gamma_{in}|$ and $|\Gamma_{out}|$ depend on the source and load matching networks, the stability of the amplifier depends on $\Gamma_S$ and $\Gamma_L$ (source and load reflection co-efficient) as presented by the matching networks. Thus, we can define two types of stability:

1. **Unconditional stability**: The network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive sources and load impedances (i.e., $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).

2. **Conditional stability**: The network is conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

The stability condition of an amplifier circuit is usually frequency dependent, since the input and output matching networks generally depend on frequency. Thus it is possible for an amplifier to be stable at its design frequency, but unstable at other frequencies. Hence, the amplifier designer should consider this.

![General transistor amplifier circuits](image)

Figure 2.1: General transistor amplifier circuits
The discussion of stability is limited to two-port amplifier circuits of the type shown in Figure 2.1, where the S parameters of the active device can be measured without oscillations over the frequency band of interest. The rigorous general treatment of stability requires that the network S parameters (or other network parameters) have no poles in the right-half complex frequency plane, in addition to the conditions that $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ (Ohtomo M, 1995). These conditions are difficult assessment in practice, but for the case considered here, the S parameters are known to be pole-free. Hence the following stability conditions are adequate.

### 2.2.2 STABILITY CIRCLES

The following conditions are to be satisfied by $\Gamma_S$ and $\Gamma_L$ if the amplifier is unconditionally stable

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1,$$  \hspace{1cm} (5)

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{22}\Gamma_S} \right| < 1,$$  \hspace{1cm} (6)

where  \hspace{1cm} $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$,  \hspace{1cm} $\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}$

If the device is unilateral ($S_{12}= 0$), this condition on Equation (5) and (6) reduce to the simple results showing that $|S_{11}| < 1$ and $|S_{22}| < 1$ are sufficient for unconditional stability. Otherwise, the inequalities of Equation (5) and (6) define a range of values for $\Gamma_L$ and $\Gamma_S$ where the amplifier will be stable. Finding this range for $\Gamma_L$ and $\Gamma_S$ can be facilitated by using Smith chart, and plotting the input and output stability circles. The stability circles are defined as the loci in the $\Gamma_L$ (or $\Gamma_S$) plane for which $\Gamma_{in} =1$ (or $\Gamma_{out} =1$). The stability circles then define the boundaries between stable and potentially unstable regions of $\Gamma_L$ and $\Gamma_S$. $\Gamma_L$ and $\Gamma_S$ must lie on the Smith chart ($|\Gamma_S| < 1$, $|\Gamma_L| < 1$ for passive matching networks).
We can derive the equation for output stability circle as follows. First let us use Equation (5) to express the condition, $\Gamma_{in} = 1$ as

$$\left| S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1-S_{22} \Gamma_L} \right| = 1,$$

or

$$\left| S_{11} (1 - S_{22} \Gamma_L) + S_{12} S_{21} \Gamma_L \right| = |1 - S_{22} \Gamma_L|$$

Now the determinant of the scattering matrix, $\Delta$ is defined as

$$\Delta = S_{11} S_{22} - S_{12} S_{21}$$

Then we can write the above results as

$$\left| S_{11} - \Delta \Gamma_L \right| = \left| 1 - S_{22} \Gamma_L \right|$$

Squaring both sides and simplifies

$$|S_{11}|^2 + |\Delta|^2 |\Gamma_L|^2 - (\Delta \Gamma_L S_{11}^* + \Delta^* \Gamma_L^* S_{11}) = 1 + |S_{22}|^2 |\Gamma_L|^2 - (S_{22}^* \Gamma_L^* + S_{22} \Gamma_L)$$

$$(|S_{22}|^2 - |\Delta|^2) \Delta \Gamma_L \Gamma_L^* - (S_{22} - \Delta S_{11}^*) \Gamma_L - (S_{22}^* - \Delta S_{11}) \Gamma_L^* = |S_{11}|^2 - 1$$

$$\Gamma_L \Gamma_L^* - \frac{(S_{22} - \Delta S_{11}^*) \Gamma_L^*}{|S_{22}|^2 - |\Delta|^2} = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2}$$

Next, completing the square by adding $|S_{22} - \Delta S_{11}^*|^2 / (|S_{22}|^2 - |\Delta|^2)$ to both sides

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)}{|S_{22}|^2 - |\Delta|^2} \right|^2 = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2} + \frac{|S_{22} - \Delta S_{11}^*|^2}{(|S_{22}|^2 - |\Delta|^2)^2},$$

or

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)}{|S_{22}|^2 - |\Delta|^2} \right| = \frac{|S_{12} S_{21}|}{|S_{22}|^2 - |\Delta|^2}$$

(11)
In the complex $\Gamma$ plane, an equation of the form $|\Gamma - C| = R$ represents a circle with center at $C$ (a complex number) and a radius $R$ (a real number). Thus, Equation (11) defines the output stability circle with a center $C_L$ and radius $R_L$, where

$$C_L = \frac{(S_{22} - \Delta S_{11})^*}{|S_{22}|^2 - |\Delta|^2} \quad \text{(center),}$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad \text{(radius),}$$

(12)

(13)

Similar results can be obtained for the input stability circle by interchanging $S_{11}$ and $S_{22}$

$$C_S = \frac{(S_{11} - \Delta S_{22})^*}{|S_{11}|^2 - |\Delta|^2} \quad \text{(center),}$$

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|, \quad \text{(radius),}$$

(14)

(15)

From the $S$ parameters of the transistor, we can plot the input and output stability circles where $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$. On one side of the input stability circle we will have $|\Gamma_{out}| < 1$, while on the other side we will have $|\Gamma_{out}| > 1$. Similarly, we will have $|\Gamma_{in}| > 1$ on one side of the output stability circle, and $|\Gamma_{in}| > 1$ on the other side. So we now need to determine the areas on the Smith chart which represent the stable region, for which $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$.

The output stability circles plotted for unconditionally stable device are shown in Figure 2.2 for $|S_{11}| < 1$ and $|S_{11}| > 1$. If we set $Z_L = Z_0$, then $\Gamma_L = 0$ and Figure 2.2 (a) shows that $|\Gamma_{in}| = |S_{11}|$. Now if $|S_{11}| < 1$, then $|\Gamma_{in}| < 1$, so $\Gamma_L = 0$ must be in a stable region. This means that the center of the Smith chart ($\Gamma_L = 0$) is in the stable region, so all of the Smith chart ($|\Gamma_L| < 1$) that is exterior to the stability circle defines the stable range for $\Gamma_L$. 

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Figure 2.2: Output Stability for unconditionally stable device (a) $|S_{11}| < 1$ (b) $|S_{11}| > 1$

This region is shaded in Figure 2.2 (a). Alternatively, if we set $Z_L = Z_0$ but have $|S_{11}| > 1$, then $|\Gamma_{in}| > 1$ for $\Gamma_L = 0$ and the center of the Smith chart must be in an unstable region. In this case the stable region is the inside region of the stability circle that intersects the Smith chart, as illustrated in Figure 2.2(b). Similar results can be applied to the input stability circle.

If the device is unconditionally stable, the stability circles must be in completely outside (or totally enclose) the Smith chart. We can state this result mathematically as

$$||C_L|-R_L| > 1, \quad \text{for } |S_{11}| < 1,$$  \hspace{1cm} (16)

$$||C_S|-R_S| > 1, \quad \text{for } |S_{22}| < 1,$$  \hspace{1cm} (17)

If $|S_{11}| > 1$ or $|S_{22}| > 1$, the amplifier cannot be unconditionally stable because we can always have a source or load impedance of $Z_0$ leading to $\Gamma_S = 0$ or $\Gamma_L = 0$, thus causing
| \Gamma_{\text{in}} | > 1 \text{ or } | \Gamma_{\text{out}} | > 1. \text{ If the device is only conditionally stable, operating points for } \Gamma_S \text{ and } \Gamma_L \text{ must be chosen in stable regions, and it is good practice to check the stability at several frequencies near the design frequency. If it is possible to accept a design with less than maximum gain, a transistor can usually be made to be unconditionally stable by using resistive loading.}

2.2.3 TESTS FOR UNCONDITIONAL STABILITY

The stability circles discussed above can be used to determine regions for \( \Gamma_S \) and \( \Gamma_L \), where the amplifier circuit will be conditionally stable, but simpler tests can be used to determine unconditional stability. One of these is the \( K - \Delta \) test, where it can be shown that a device will be unconditionally stable if Rollet's condition, defined as

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1
\]

(18)

along with the auxiliary condition that

\[
|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1
\]

(19)

are simultaneously satisfied. These two conditions are necessary and sufficient for unconditional stability, and can easily be evaluated. If the S parameters do not satisfy the \( K - \Delta \) test, the device is not unconditionally stable, and stability circles must be used to determine if there are values of \( \Gamma_S \) and \( \Gamma_L \) for which the device will be conditionally stable. Also, recall that we must have \( |S_{11}| < 1 \) and \( |S_{22}| < 1 \) if the device is to be unconditionally stable.

While the \( K - \Delta \) test of Equation (18) and (19) is a mathematically rigorous condition for unconditional stability, it cannot be used to compare the relative stability of two or more devices since it involves constraints on two separate parameters. However, a
new criterion has been proposed (Marion Lee Edwards, 1992) that combines the \( S \) parameters in a test involving only a single parameter, \( \mu \), defined as

\[
\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}| + |S_{12} S_{21}|} > 1
\]

(20)

Thus, if \( \mu > 1 \), the device is unconditionally stable. In addition, it can be said that larger values of \( \mu \) imply greater stability.

The \( K - \Delta \) test of Equation (18) - (19) can be derived from a similar starting point, or more simply from the \( \mu \)-test of (20). Rearranging (20) and squaring gives

\[
|S_{22} - \Delta S_{11}|^2 < (1 - |S_{11}|^2 - |S_{12} S_{21}|)^2
\]

(21)

It can be verified by direct expansion that

\[
|S_{22} - \Delta S_{11}|^2 = |S_{12} S_{21}|^2 + (1 - |S_{11}|^2)(|S_{22}|^2 - |\Delta|^2),
\]

so Equation (21) can be expanded to

\[
|S_{12} S_{21}|^2 + (1 - |S_{11}|^2)(|S_{22}|^2 - |\Delta|^2) < (1 - |S_{11}|^2)(1 - |S_{11}|^2 - 2|S_{12} S_{21}|) + |S_{12} S_{21}|^2.
\]

can be simplified as

\[
|S_{22}|^2 - |\Delta|^2 < 1 - |S_{11}|^2 - 2|S_{12} S_{21}|,
\]

which yields Rollet's condition of (18), after rearranging

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} S_{21}|} > 1.
\]

In addition to Equation (18), the \( K - \Delta \) test also requires an auxiliary condition to guarantee unconditional stability. Although we derived Rollet's condition from the necessary and sufficient result of the \( \mu \)-test, the squaring step used in Equation (21)
introduces an ambiguity in the sign of the right-hand side, which requires an additional condition. This can be derived by considering that the right-hand side of Equation (21) must be positive before squaring. Thus,

$$|S_{12}S_{21}| < 1 - |S_{11}|^2.$$  

Because similar conditions can be derived for the input side of the circuit, we can interchange $S_{11}$ and $S_{22}$ to obtain the analogous condition

$$|S_{12}S_{21}| < 1 - |S_{22}|^2.$$  

Adding these two inequalities

$$2|S_{12}S_{21}| < 2 - |S_{11}|^2 - |S_{22}|^2.$$  

From the triangle inequality we know that

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \leq 1 - |S_{11}S_{22}| + |S_{12}S_{21}|,$$

so we can write

$$|\Delta| < |S_{11}| |S_{22}| + 1 - \frac{1}{2} |S_{11}|^2 - \frac{1}{2} |S_{22}|^2 < 1 - \frac{1}{2} (|S_{11}|^2 - |S_{22}|^2) < 1,$$

which is identical to Equation (19).
2.3 DESIGN CHALLENGES OF FET DEVICES FOR RF APPLICATIONS

The downscaling of transistor is possible with modifications in device dimension, material-oriented and structural changes which improves DC performance but degrades RF performances of device. Hence, there is a need to analyze the device parameters which can cause fluctuation on the device RF characteristics. These are very useful in device design for RF applications. For small channel devices the parasitic capacitance and resistance become important as they can degrade the device RF performance. The source and drain region and its extension regions of nanoscale devices should be carefully designed for RF applications. In this section, conventional MOSFET and multi-gate FETs design challenges are presented for RF applications.

2.3.1 SINGLE GATE MOSFET

Kilchystka V et al, (2003) investigated the effect of various process options on RF performance of Fully Depleted (FD) Silicon-on-Insulator (SOI), Partially Depleted (PD) SOI and bulk MOSFET as shown in Figure 2.3. Figure 2.4 shows transition frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) for different bias conditions of silicided FD and PD SOI MOSFET composed of 12-Parallel connected gate fingers of 0.26µm effective channel length and 6.6 µm width each. The $f_T$ increases with increase in $g_m$ and reduced $g_d$ in FD MOSFET.

![Diagram of MOSFETs](image)

Figure 2.3: Schematic view of (a) Bulk MOSFET (b) FD SOI MOSFET (c) PD SOI MOSFET
Figure 2.4: $f_T$ and $f_{\text{max}}$ for different bias conditions of silicided FD and PD SOI MOSFET

Figure 2.5 represents evolution of $f_T$ and $f_{\text{max}}$ for different channel lengths of various silicided SOI nMOSFET having a total gate width of 80 µm and biased at $V_{gs}=V_{ds}=0.9V$. $f_t$ increases with reduction of channel length. $g_m$ being proportional to $W/L$ and $(C_{gs}+C_{gd})$ to $W \times L$. $f_t$ is function of $1/L^2$, $f_{\text{max}}$ also presents $1/L^2$ dependence for larger channel length but rising rate decreases for L smaller than 0.5 µm because $R_g$, $g_d$ and $C_{gd}$ increases with reduction of channel length (L) become dominant.

Figure 2.5: $f_T$ and $f_{\text{max}}$ for different channel length for silicided FD (solid line) and PD (dashed line) SOI nMOSFETs.
A. Kranti et al, (2010) analyzed the potential of underlap S/D channel architecture to improve analog/RF performance metrics of sub 100nm Ultra Thin Body BOX (UTBB) SOI MOSFETs. Figure 2.6 shows dependence of \( f_T \) on drain current for various \( L_g \) UTBB devices. Scaling down of \( L_g \) leads to improvement in peak \( f_T \) and current level corresponding to peak \( f_T \) is around 300\( \mu \)A/\( \mu \)m for all devices.

Figure 2.7 shows that well scaled underlap UTBB design with film thickness (\( T_{si} \)) value of \( L_g /5 \) achieve intrinsic voltage gain values within range 20-26dB and \( g_m/I_{ds} \) of 12-13V-1 over entire \( L_g \) range (85-30nm) along with expected enhancement in \( f_T \) with \( L_g \) downscaling.
2.3.2 MULTIPLE GATE MOSFET

The impact of structural parameters such as silicon body thickness ($t_{si}$), lateral spacer length ($L_{spacer}$) and elevated height of source / drain ($H_{raise}$) on RF performance of DG MOSFET shown in Figure 2.8 are reported by Liang J et al., (2008). The parasitic source and drain resistance decreases with increase in silicon body thickness, transconductance ($g_m$) also increases with increase in $t_{si}$. The gate capacitance varies with variation in silicon body thickness and thus larger $t_{si}$ exhibits higher $f_t$. As $t_{si}$ increases, the parasitic source/drain resistance reduces which results in increase in transconductance and output conductance. Hence, $f_{max}$ decreases with increase in $t_{si}$ as $C_{gd}$ increases. The variation of spacer length effects on both the parasitic resistance and fringing capacitance in source/drain extension region and has significant impact on $f_t$ and $f_{max}$. Any small variation on $L_{spacer}$ has impact on $f_t$ as $g_m$ and $C_{gg}$ varies with $L_{spacer}$. As spacer length decreases $f_t$ saturates due to increase in fringing capacitance. $f_{max}$ is mainly determined by $g_m$, $g_{ds}$, $C_{gd}$ and parasitic resistance, as $L_{spacer}$ decreases $g_m$ decreases and $f_{max}$ increases as the both $g_m$ and $g_{ds}$ increase, whereas access resistance reduces. $C_{gd}$ in the saturation region is mostly determined by the outer fringing capacitance, which is approximately exponential to $L_{spacer}$. Hence optimizing $L_{spacer}$ and $H_{raise}$ will improve both $f_t$ and $f_{max}$ of DG MOSFET.

Figure 2.8: Cross-sectional view of the double gate MOSFET.
The impact of parasitic components such as capacitances and source/drain resistances along with fin structural parameters on RF Performance of FinFET shown in Figure 2.9 are reported by Abhinav Kranti et al., (2008). The fin structural parameters such as aspect ratio (AR), fin width ($T_{\text{fin}}$), fin height ($H_{\text{fin}}$) and fin spacing ($S_{\text{fin}}$) are adjusted to obtain improved RF performance. The AR is defined as the ratio of fin height to fin width and technologically its value limited to 5 (Wen Shiang Liao et al., 2005). The smaller $T_{\text{fin}}$ shows significant reduction in $C_{gg}$ with increase in AR and decrease in $S_{\text{fin}}$. FinFET designed with lower AR and wider fins achieve higher $f_t$ values as compared to narrow fin devices. But $f_{\text{max}}$ degrades due to higher $C_{gd}$ and $g_{ds}$. Hence, FinFET designed with AR less than 3 along with thicker $T_{\text{fin}}$ and low $S_{\text{fin}}$ exhibit better $f_t$ and $f_{\text{max}}$. Another limiting parameter for RF performance of FinFET is parasitic Source / Drain resistance and can be optimized by AR, $T_{\text{fin}}$, $S_{\text{fin}}$. Similarly $f_{\text{max}}$ improves with increase in $f_t$ and reduction in gate and drain contact resistances.

The parasitic elements are analyzed in terms of gate height ($H_g$), the contact resistance ($R_{sd}$), SDE region length $L_{ex}$ and nanowire diameter ($d_w$) of SNWT shown in Figure 2.10 for RF applications (Jing Zhuge et al, 2008). The fringing capacitances are important component of parasitic capacitance in nanowire structures. The outer fringing capacitance is larger than intrinsic capacitance as $H_g/L_g$ is greater than 2. In SNWT, the contact resistance and resistance of ultra narrow Source Drain Extension (SDE) region are the parasitic resistances.
The parasitic resistance of single nanowire ranges from 0 to 2000\(\Omega\). Generally, SNWT are designed with several fingers which reduce contact resistance on each SNWT due to shared Source and Drain contacts. At low gate voltage, contact resistance has slight influence on \(g_m\) or \(f_t\). As contact resistance increases the degradation of \(f_t\) decreases, because contact resistance is small compared to induced ultra narrow SDE region, ranging \(10^3 - 10^4\) \(\Omega\) (Kedzierski J et al, 2003, A. Dixit et al, 2005, V. Subramanian et al, 2006). Hence by optimizing SDE region, we can reduce parasitic resistance to improve RF Performance. SNWT RF performance is influenced by total parasitic series resistance which is due to resistance induced by ultra narrow SDE region.

For gate underlap architecture, more gradient doping profile and longer \(L_{ex}\) leads to large parasitic resistance, similarly less gradient profile and shorter \(L_{ex}\) may result in larger overlap capacitances. Hence there is trade-off between parasitic resistance and capacitance when optimizing SDE region of SNWT for RF Performance. The better characteristic frequency \(f_t\) and \(f_{\text{max}}\) behavior can be obtained by suitable design of \(L_{ex}\), \(H_g\) and \(d_w\).
2.4 STUDY ON MULTIGATE TRANSISTOR: RF PERSPECTIVE

Many researchers worked on DG MOSFET architecture for digital logic applications. DG MOSFETs exhibit improved RF behavior because of volume inversion effect at low gate bias and better scalability. Impact of geometrical parameter of DG MOSFET on RF characteristics with structural optimization is reported by Liang J et al, (2008) and they provided design guidelines for optimizing device for RF Performance. Effect of gate engineering such as single metal (SM) DG MOSFET, Dual Metal Gate (DM) DG MOSFET and halo implanted DG MOSFET are reported by Mohankumar N et al, (2010). Figure 2.11 shows the extracted cut-off frequency ($f_c$) for n-channel DM DG MOSFET, halo implanted DG MOSFET and conventional DG MOSFET as a function of drain current ($I_d$) for $V_{ds}=1.0V$. It shows that DM-DG device exhibits better $f_c$ as compared to conventional DG MOSFET and halo DG MOSFET which is due to lower gate capacitance in saturation region. The halo doped DG MOSFET shows lower $f_c$ due to degradation of $g_m$ at strong inversion region.

![Graph showing cut-off frequency for various DG MOSFETs](image)

Figure 2.11: Obtained $f_c$ for various DG MOSFETs as a function of drain current.
The maximum oscillation frequency can be calculated with the help of gate resistance which predicts high frequency behavior. Figure 2.12 shows comparison of $f_{\text{max}}$ for n-channel DM- DG, Halo DG and conventional DG MOSFET as a function of $I_d$. It is evident from Figure 2.12 that peak $f_{\text{max}}$ occurs for gate engineered DG devices, whereas halo DG show degraded $f_{\text{max}}$ due to lower transconductance. As reported by Mohankumar N et al, 2010, gate engineering device shows an improvement of 21.6% and 20% in case of $f_t$ and $f_{\text{max}}$ values whereas channel engineering device exhibits reduction of $f_t$ by 2.7% with nearly equal $f_{\text{max}}$. But complex lithography process is a limiting factor for fabricating DM DG devices.

Angusuman Sarkar et al, (2012) studied the effect of triple-material with three different work function double gate SOI DG-MOSFET on RF performance characteristics. Figure 2.13 shows the comparison of $f_t$ for Triple Material (TM) DG MOSFET, DM-DG MOSFET and SM-DG MOSFET structures. It shows that TM-DG (1:2:3) device exhibits higher transconductance and lowest parasitic gate capacitance as compared to other structures. Higher value of $f_t$ is obtained for TM-DG MOSFET as compared to other device structures due to smaller $C_{gd}/C_{gs}$ ratio. For scaled DG MOSFET with small gate resistance, other factors like $R_i$, $g_m$ and $g_{ds}$ predominate.
Figure 2.13: Obtained $f_t$ for various DG MOSFETs as a function of drain current ($I_d$)

Figure 2.14 shows obtained maximum oscillation frequency ($f_{\text{max}}$) as a function of $I_{ds}$ for various DG devices, peak $f_{\text{max}}$ is obtained for TM-DG (1:2:3) at a drain current of $3.5 \times 10^{-4}$ A/µm (Angusuman Sarkar et al, 2012). TM-DG (1:2:3) device shows 28.85% increase in $f_{\text{max}}$ than conventional SM-DG MOSFET. But these device structures also require additional and stringent lithography processes.

Figure 2.14: Obtained $f_{\text{max}}$ for various DG MOSFETs as a function of drain current ($I_d$)
Figure 2.15: Obtained variation of (a) $f_T$ and (b) $f_{\text{max}}$ with drain current $I_{DS}$ in linear scale for various DG MOSFETs at $V_{DS} = 1.0$ V. Variation of (a) $f_T$ and (b) $f_{\text{max}}$ with drain current $I_{DS}$ in log scale (inset).

Rupendra Kumar Sharma and Matthias Bucher, (2012) studied the effect of device engineering such as graded channel dual material double gate (GCDMDG), graded channel double gate (GCDG), Dual material double gate (DMDG) MOSFET on RF Performance. Figure 2.15 shows the variation of $f_T$ and $f_{\text{max}}$ as a function of drain current for DG, DMDG, GCDG, and GCDMDG obtained by Rupendra Kumar Sharma and Matthias Bucher, (2012) . It shows that GCDG and GCDMDG exhibit higher $f_T$ due to improved $g_m$. It is interesting to note that GCDG and GCDMDG exhibit higher $f_T$ and $f_{\text{max}}$ for lower value of $I_d$. 

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The GC DG MOSFET exhibits better RF performance due to improved $g_m$ for doping profile along the channel due to improvement of inversion charge carriers inside channel region. Table 2.1 shows RF FoM of different DG devices, it is clear that GC DMDG exhibits better analog/RF performance as compared to other DG devices.

Analog performance of FinFET was investigated by Ledrer D et al, (2005), they reported that non-uniform silicidation of 3D poly-silicon gate have impact on $f_{\text{max}}$. They analyzed FinFET under static and dynamic conditions upto 110 GHz. The 3D nature of FinFET results in non uniformly doped or unsilicided region around fins leading to higher gate resistance. Hence optimization is required on polysilicon doping in order to reduce gate resistance. Ledrer D et al, (2005) also show that extra parasitic capacitance on gate side related to residual polysilicon lines along fins, a non uniform silicidation of poly si gate resulting in increase of gate resistance leads to reduced $f_{\text{max}}$ which also increases source and drain resistance compared to planar devices. Hence gate patterning gate silicidation and source/drain engineering are critical step in the design of RF FinFET devices, therefore, need to be optimized to increase $f_{\text{max}}$.

A non-quasi static small signal modeling and analytical parameter extraction of SOI FinFET were reported by In Man Kang and Hyungcheol Shin, (2006). The intrinsic parameters were extracted using Y-parameter analysis after de-embedding the extrinsic capacitance and source/drain resistance. The bias dependency of small signal parameters are reported and found that for all bias conditions, small signal model accurately predicts upto $f_t$ with total $rms$ error less than 1%.

<table>
<thead>
<tr>
<th>Devices</th>
<th>$f_T$ (GHz)</th>
<th>$f_{\text{max}}$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DG</td>
<td>476</td>
<td>1140</td>
</tr>
<tr>
<td>DMDG</td>
<td>439</td>
<td>1110</td>
</tr>
<tr>
<td>GCDG</td>
<td>546</td>
<td>1170</td>
</tr>
<tr>
<td>GCDMDG</td>
<td>534</td>
<td>1160</td>
</tr>
</tbody>
</table>

Table 2.1: RF Figures of Merit for various DG MOSFET
Figure 2.16: Obtained $f_t$, as a function of gate length for FinFETs and planar transistors

Pravias B et al, (2007) fabricated FinFET with variable gate length with silicon fin height of 60nm. Figure 2.16 shows the obtained $f_t$ as function of gate length at $V_{ds}=1.1V$ (Pravias B et al, 2007). It is evident that RF behavior of FinFET is severely affected by reduced effective transconductance. The impact of parasitic capacitance on higher gate length device will greatly affect $f_t$ as compared to small channel devices by varying fin width, $R_{sd}$ can be decreased which improves $f_t$ but SCE increases. The parasitic source and drain resistances can be reduced by spacer width reduction and Si epitaxy. But spacer width reduction will lead to increased SCE (Kranti A et al, 2007). $R_{sd}$ reduction without SCE can be achieved by selective epitaxial growth.

2.4 SUMMARY

In this chapter, theory on RF FOM of transistor and stability factor and detailed review on design challenges of various field effect transistors for RF application is presented. The review shows that impact of physical parameter and intrinsic and extrinsic small signal parameter on RF Performance is significant. Scaling of
conventional Si MOSFET will improve device switching performance, however, high frequency behavior of these devices do not show much improvement as compared to its counterpart non-silicon based devices. In order to have SCE suppression, multigate MOSFETs were introduced and found that these devices exhibit improved performance at RF range. This shows that multigate MOSFETs such as DG MOSFET, FinFET and Gate All Around (GAA) FET can be used for futuristic analog/RF applications. As per ITRS recommendation, the devices should exhibit $f_t$ and $f_{max}$ of 443GHz and 363GHz respectively.

From the review on RF performance of multigate transistor, it is evident that stability study on these multi gate transistors has not received attention which is one of the important FOM for the design RF amplifiers. Keeping this in mind, the RF Stability performance of DG MOSFET, DG Tunnel FET, FinFET and SNWT are reported in this thesis.