Chapter 2

Decimation Filter Design: A Toolbox Approach

A multi-standard decimation filter design often involves extensive system level analysis and architectural partitioning, typically requiring extensive calculations. This chapter describes a multistage decimation filter design tool developed in MATLAB® using Graphical User Interface Development Environment (GUIDE) for visual analysis. The toolbox is designed for six popular wireless communication standards consisting of GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX.

This chapter also presents a computationally efficient polyphase implementation of non-recursive cascaded integrator comb (CIC) decimator for Sigma-Delta Converters. This polyphase implementation offers high speed operation and low power consumption for the first stage of a multistage decimator.
2.1 Decimation Filter Design Considerations

Software defined radio (SDR) is a wireless interface technology in which software-programmable hardware is used to provide flexible radio solutions in a single transceiver system. New telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. Current RF transceivers demand higher integration for low cost and low power operations, and adaptability to multiple communication standards. Multi-standard operation is achieved by using a receiver architecture that performs channel selection on chip at baseband [Gray and Meyer, 1995]. This baseband channel filtering is performed in digital domain to adapt to the channel bandwidths, sampling rates, carrier to noise (C/N) ratio, and blocking and interference profiles of multiple communication standards [Barrett, 1997].

Sigma-delta ADCs are used in multi-standard transceivers to adapt to the requirements of different standards. The dynamic range of a SD-ADC can be easily adjusted by selecting different oversampling ratios. Sigma-delta modulator based on oversampling technique provides high resolution over wide bandwidth that is required in multi-mode receivers. High signal to noise ratio (SNR) is achieved in the signal band through noise shaping. The digital decimation filter selects a desired channel and removes the out-of-band quantization noise produced by the modulator. Further, it reduces the sampling rate from oversampled frequency of the modulator to the Nyquist rate of the channel [Norsworthy et al., 1997]. Therefore in a multi-mode transceiver, SD-ADC requires a decimation filter with programmable decimation ratios.
The design issues of decimation filters for wireless communication transceivers are well studied in literature. A low power fifth order comb decimation filter with programmable decimation ratios and sampling rates for GSM (Global System for Mobile communications) and DECT (Digital Enhanced Cordless Telecommunication) standards is presented by Gao [Gao et al., 2000]. They have developed non-recursive architecture for comb filter to achieve a low power VLSI implementation. Ghazel has presented the design and implementation of digital filter processors that can be used as downsamplers in wireless transceivers. The method is detailed for DECT standard [Ghazel et al., 2003]. Low complexity decimation filter architecture is presented [Xihuitl, 2005] by using infinite impulse response (IIR) filters implemented by all-pass sum that avoids multiplications. A low-power high linearity variable gain amplifier (VGA) embedded in a multi-standard receiver that meets the standard requirements has been reported [Amico et al. 2006]. Tao et al. have given an overview on the design considerations of the decimation filters for GSM, WCDMA (Wideband Code Division Multiple Access), 802.11a, 802.11b, 802.11g and WiMAX (Worldwide Interoperability for Microwave Access) standards [Tao et al., 2006].

As a part of the research, a decimation filter design toolbox is developed in MATLAB® Graphical User Interface Development Environment (GUIDE) addressing the design issues presented in the above papers. The toolbox includes six wireless standards consisting of GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX, and provides an appropriate multistage decimation filter for each standard. The toolbox will help the user or design engineer to perform a quick design and analysis of decimation filter for multiple standards without doing extensive calculation of the underlying methods. Decimation is done in two or three stages to reduce the hardware
complexity and power dissipation. Each stage is implemented with optimized filters so that the overall cascaded filter response meets the specification for a particular standard. The implementation complexity in terms of filter length that meets the specification for any of these standards is computed using this tool, and is tabulated.

2.2 Receiver Architecture for Multi-standard Operation

The receiver architecture that emphasizes high integration and multi-standard capability is required for new generation wireless applications. High integration can be achieved by utilizing a receiver architecture that performs baseband channel select filtering on chip. This enhances the programmability to different dynamic range, linearity and signal bandwidth to meet the requirements of multiple RF standards. A wideband high dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent channel interferers.

A direct conversion homodyne receiver architecture which is an example of a receiver suitable for high integration and adaptability [Barrett, 1997] is shown in Figure 2.1. This architecture translates the incoming frequency to baseband directly to eliminate external components within the receive path. It can be programmed for multi-standard operation since the local oscillator (LO) is tuned to the same frequency as the incoming RF frequency to select different standards. The incoming RF signal is multiplied by one sided LO signal of a frequency equal to the centre frequency of the desired signal band, and hence does not suffer from image signal interference. The down-conversion with a one sided LO signal is achieved by a quadrature mixer in which the incoming signal is multiplied by two LO signals with 90
degrees out of phase. These in-phase and quadrature-phase components are then lowpass filtered and sent to ADCs. The digital signal from ADC is given to digital signal processing section for demodulation. Homodyne receivers are multi-standard capable because the channel filtering is done at baseband. However, the noise and DC offset are to be reduced to achieve adequate dynamic range.

![Figure 2.1 Direct conversion homodyne receiver architecture](image)

**2.2.1 Reconfigurable Sigma-Delta ADC**

The sigma-delta (ΣΔ) analog-to-digital converters are widely used in wireless systems because of their superior linearity, robustness to circuit imperfections, inherent resolution-bandwidth trade off and increased programmability in digital domain. A highly linear sigma-delta modulator for multi-standard operation that can achieve high resolution over a wide variety of bandwidth requirements remains challenging. A reconfigurable ADC is a promising solution to keep the power dissipation as low as possible [Xotta et al., 2005], [Zhang et al., 2004].

Single loop and multistage noise shaping (MASH) topologies are two different approaches for implementing ΣΔ modulators. Single loop structures with a higher-order noise transfer function combined with multi-bit feedback can achieve higher dynamic range (DR) with low oversampling ratio (OSR).
But the linearity and resolution of the overall $\Sigma\Delta$ modulator are limited by the precision of the multi-bit digital-to-analog converter (DAC). MASH topology is preferred over single loop structures since the coefficients are optimized for a specific OSR. It has flexibility to handle different OSRs with little modification. MASH structures are adopted for multi-mode receivers considering the stability and reconfigurability.

The theoretical dynamic range has been used in conjunction with the implementation attributes to choose the optimal topology for different RF standards. The dynamic range $\text{DR}$ of a $\Sigma\Delta$ modulator is given by

$$DR = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} (2^B - 1)^2$$  \hspace{1cm} (2.1)

where $L$ is the order of modulator, $M$ is the OSR and $B$ is the number of bits of the quantizer. The six popular standards considered for the toolbox are GSM, WCDMA, 802.11a, 802.11b, 802.11g and WiMAX. These standards have different bandwidth requirements. Since the bandwidth requirements of WLAN-a, b, g and WiMAX are more or less the same, the same topology can be adopted with different OSRs. This will reduce the DR calculation for the main three standards GSM, WCDMA and WLAN (Wireless Local Area Network) whose DR requirements are chosen as 94dB, 79dB and 69dB respectively.

OSR can be selected as 128 for low data rate application, such as GSM receiver, due to a much smaller signal bandwidth. A basic second order modulator with 1-bit quantization is sufficient for this kind of application. In order to meet the DR requirements demanded by WCDMA, a fourth order cascaded MASH topology will be enough with an OSR of 16. If WLANa becomes the target standard, a fifth order topology is a good compromise to achieve the required DR with a 4-bit quantizer and an OSR of 8. The sigma-
delta modulator can be made programmable, and all the blocks are switched to operation only in the WLAN mode. This results in power saving when the receiver is operating in other modes. Similar considerations apply for other standards also. The OSR is chosen as 12, 12 and 8 for WLANb, WLANg and WiMAX respectively. Sigma-delta modulator is followed by a programmable decimation filter operating in the digital domain. The toolbox focuses on the design of multistage decimation filter for multiple standards, which is highlighted in Figure 2.1.

2.3 Multistage Decimation Filter

The sampling rate is downconverted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors. This minimizes the power consumption of DSP processors for demodulation and equalization. The purpose of decimation filter is to remove all the out-of-band signals and noise, and to reduce the sampling rate from oversampled frequency of the sigma-delta modulator to Nyquist rate of the channel. The decimation filter consists of a lowpass filter and a downsampler. It is possible to perform noise removal and downconversion with a single stage finite impulse response (FIR) filter. The filter order $N$ of FIR lowpass filter is given in (2.2), where $D_\omega$ is a function of the required ripples $\delta_p$ and $\delta_s$ in the passband and stopband respectively, $F_s$ is the sampling frequency and $\Delta f$ is the width of transition band.

$$N \approx D_\omega \left( \delta_p, \delta_s \right) \left( \frac{F_s}{\Delta f} \right)$$

(2.2)

As the sigma-delta modulators are oversampled, the transition band is small relative to sampling frequency leading to excessively large filter orders.
The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes much power. This can be overcome by multistage approach.

Implementing decimation filter in several stages reduces the total number of filter coefficients. The filters operating at higher sampling rates have larger transition bands, and the filters with lower transition bands operate at reduced sampling frequencies. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will lead to low power consumption. A multistage sampling rate conversion (SRC) system consists of a cascade of single stage SRC systems as shown in Figure 2.2. The ‘i\textsuperscript{th}’ stage performs decimation by a factor of ‘$R_i$’ such that the overall decimation factor ‘$R$’ is given by $R = \prod_{i=1}^{P} R_i$, where ‘$P$’ is the total number of stages. The individual filter of each stage is designed within the frequency band of interest in order to prevent aliasing in the overall decimation process.

The performance of a decimation filter depends on the filter architecture and the order of each stage of a multistage decimator. FIR filters are widely used in decimators as most of the modulation schemes require linear phase characteristics. The different filter architectures used in this work are given below.
2.3.1 Cascaded Integrator Comb Filter

Hogenauer devised a flexible, multiplier free Cascaded Integrator Comb (CIC) filter that can handle large sampling rate changes suitable for hardware implementation [Hogenauer, 1981]. The basic structure of the Hogenauer CIC filter is shown in Figure 2.3. This consists of an integrator and a comb filter as two basic building blocks. So, it is an infinite impulse response (IIR) filter followed by a finite impulse response (FIR) filter. In a CIC filter of order $k$, the integrator section consists of a cascade of $k$ digital integrators operating at the high sampling rate $F_s$. Each integrator is a one-pole filter with unity feedback coefficient, and the transfer function is

$$H_I(z) = \frac{1}{1 - z^{-1}}$$ (2.3)

The comb section consists of $k$ comb stages with a differential delay of $M$ and operates at the low sampling rate $F_s/R$, where $R$ is the rate change or decimation factor. The transfer function of a comb stage referenced to high sampling rate is

$$H_C(z) = 1 - z^{-RM}$$ (2.4)

The rate change switch between the two filter sections subsamples the output of the integrator stage reducing the sample rate from $F_s$ to $F_s/R$. In practice, the differential delay, $M$ is usually held equal to 1 or 2. Using (2.3) and (2.4), the system transfer function of the CIC filter with respect to the high sampling rate $F_s$ is given by

$$H(z) = H_I^k(z)H_C^k(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}}\right)^k = \left[\sum_{i=0}^{RM-1} z^{-i}\right]^k$$ (2.5)
The working of CIC filters is based on the fact that perfect pole/zero cancellation can be achieved. From the transfer function in (2.5), it is clear that \( R \) \( M \) zeros are generated by the numerator term with a multiplicity of \( k \). The \( k \) poles at \( z = 1 \), generated by the denominator are cancelled by the \( k \) zeros of the CIC filter [Meyer-Baese, 2001]. On evaluating the frequency response given by (2.5) at \( z = \exp(j2\pi f/R) \), where \( f \) is the frequency relative to low sampling rate \( (F_S/R) \), the magnitude response of CIC filter is obtained as

\[
|H(f)| = \left| \frac{\sin \pi Mf}{\sin \frac{\pi f}{R}} \right|^N
\]

(2.6)

As for small values of \( x \), \( \sin x \approx x \), the magnitude response given in (6) can be approximated for large \( R \) as

\[
|H(f)| = \left| RM \frac{\sin \pi Mf}{\pi Mf} \right|^N \quad \text{for} \quad 0 \leq f < \frac{1}{M}
\]

(2.7)

The output spectrum has nulls at multiples of \( f = \frac{1}{M} \). The aliasing or imaging occurs in the region around the nulls. An example of CIC response used for GSM case, with \( F_s = 34.667 \text{MHz} \), \( R = 32 \), \( M = 1 \) and \( k = 3 \) is shown in Figure 2.4.
The amount of passband aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the CIC filter. It will also increase the passband droop. The width of the passband and the frequency characteristics outside the passband are severely limited. So, CIC filters are used only to facilitate transition between high and low sampling rates. The CIC filter is followed by one or two stages of finite impulse response (FIR) filters operating at low sampling rates. These are designed to attain the required transition bandwidth and stopband attenuation.

### 2.3.2 Halfband filter

Halfband filters are a special class of symmetric FIR filters used in second stage of multistage decimators. Halfband filters are characterized by equal passband and stopband ripples ($\delta_p = \delta_s$), and the transition band is symmetrical about $\pi/2$ such that $\omega_p + \omega_s = \pi$, where $\omega_p$ and $\omega_s$ correspond to the passband and stopband edges. The impulse response $h(n)$ exhibits symmetry with almost 50% of coefficients ‘zero’ and with a magnitude of 0.5
at $F_s/4$. This implies reduced number of filter taps, lesser hardware and low power consumption. Halfband filters are used to perform decimation by a factor of 2 [Norsworthy et al., 1997]. The ideal halfband filter characteristic is as shown in Figure 2.5, where $\Delta f$ is the width of the transition band and $F_s$ is the sampling frequency.

![Magnitude response of halfband filter](image)

**Figure 2.5** Magnitude response of halfband filter

### 2.3.3 FIR filter

The third type of filter used in the multistage decimator is a FIR filter. The CIC filter response exhibits a droop in the passband which progressively attenuates the signals. The passband droop and stopband attenuation increases as the number of sections of CIC filters increases. The FIR filter used in the last stage performs decimation and CIC droop compensation. This FIR filter is designed according to the differential delay and number of sections of CIC filter along with the passband ripple and stopband attenuation to meet the overall specification of a particular standard. So, a low computational complexity multistage decimator is obtained with a CIC filter followed by
halfband and droop correct FIR filter. The magnitude response of a droop compensating FIR filter designed to compensate the passband droop produced by a CIC filter with a differential delay of $M = 1$, and number of sections $k = 4$, is shown in Figure 2.6.

![Magnitude response of droop compensating FIR filter (dB)](image)

**Figure 2.6** Magnitude response of droop compensating FIR filter with $M = 1$ and $k = 4$

### 2.4 Decimation Filter Design Specification

The specifications for all six standards considered in this toolbox and their corresponding decimation filter design parameters are given in Table 2.1. The oversampling ratio (OSR) for each standard is selected so as to get the required dynamic range for the sigma-delta modulator of a particular order and number of quantizer bits. The receiver specifications and the blocking and interference profiles are defined first in order to set the parameters for the decimation filter. There are large undesired signals called 'blockers' within the same cell, and large undesired signals known as 'adjacent channel interferers' from the neighbouring cells. These interference signals are to be limited within a certain range for each standard for proper reception of the desired signals.
The decimation filter is generally designed to minimize the undesired signals in the desired band of operation. The output carrier to noise (C/N) ratio is calculated from the bit error rate (BER) of each standard and the modulation scheme used. Table 2.2 gives the interference profile and the C/N ratio for all the six standards [Tao et al., 2006]. The passband frequency edge is taken as 80% of the bandwidth for each standard. The passband ripples are chosen to minimize signal distortions in the signal band. The stopband attenuations shown in Table 2.1 are selected according to the interference profile and C/N ratio given in Table 2.2 for each standard.

Table 2.1 Multi-standard specifications and decimation filter design parameters

<table>
<thead>
<tr>
<th>Standards</th>
<th>Frequency range (GHz)</th>
<th>Channel Spacing (MHz)</th>
<th>Symbol rate / Chip rate</th>
<th>OSR</th>
<th>Input sampling frequency, ( F_s ) (MHz)</th>
<th>Passband edge (MHz)</th>
<th>Stopband edge (MHz)</th>
<th>Passband ripple (dB)</th>
<th>Stopband attenuation (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>DL: 0.935-0.96</td>
<td>0.2</td>
<td>270.833 Ksymbols/s</td>
<td>128</td>
<td>34.667</td>
<td>0.08</td>
<td>0.1</td>
<td>0.1</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td>UL: 0.89-0.915</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WCDMA</td>
<td>DL: 2.11-2.17</td>
<td>5</td>
<td>3.84 Mchips/s</td>
<td>16</td>
<td>61.44</td>
<td>2</td>
<td>2.5</td>
<td>0.5</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>UL: 1.92-1.98</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WLANa</td>
<td>5.15-5.35</td>
<td>20</td>
<td>12 Msymbols/s</td>
<td>8</td>
<td>96</td>
<td>8</td>
<td>10</td>
<td>0.5</td>
<td>44</td>
</tr>
<tr>
<td>WLANb</td>
<td>2.4-2.4835</td>
<td>25</td>
<td>11 Mchips/s</td>
<td>12</td>
<td>132</td>
<td>10</td>
<td>12.5</td>
<td>0.5</td>
<td>42</td>
</tr>
<tr>
<td>WLANg</td>
<td>2.4-2.4835</td>
<td>25</td>
<td>12 Msymbols/s</td>
<td>12</td>
<td>144</td>
<td>10</td>
<td>12.5</td>
<td>0.5</td>
<td>44</td>
</tr>
<tr>
<td>WiMAX</td>
<td>10-66</td>
<td>20</td>
<td>16.704 Msymbols/s</td>
<td>8</td>
<td>133.632</td>
<td>8</td>
<td>10</td>
<td>0.5</td>
<td>39</td>
</tr>
</tbody>
</table>
Table 2.2 Interference profile and C/N ratio

<table>
<thead>
<tr>
<th>Standard</th>
<th>Offset from central frequency (MHz):</th>
<th>Interference magnitude (dBm)</th>
<th>C/N ratio (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>0.2 : -90</td>
<td>0.4 : -58</td>
<td>0.6 : -46</td>
</tr>
<tr>
<td>WCDMA</td>
<td>5 : -63</td>
<td>10 : -56</td>
<td>12.5 : -44</td>
</tr>
<tr>
<td>WLANa</td>
<td>20 : -63</td>
<td>40 : -47</td>
<td>28</td>
</tr>
<tr>
<td>WLANb</td>
<td>25 : -35</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>WLANg</td>
<td>20 : -63</td>
<td>40 : -47</td>
<td>28</td>
</tr>
<tr>
<td>WiMAX</td>
<td>20 : -68</td>
<td>40 : -49</td>
<td>21</td>
</tr>
</tbody>
</table>

2.5 Multi-standard Decimation Filter Design Toolbox

The ‘Multi-standard Decimation Filter Design Toolbox’ is designed using the Signal Processing Toolbox and Filter Design Toolbox from MATLAB® using GUIDE environment. The user can select a required wireless communication standard and obtain the corresponding multistage decimation filter implementation using this toolbox. The toolbox will help the user or design engineer to perform a quick design and analysis of a decimation filter for multiple standards without doing extensive calculation of the underlying methods. The front panel of the graphical user interface (GUI) is shown in Figure 2.7 and the features of the toolbox are detailed below.

Multistage decimation filter design

The toolbox is designed for six popular wireless communication standards, namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. Initially, the desired standard is selected from the pop-up menu as in Figure 2.8 and the filter design is obtained by pressing the push button named Multistandard Decimation Filter Design. The filter details such as the required channel spacing for a selected standard, passband edge, stopband edge, input
sampling frequency, OSR, number of stages and type of filter used in each stage, decimation factors for each stage, and filter complexity are displayed on the GUI as in Figure 2.9.
Cost of implementation

The cost of implementation of the multistage decimator is displayed as in Figure 2.10, in terms of total number of adders and multipliers required for all stages.

![Cost of Implementation](image)

**Figure 2.10** Cost of decimation filter implementation for GSM

Filter coefficients

The filter coefficients can be visualized by pressing the push button named *Filter coefficient*. Then a message box will pop up and it displays the filter coefficients for each stage. For GSM (current display), the message box displays the number of sections of the CIC filter as ‘3 integrators and 3 combs’, 11 halfband filter coefficients and 101 droop compensation FIR filter coefficients, as shown in Figure 2.11.

![Message box displaying filter coefficients](image)

**Figure 2.11** Message box displaying filter coefficients for GSM
Filter response

The push button named Filter response is used to display the magnitude response. The desired response such as the magnitude response for individual filter stages, cascaded responses after each stage or the multistage overall response, can be selected from the pop-up menu as in Figure 2.12. The magnitude response of individual filter is displayed on the graphical window, called axes, embedded on the front panel of the GUI as in Figure 2.13. The cascaded filter response and the overall response of the multistage decimator are displayed using filter visualization tool (FVTool) in MATLAB as in Figure 2.14.

![Figure 2.12 Pop-up menu for magnitude response selection](image)

![Figure 2.13 (a)](image)
Figure 2.13 Individual Filter response for GSM displayed on front panel of GUI

(a) CIC filter (b) Halfband filter (c) FIR filter
Pole-Zero plots

To get the pole-zero plot of individual filter, each stage can be selected from a pop-up menu as in Figure 2.15. The push button named Pole-Zero Plot is used to display the corresponding plot on the front panel graphical window of the GUI as in Figure 2.16. The multiplicity number of each pole and zero are indicated in the plot. The filter is stable when the poles lie inside the unit circle in z-plane. FIR filters are stable by design since the transfer functions do not have denominator polynomials, and thus no feedback to cause instability. CIC filters are stable even with the presence of integrators, as the poles on unit circle due to the denominator of transfer function are cancelled by equal number of zeros at the same position produced by the numerator.

The multistage decimation filter implementation results obtained for each of the six standards using the new toolbox are given in Section 6.1.
Figure 2.15 Pop-up menu for pole-zero plots

Figure 2.16 (a)
Figure 2.16 Pole-Zero plot of individual filters for GSM (a) CIC filter (b) Halfband filter (c) FIR filter
2.6 Polyphase Implementation of Non-recursive Comb Decimators

In a sigma-delta analog-to-digital converter (SD-ADC), the most computationally intensive block is the decimation filter and its hardware implementation may require millions of transistors. Since these converters are now targeted for a portable application, a hardware efficient design is an implicit requirement. In this effect, this section presents a computationally efficient polyphase implementation of non-recursive cascaded integrator comb (CIC) decimators for sigma-delta converters. The SD-ADCs are operating at high oversampling frequencies and hence require large sampling rate conversions. The digital decimator part consists of a lowpass filter and a downsampler that is responsible for transforming the low resolution oversampled signal into high resolution signal sampled at Nyquist rate [Allen and Holberg, 2002]. The filtering and rate reduction are performed in several stages to reduce hardware complexity and power dissipation [Norsworthy et al., 1997]. The CIC filters are widely adopted as the first stage of decimation due to its multiplier free structure. In this research, the performance of polyphase structure is compared with the CICs using recursive and non-recursive algorithms in terms of power, speed and area. This polyphase implementation offers high speed operation and low power consumption.

The first stage of decimation filter can be implemented very efficiently using a cascade of integrators and comb filters which do not require multiplication or coefficient storage. The remaining filtering is performed either in single stage or in two stages with more complex FIR or IIR filters according to the requirements. The amount of passband aliasing or imaging
error can be brought within prescribed bounds by increasing the number of stages in the CIC filter. The width of the passband and the frequency characteristics outside the passband are severely limited. So, CIC filters are used to make the transition between high and low sampling rates. Conventional filters operating at low sampling rate are used to attain the required transition bandwidth and stopband attenuation. In this manner, CIC filters are used at high sampling rates where economy is critical, and conventional filters are used at low sampling rates where the number of multiplications per second is less.

Different implementations of decimation filter architecture for sigma-delta ADCs are available in literature. Hogenauer has described the design procedures for decimation and interpolation CIC filters with emphasis on frequency response and register width [Hogenauer, 1981]. Candy has proved that a Sinc$^k$ filter is appropriate for decimating sigma-delta modulation down to four times the Nyquist rate [Candy, 1986]. A power optimized Sinc$^4$ filter is implemented for decimation by removing the pipelining registers between the adders [Gursoy et al., 2005]. Another FIR-Sinc architecture is given for low-power consumption by taking the advantage of the low number of bits at input and use of multiple V$_{DD}$ logic [Li and Wetherrell, 2000]. Simon Foo has presented a fifth order sigma delta modulation and decimation technique with a very high precision noise shaping, suitable for high fidelity audio application [S. Foo et al., 2004]. F Gao et al. have investigated the performance of non-recursive algorithm for comb decimators [Gao et al., 1999]. The comparison results with recursive CIC structure show that the non-recursive implementation provides reduced power consumption and increased circuit speed. Laddomada has performed performance comparison of various comb-
based decimation filter schemes for sigma-delta ADCs. The use of a combination of sharpened filter cells and modified-comb cells which diminishes the filter passband droop and increases the quantization noise rejection is presented [Laddomada, 2007].

To reduce power consumption in a circuit either the clock rate or the operating voltage has to be decreased. But sigma-delta ADCs utilize oversampling at high clock rates, and hence power consumption will increase. Lowering the operating voltage increases the circuit delay that will put a bound on operating frequency. One solution to this problem is to use parallel processing. Polyphase decomposition has been traditionally used to implement parallel structures in digital signal processing. Yang proposed a polyphase CIC implementation for high speed operation [Yang and Snelgrove, 1996], but the complete rate reduction is achieved by using another CIC which is again a recursive structure.

2.6.1 Classical Recursive CIC Filter

Hogenauer devised a flexible, multiplier free recursive filter suitable for hardware implementation that can handle large sampling rate changes as detailed in Section 2.3.1. The major problems encountered with the Hogenauer CIC filter include the following. The first problem is that the register widths can become large for large rate change factors. The register growth is considered in filter design process to ensure that no data are lost due to register overflow. The maximum register growth $G_{max}$ from the first stage up to and including the last stage is approximated as in (2.8), where $R$ is the rate change factor, $M$ is the differential delay and $k$ is the number of stages of the CIC filter.

Decimation Filter Design: A Toolbox Approach
\[ G_{\text{max}} = (RM)^k \] (2.8)

If the number of bits in the input data stream is \( B_{in} \), then the register growth can be used to calculate \( B_{max} \), the most significant bit at the filter output. It is given by \( B_{max} = \left\lfloor k \log_2 RM + B_{in} - 1 \right\rfloor \), where the least significant bit of the input register is considered to be bit number ‘zero’. Since the first ‘\( k \)’ stages of the filter are integrators with unity feedback, the integrator outputs grow without bound for uncorrelated input data. It can be concluded that \( B_{max} \) is the most significant bit not only for the integrators, but also for the combs that follow. \( B_{max} \) is large for many practical cases, and can result in large register widths. So, truncation or rounding has to be used at each filter stage to reduce the register widths.

Second problem with the recursive CIC filter is the higher power consumption since the integrator stage works at the highest oversampling rate with a large internal word length. As the decimation ratio and filter order are increasing, power consumption increases significantly. Third problem is that the circuit speed will be limited by the large word length and recursive loop of the integrator stage.

2.6.2 Non-Recursive CIC filter

The non-recursive CIC filter reduces power dissipation and increases speed of operation by avoiding the IIR part in the recursive structure [Gao et al., 1999]. The difference between the non-recursive and recursive algorithms is that they use different VLSI structures to implement the transfer function in (2.5). Taking differential delay \( M = 1 \) and rate change factor, \( R = 2^N \), the transfer function can be rewritten as
\[ H(z) = \left( \frac{1 - z^{-R}}{1 - z^{-1}} \right)^k = \left( \sum_{i=0}^{R-1} z^{-i} \right)^k = \left( \sum_{i=0}^{2^k-1} z^{-i} \right)^k = \prod_{i=0}^{N-1} (1 + z^{-2^i})^k \quad (2.9) \]

The non-recursive CIC architecture is shown in Figure 2.17. Every stage is a FIR filter but operates at different sampling rate. After each stage, the sampling rate is reduced by a factor of 2. The output from a sigma-delta modulator of word length \( B_{in} \) is given as input to the filter. The word length increases through every stage by ‘\( k \)’ bits, but the sampling rate decreases through every stage by a factor of 2 starting from the oversampling rate \( f_s \). Thus the word length is short when the sampling rate is high, and when the word length increases the sampling rate decreases. In the recursive algorithm, the IIR part has to operate with the oversampling rate and has a word length of \( \lfloor k \log_2 R + B_{in} \rfloor \) bits. In the non-recursive algorithm, the first stage works at the oversampling rate but has only a word length of \( (B_{in} + k) \) bits. This helps to reduce the power consumption and to increase the maximum speed of operation for non-recursive decimator.

\[ \begin{array}{c}
\downarrow 2 \\
\downarrow 2 \\
\downarrow 2 \\
\end{array} \]

\text{Stage 1} \quad \text{Stage 2} \quad \ldots \quad \text{Stage N}

\[ X(n) \quad (1+z^{-1})^k \quad (1+z^{-1})^k \quad (1+z^{-1})^k \quad \downarrow 2 \quad \downarrow 2 \quad \downarrow 2 \quad Y(m) \]

\textbf{Figure 2.17 Non-recursive comb decimator}

2.6.3 Polyphase Non-Recursive CIC Architecture

The average power consumption of a digital signal processing system is determined by the number of computations performed per sample, the word
length and the sampling frequency. Parallel processing through polyphase decomposition is an efficient way to achieve high speed and lower power consumption [Meyer-Baese, 2001]. In this research, polyphase decomposition is done for each FIR filter stage of the non-recursive decimator as shown in Figure 2.18. Here, decimation occurs at the input of each filter reducing the sampling frequency by a factor of 2. So the number of computations per sample is also reduced to half of that for non-recursive implementation leading to low power consumption. As in non-recursive structure, polyphase implementation is also not having any register overflow problems, and the word length of initial stages is limited to a few bits. Since the use of polyphase decomposition has reduced the operating frequency of the filters significantly at the last stages, the critical path is no longer a problem. So, the polyphase CIC filter can operate at a higher speed.

\[
H(z) = \sum_{k=0}^{N} h(k)z^{-k} = \sum_{m=0}^{L-1} z^{-m} E_m(z^L)
\]  

(2.10)
where

\[ E_m(z) = \sum_{n=0}^{[(N+1)/L]} h(Ln + m)z^{-n}, 0 \leq m \leq L - 1, \text{ with } h(n) = 0, \text{ for } n > N \]  

(2.11)

Performing two-branch polyphase decomposition of each FIR block of the non-recursive comb decimator, the transfer function in (2.9) can be rewritten as

\[ H(z) = \sum_{m=0}^{1} z^{-m} E_m(z^2) \]  

(2.12)

Consider the comb decimator with decimation factor \( R = 64 \), and order \( k = 4 \), so that the polyphase filter equations are:

\[ E_0(z) = h(0) + h(2)z^{-1} + h(4)z^{-2} = 1 + 6z^{-1} + z^{-2} \text{ and } \]
\[ E_1(z) = h(1) + h(3)z^{-1} = 4 + 4z^{-1}. \]

The corresponding polyphase CIC filter architecture is shown in Figure 2.19. The multipliers in the polyphase filter are implemented using shift and add method, which require only adder circuit as shifting can be achieved by properly routing the input bits. For example, multiplication of input ‘x’ by 6 is carried out by adding ‘4x’ and ‘2x’. So, the operation is only an addition as the numbers ‘4x’ and ‘2x’ are easily obtained by inserting zeros at least significant bit positions.

The simulation results obtained for a 4th order CIC filter using the three different architectures are presented in Section 6.2. Performance evaluation of three architectures for different decimation factors as \( R = 64, 128, \) and 256 are also given.
2.7 Summary

A multistage decimation filter design toolbox is developed for six popular wireless communication standards, namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. The toolbox allows the user or design engineer to perform a quick design and analysis of decimation filters for different standards without doing extensive calculation of the underlying methods. The tool provides the user with all necessary details of decimation filter designed for the selected standard including filter coefficients, frequency response, pole-zero plot, cost of implementation etc. The implementation of multistage decimation filter reduces the hardware and computational effort while meeting the standard requirements. A computationally efficient polyphase implementation of non-recursive CIC filter is presented. The polyphase CIC filter has higher speed of operation, lower power consumption and more area requirement. So, the designer can trade and select the CIC architecture based on the overall system requirements. The implementation results obtained for the multistage decimators using the toolbox and the polyphase non-recursive comb decimator are presented in Section 6.1 and 6.2 respectively.