ABSTRACT

From its humble commencement in the early 1950’s to the production of circuits with millions of components today, VLSI design has brought the power of the mainframe computer to the laptop. This tremendous advancement in the area of VLSI design is made achievable by the development of sophisticated design tools and software. There is a stressing demand on industry for faster and more efficient CAD tools for VLSI design due to the increase in complexity and size of circuits. The future growth of VLSI systems depends significantly on the research and development of Physical Design (PD) Automation tools.

The problem of partitioning appears in numerous areas ranging from VLSI, parallel programming, to molecular biology. In order to keep up with the rapid increase in system complexity due to substantial advances in VLSI process technology, partitioning is performed at various level of design hierarchy until subproblems become more manageable. The scope of the research study is to develop an algorithm using evolutionary approach for digital Circuit Layout problem based on graph partitioning technique. Keeping in view, the nature and wide applications of the problem, accordingly, a research study with the title DEVELOPMENT OF AN ALGORITHM USING EVOLUTIONARY APPROACH FOR DIGITAL CIRCUIT LAYOUT BASED ON GRAPH PARTITIONING TECHNIQUE” was envisaged with the following aims and objectives.

- Transformation of graph partitions into problem domain.
- Development of an algorithm using evolutionary approach.
- Evaluation of developed algorithm by taking number of iterations, memory requirements and minimum cuts during computation.
- To verify the algorithm by comparing with existing approaches.

Maninder Kaur
(Registration No.402 PU(P)98)