IMPACT OF DIELECTRIC POCKET ON DIFFERENT GATE GEOMETRY MOSFET ARCHITECTURES FOR IMPROVED ANALOG AND DIGITAL PERFORMANCE: MODELING AND SIMULATION

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ABSTRACT

“The important thing is not to stop questioning. Curiosity has its own reason for existing. One cannot help but be in awe when he contemplates the mysteries of eternity, of life, of the marvelous structure of reality. It is enough if one tries merely to comprehend a little of this mystery every day. Never lose a holy curiosity”

Albert Einstein

Unprecedented growth in information technology (IT), and communications market has been mainly enabled by continuous progress in silicon-based complementary metal-oxide-semiconductor (CMOS) technology. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is one of the successful and most manufactured electronic device in the history of electronics. This progress has been made possible only because of considerable reduction in the device dimensional, which also results in higher device density and better device performance. The economic productivity has also been continuously increasing with every new technology generation due to the reduction in cost-per-chip. In addition to its scalability, the unique properties of CMOS transistor such as high input resistance,
zero static power dissipation, simple layout and process steps have made MOSFET as the main component of the current integrated circuits (ICs). Nowadays, semiconductor technologies based ICs are everywhere and indispensable in our daily life. These include not only microprocessor, memory chips but also ranging from portable electronics (i.e. multimedia devices and high definition display) to telecommunications, transportation and medical instruments. These broad applications are possible only because of the mixed signal technologies which enable large scale integration of non-digital functions such as analog/radio frequency signal processing, data conversion between analog and digital functions.

Downscaling of silicon based MOSFET has almost reached its saturation limit due to increase in charge sharing between source and drain region which results in reduction of gate control over the channel depletion charges and also leads to the emergence of sever Short Channel Effects (SCEs). The major key issues in reducing the size of the CMOS transistor are: unacceptable leakage current which does not allow the further reduction in threshold voltage, higher electric field at the drain side which worsens the device reliability, punchthrough effect and enhance Channel Length Modulation (CLM) and Drain Induced Barrier Lowering (DIBL) Effect. This posed a fundamental limitation on the maximum performance improvement that can be achieved by downscaling the feature size of CMOS technology.

Thus, due to those ever increasing SCEs, two major approaches are introduced to extend Moore’s Law for CMOS devices and these are: (i) channel materials other than silicon to improve carrier transport properties and (ii) advance device engineering techniques to improve the electrostatics of CMOS. Use of high-k material and new gate electrode material have improved carrier transport properties as well as new material in the source/drain region which reduced channel resistance and carrier injection properties of the device. Current approaches (or architectures) to control these small-geometry effects by using device engineering techniques are: lateral channel engineering (i.e. Lightly Doped Drain, Halo MOSFET and Dielectric Pocket/Insulated Shallow Extension MOSFET), substrate engineering (Silicon On Insulator and Silicon On Nothing MOSFET) and gate electrode engineering (Dual Gate FET, Split Gate, Double Gate MOSFET, Tri Gate and FinFET) techniques. Among the
various advance non-classical device architectures mentioned above, we have focused our discussion in the present dissertation on the Insulated Shallow Extension (ISE)/Dielectric Pocket (DP) MOSFET, Silicon On Nothing (SON) MOSFET and Double Gate (DG) MOSFET. Silicon On Insulator technology, Pocket implant technology (such as Dielectric Pocket MOSFET) and multiple gate technology (such as Double Gate MOSFET and FinFET).

In Silicon On Insulator (SOI) Technology, buried insulator (having SiO$_2$ as an insulator) is used to suppress the undesirable coupling between source drain and drain channel region resulting in reduce source drain junction capacitance along with the improved switching speed and reduced power consumption. In addition this, perfect lateral and vertical isolation from substrate in SOI MOSFET provides latch-up and inter-device leakage free CMOS technology. Further improvement in the device performance is achieved by replacing SiO$_2$ with Air as buried insulator which provides better isolation between drain and substrate region i.e. Silicon On Nothing (SON) MOSFET.

The performance of the CMOS technology can also be improved by placing insulating layer near the drain side to suppress the drain side electric field and hence Hot Carrier Effects i.e. Insulated Shallow Extension (ISE) MOSFET also known as Dielectric Pocket (DP) MOSFET. ISE MOSFET provides better dielectric isolation from drain to source region resulting in lower threshold voltage roll-off and punchthrough effect.

In order to overcome the device performance degradation at sub-100 nm regime, extensive consideration has been devoted to explore the potential benefits of two non-classical devices i.e. ISE/DP and SON MOSFET to form a single device design i.e. Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET. The insulating layer present at the side walls and underneath the channel region in ISESON MOSFET provides the necessary isolation required to suppress the undesirable coupling between drain and active channel region apart from substrate region. In addition to this, ISESON MOSFET exhibits lower $DIBL$, punchthrough
effect, threshold voltage roll-off, and suppression of leakage current apart from excellent sub-threshold slope as compared to ISE and SON MOSFETs.

Thereafter, the emphasis has been shifted towards multi gate MOSFET design i.e. Double Gate (DG) MOSFET to further enhance the gate controllability over the channel region and to eliminate floating body effect arising in bulk MOSFET. DG MOSFET possesses higher channel mobility because of undoped silicon body and avoids undesirable effect of threshold voltage roll-off arising due to channel dopant fluctuation. However, the DG MOSFET suffers from enhance parasitic (gate to source ($C_{gs}$) and gate to drain ($C_{gd}$)) capacitances as compared to bulk MOSFET. In order to overcome this problem, Dielectric Pockets were placed at side wall of DG MOSFET resulting in new device design known as Dielectric Pocket Double Gate (DP-DG) MOSFET. This significantly decreases the parasitic capacitance and also reduces the dopant-out diffusion from the Source/Drain to the channel region. However DP-DG MOSFET has higher effective channel length in comparison to DG MOSFET and thus has lower on-state current and trans-conductance. To overcome this problem, Empty Space in Double Gate (ESDG) MOSFET was proposed where insulating layer (or Empty Space Layer) was present in the channel region instead at the side walls of DG MOSFET.

The present work is mainly focussed on modeling and simulation of three non-classical device architectures i.e. ISESON MOSFET, DP-DG MOSFET and ESDG MOSFET for the assessment of its analog and digital performance.

In Chapter 1, brief overview of the fundamental concept and objective behind the research problem related to present dissertation is provided. Overview of the various non-classical devices, their merits and demerits and fabrication related issues are also summarized in Chapter 1.

In Chapter 2, the impact of insulating layers on the single gate device geometry architecture is presented by combining the features of two advance MOSFET designs i.e. Insulated Shallow Extension MOSFET and Silicon On Nothing MOSFET resulting in new device architecture known as Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET. The physics behind the operation of
proposed ISESON MOSFET is explored by developing an efficient two dimensional analytical channel potential model. The model is further extended to derive the temperature dependent drain current expression from sub-threshold to saturation region. The performance of the device has also been analysed at different channel length, drain bias, channel thickness, side pillar thickness and shallow extension depth. It is also evident from the results that better short channel immunity as well as immunity against temperature variation is achieved by using air as buried insulator instead of SiO$_2$. The impact of gate stack architecture with ISESON MOSFET at sub-100 nm regime is also presented in chapter 2. The unique features of ISESON MOSFET i.e. higher immunity against temperature variation with electrical parameters like threshold voltage roll-off, sub-threshold slope and DIBL are highlights of the chapter.

In addition to this, chapter also deals with the development of a 2-D analytical drain current model for Ultra Thin Body/BOX (UTB) ISESON MOSFET design which account for the impact of back gate bias on the threshold voltage, sub-threshold slope, DIBL and $I_{on}/I_{off}$ ratio. The impact of temperature variation on the characteristics of NMOS inverter (such as Voltage Transfer Characteristics VTCs, supply voltage, inverter gain and transient response) and impact of back gate bias on the performance of CMOS inverter (such as VTCs and supply voltage) based on different devices is also investigated through exhaustive device simulation.

Continuous scaling of the MOSFET dimensions has made silicon technology viable for high-performance logic, memory and RF applications. However this adversely affects the analog performance of the device. In Chapter 3 extensive consideration has been given to analyze the performance of various non-classical devices such as Insulated Shallow Extension (ISE), Silicon On Nothing (SON) and ISESON MOSFETs for high temperature analog performance through extensive device simulations. Results reflect that ISESON MOSFET shows better immunity against temperature variation in terms of $g_m/I_{ds}$ ratio, early voltage, output resistance and device gain thus proving its efficacy for low-voltage low-power analog applications. The use of gate stack architecture (high-k/SiO$_2$) further helps to increase the on-current ($I_{on}$) and bring out a simultaneous reduction in off-current ($I_{off}$), thereby
greatly increasing the $I_{on}/I_{off}$ ratio, which is an indicator of better switching characteristics in digital circuits. Also the much better linearity performance i.e. higher $VIP_2$, $VIP_3$ and $IP_3$ is seen in case of ISESON MOSFET as compared to ISE and SON MOSFETs even at the high operating temperature. The impact of technology variations (i.e. shallow extension depth and thickness of side pillar) on linearity and analog performance metrics (i.e. $g_m/I_{ds}$, $V_{ea}$, and $R_{out}$) has also been examined to determine optimum bias point. Thus it has been observed that sufficiently thick side pillar and shallower extension depth are required to achieve the desired short channel behaviour at the expense of drain current and trans-conductance.

Chapter-4 explores the behaviour of the ISESON MOSFET as a reliable and temperature variation resistant device design exhibiting improved CMOS inverter performance. The chapter also looks into the temperature dependence of Voltage Transfer Characteristics, supply voltage, and noise margin of CMOS inverter circuit which play a vital role in designing small sized VLSI circuits. Moreover, intensive device simulation has been carried-out to investigate the invariance of ISESON MOSFET against technology scaling (in terms of channel length and supply voltage) at 32 nm channel length. Smaller propagation delay associated with ISESON MOSFET further makes the device more reliable for high performance logic circuits such as NAND and NOR gate and ring oscillator as compared to ISE and SON based circuits. The advantage of the proposed ISESON MOSFET for sequential circuit applications (i.e. R-S and D Flip Flop) is also highlighted. It is also examined that ISESON MOSFET results in superior analog ($g_m/I_{ds}$, $V_{ea}$, $R_{out}$ and $I_{on}/I_{off}$) and digital (propagation delay, noise margin, dynamic power dissipation and power delay product) performance as compared to ISE and SON MOSFET under the influence of interface charges.

In previous chapters, the impact of insulating layers on the performance of single gate devices (i.e. ISE, SON and ISESON) has been discussed. Apart from these structures, Double Gate MOSFET has received serious attention due to its unique property of enhanced current driving capability as well as higher gate controllability. However, DG MOSFET suffers from higher parasitic capacitances i.e. gate to drain and gate to source capacitances. In order to overcome the problem, a new structural
concept of Double Gate MOSFET incorporating Dielectric Pocket (DP-DG) MOSFET has been proposed in Chapter 5. In DP-DG MOSFET, dielectric pockets are present at the side walls of DG MOSFET to suppress associated parasitic capacitances. Moreover, extensive consideration has been given to develop physics based analytical drain current model of DP-DG MOSFET incorporating Channel Length Modulation and velocity saturation effect for channel length down to 32 nm. Chapter 5 also discusses the development of temperature dependent analytical model for DP-DG MOSFET which is further extended to investigate the behavior of NMOS inverter under wide range of operating temperature. It is demonstrated that integration of Dielectric Pocket with Double Gate MOSFET leads to improve analog and digital performance metrics as compared to conventional bulk, DP and DG MOSFETs. The higher $I_{on}/I_{off}$ ratio in DP-DG MOSFET indicates faster switching response and the observed intrinsic delay is lower for DP-DG MOSFET. Further, the impact of change in position of dielectric pockets (i.e. either dielectric pocket is present at the S/D junctions or inside the drain region) on the performance of DP-DG MOSFET has also been studied in chapter 5. It is evident from the results that the position of dielectric pocket when it is at the side wall but completely inside the channel region exhibit poor linearity performance, higher intrinsic delay apart from higher dynamic power dissipation and power delay product.

In previous chapter, dielectric pockets were placed at the side walls of DG MOSFET. However, DP-DG MOSFET still suffers from lower drain current and trans-conductance. Chapter 6 explores the novel way of overcoming the problem by changing the position of insulating layer (Empty Space Layer) from the side walls to middle of the channel region resulting in a new device design known as Empty Space in Double Gate (ESDG) MOSFET. The complete drain current model from sub-threshold to saturation region incorporating velocity saturation and $DIBL$ effects for un-doped symmetric ESDG MOSFET is presented. The developed model based on Evanescent Mode Analysis is also useful for the assessment of device characteristics down to sub-50nm regime thereby offering extensive outlook for the design and optimization of ESDG MOSFET. The enhance drain current and highly suppressed drain–conductance is achieved in ESDG MOSFET resulting in higher early voltage
(V_{ox}) and output resistance. ESDG MOSFET provides significantly improved Short Channel immunity and better analog performance metrics ($g_m$, $g_m/I_{ds}$, $V_{ea}$ and $R_{out}$) even at higher operating temperature. It is also evident from the results that ESDG MOSFET exhibits lower temperature sensitivity. The chapter also demonstrates the superiority of ESDG MOSFET for better digital application due to its higher noise margin and lower propagation delay of various logic gates (like NAND and NOR gate and ring oscillator) circuits.

Finally, Chapter 7 presents an overall summary of the results obtained in the previous chapters of this dissertation and also highlights the possible future research work in this direction.