CHAPTER 4

Performance Investigation of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for Low Voltage Digital Applications
4.1 Introduction

CMOS technology has been widely used as the digital switching element in semiconductor memories and System On Chip (SOC) applications due to low cost, large noise margin, easy manufacturing process and overall device reliability [Kuo01]. CMOS is also used in all recent technologies such as to develop random access memory (RAM), microprocessors, Digital Signal Processors (DSP) and image sensors. The device scaling leads to improved on-current ($I_{on}$) and enhanced switching speed, however it also introduces Short Channel Effects (SCEs) that adversely affect the device performance and long term reliability [Schwierz10]. For low-voltage-low-power digital applications, device should have smaller $I_{off}$ and better noise immunity [Slisher99]. Lower leakage current and high drive current is required to optimize the power dissipation and gate delay metric ($CV/1$). While it is essential to maintain advantages associated with technology scaling, it is also important to find solution for minimizing leakage current and sub-threshold slope. Hence, it has become essential to explore for non-conventional alternative device structures to meet the ITRS requirements for mixed mode Integrated Circuit (ICs).

In chapter 2 and 3, the performance of a new device design i.e. Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET was investigated, that combines the advantages of both ISE and SON MOSFETs. In chapter 2, temperature dependent drain current model of gate stack ISESON MOSFET was developed. The suitability of the ISESON MOSFET for improved analog and linearity performance was investigated in chapter 3 for wide range of operating temperature i.e. 300 K to 500 K [Kumari12b]. But its usage for low-voltage low-power digital application were not discussed.

The advantages offered by ISESON MOSFET over conventional ISE and SON MOSFET, which are also beneficial for improved digital performance are 1) reduction in parasitic capacitances, 2) lower sub-threshold slope, 3) higher device gain and 4) lower drain/substrate electric field [Kumari12a]. ISESON MOSFET also exhibits lower gate and substrate leakage current in comparison to ISE and SON MOSFET [Kumari12c]. In chapter 2, behavior of N-MOS inverter based on ISESON, SON and ISE MOSFET were discussed. But N-MOS inverter circuit showed higher dynamic
power dissipation due to resistive load. Thus in order to overcome this problem, load resistance as in case of N-MOS inverter, is replaced by P-MOS transistor to form CMOS inverter circuit. CMOS inverter circuit is considered as the basic building block of digital applications. The preliminary results related to CMOS inverter were presented in chapter 2 but only the Voltage Transfer Characteristics (VTCs) of CMOS inverter was studied. However, the other parameters which are also essential for describing behavior of CMOS inverter which were not addressed in chapter 2 are therefore discussed in the present chapter. Thus, the impact of parametric variation on static and transient behavior of CMOS inverter circuit [Weste06] [Taur09] based on different devices have been analyzed in this chapter for low voltage digital applications.

In the present chapter, the impact of process variability and immunity against temperature variation has also been studied for ISESON (as shown in figure 4.01) based CMOS inverter circuit. In addition to this, the application of the non-classical devices have also been extended to explore its usage for implementing the universal logic gate (i.e. NAND, NOR and XOR gate) [Mitra04] [Shadrokh08], ring oscillator [Baker00] and sequential circuits (i.e. R-S and D Flip Flop).

**Figure 4.01** Schematic cross sectional view of ISESON MOSFET, where $\varepsilon_1$, $\varepsilon_2$ and $\varepsilon_3$ are permittivity of channel, buried oxide layer and side pillars respectively; $T_{st}$ (10 nm) is the thickness of side pillar, $X_e$ is the shallow extension depth, $N_{ch}$ ($1\times10^{17}$ cm$^{-3}$) and $N_{sub}$ ($2\times10^{18}$ cm$^{-3}$) are doping concentration in the channel and the substrate region respectively, $L$ is the channel length, $t_d$ is the channel thickness and $t_{box}$ is the buried oxide thickness [Kumari13a].
4.2 Simulation Details and Calibration

The CMOS inverter circuit having load (P-MOS) and driver MOSFET (N-MOS) is investigated using ATLAS 3D mixed mode simulation [ATLAS10]. The models invoked during simulation are parallel and transverse FiELD dependent MOBility (FLDMOB) and CONcentration dependent MOBility (CONMOB) models along with the Shockley–Read–Hall (SRH for fixed carrier lifetime) recombination model for minority carrier recombination.

In order to account for the “non-local” effects such as velocity overshoot and impact ionization which have significant impact on the device performance at the shorter gate lengths, hydrodynamic transport model is used for the device simulations. Hydrodynamic transport model adds continuity equations for the carrier temperatures, and impact ionization coefficients as functions of carrier temperatures rather than functions of local electric field. The various physical device parameters which are used during simulation are listed in Table 4.01.

Table 4.01 List of parameters used for simulating various devices i.e. ISESON, SON, SOI ISE and Bulk MOSFET [Kumari13a].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ISESON</th>
<th>SON</th>
<th>SOI</th>
<th>ISE</th>
<th>Bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length (L)</td>
<td>32 nm</td>
<td>32 nm</td>
<td>32 nm</td>
<td>32 nm</td>
<td>32 nm</td>
</tr>
<tr>
<td>Channel Thickness (t₀)</td>
<td>10 nm</td>
<td>10 nm</td>
<td>10 nm</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Buried Oxide Thickness (tl)</td>
<td>10 nm</td>
<td>10 nm</td>
<td>50 nm</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Shallow Extension Depth (Xₑ)</td>
<td>5 nm</td>
<td>--</td>
<td>--</td>
<td>5 nm</td>
<td>--</td>
</tr>
<tr>
<td>Shallow Extension Thickness (Tₑ)</td>
<td>10 nm</td>
<td>--</td>
<td>--</td>
<td>10 nm</td>
<td>--</td>
</tr>
<tr>
<td>Channel Doping (Nₓ) (in cm⁻³)</td>
<td>1×10¹⁷</td>
<td>1×10¹⁷</td>
<td>1×10¹⁷</td>
<td>1×10¹⁷</td>
<td>1×10¹⁷</td>
</tr>
<tr>
<td>Substrate Doping (Nₓ) (in cm⁻³)</td>
<td>2×10¹⁸</td>
<td>2×10¹⁸</td>
<td>2×10¹⁸</td>
<td>Nₓ=Nₓ</td>
<td>Nₓ=Nₓ</td>
</tr>
<tr>
<td>Permittivity of channel (ε₁)</td>
<td>11.9</td>
<td>11.9</td>
<td>11.9</td>
<td>11.9</td>
<td>11.9</td>
</tr>
<tr>
<td>Permittivity of buried oxide (ε₂)</td>
<td>1</td>
<td>1</td>
<td>3.9</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Permittivity of side pillars (εₓ)</td>
<td>3.9</td>
<td>--</td>
<td>--</td>
<td>3.9</td>
<td>--</td>
</tr>
</tbody>
</table>

Due to non-availability of experimental results of ISESON MOSFET, the simulation results were calibrated with the available experimental results for 80 nm channel length n-type SON MOSFET [Monfry01]. The same models were further used to simulate various devices such as ISESON, SON and ISE MOSFET.
In order to obtain the best fit with the experimental result (as shown in figure 4.02), transverse and parallel field dependent mobility model were adjusted by choosing acc.sf=0.5 and inv.sf=0.5. The accumulation saturation factor (acc.sf) and inversion saturation factor (inv.sf) describes the ratio of majority carrier concentration in accumulation and inversion layer respectively before and after bending of conduction and valence bands. The default values of hydrodynamic model have been used i.e KSN=0 and KSP=0 [ATLAS10] where KSN and KSP are the hot carrier models for electrons and holes respectively.

For fair comparison among various devices i.e. ISESON, ISE, SON and bulk MOSFET, same structural parameters for different devices are taken into consideration. Thereafter, threshold voltage for both P-MOS and N-MOS is optimized i.e. \( V_{th}=0.25 \) V at \( V_{ds}=0.5 \) V for different devices by tuning the metal gate work-function in the range of 4.4 eV to 4.9 eV, keeping all other device parameters constant.

The two important aspects that needs to be analyzed for better digital performance are: 1) hot carrier reliability and 2) leakage current. The hot carrier reliability of the device is analyzed by investigating electron temperature as shown in figure 4.03. It is evident from the results that ISESON MOSFET exhibits lower electron temperature near the drain side in comparison to ISE and SON MOSFETs. This is mainly because
of screening effect due to presence of dielectric pockets at the drain side of ISESON MOSFET. Thus ISESON MOSFET shows improved hot-carrier reliability, because of lower electron temperature at the drain side as compared to ISE and SON MOSFETs.

![Graph showing electron temperature variation along the channel length](image)

**Figure 4.03** Variation of electron temperature along the channel length for different devices; L=60 nm [Kumari12d].

![Graph showing transfer characteristics](image)

**Figure 4.04** Transfer characteristics ($I_d$-$V_{gs}$) of N-MOS and P-MOS for different devices at $V_{ds}$=1.0 V, in (a) logarithmic scale and (b) linear scale [Kumari13a].

Figure 4.04 (a) and (b) shows the transfer characteristics in both logarithmic and linear scale respectively for different devices. Lower leakage current in ISESON MOSFET as compared to other devices is mainly because of the lower electron temperature near the drain side as discussed above. As can be seen from the
figure 4.04, leakage current for N-MOS and P-MOS (i.e. \(I_n\) and \(I_p\) at \(V_{gs}=0\) V) are same in case of each devices i.e. ISESON, ISE, SON and bulk MOSFET. Also, significantly enhanced leakage current (\(I_{off}\)) for bulk MOSFET is observed followed by ISE, SON and ISESON MOSFET. In addition to this, ISESON MOSFET also exhibits lower on-state current as compared to SON MOSFET because of higher effective channel length [Jurczak01]. The various other parameters like sub-threshold slope, \(I_{on}/I_{off}\) ratio, DIBL and on-state resistance (\(R_{on}\)) that has a strong influence on the digital circuit design are also investigated and analyzed in Table 4.02.

It can be seen that, ISESON MOSFET exhibits higher \(I_{on}/I_{off}\) ratio followed by SON, ISE and bulk MOSFET because of the tremendously suppressed leakage current thereby showing fast digital performance as compared to other devices. The sub-threshold slope (\(S\)) of ISESON MOSFET is also lower than that of the other devices. The on-state resistance of ISESON MOSFET is marginally higher than the SON MOSFET because of the comparatively lower on-state current. Furthermore, the DIBL is also lower in case of ISESON MOSFET, thereby showing immunity against the drain bias variations.

**Table 4.02 Simulated electrical parameters of various devices i.e. ISESON, SON, ISE and Bulk MOSFET optimized at the same \(V_{th}\) (0.25 V); \(L=32\) nm, \(t_{ox}=10\) nm, \(T_{si}=10\) nm, \(X_e=5\) nm, \(I_{on}\) at \(V_{gs}=1\) V and \(R_{on}\) at \(V_{gs}=1\) V [Kumari13a].**

<table>
<thead>
<tr>
<th></th>
<th>DIBL (mV/V)</th>
<th>(I_{on}/I_{off})</th>
<th>(S) (mV/decade)</th>
<th>(R_{on}) (KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISESON</td>
<td>355</td>
<td>2.0×10^6</td>
<td>100</td>
<td>1.8</td>
</tr>
<tr>
<td>SON</td>
<td>378</td>
<td>1.0×10^6</td>
<td>113</td>
<td>1.7</td>
</tr>
<tr>
<td>ISE</td>
<td>722</td>
<td>9.6×10^4</td>
<td>171</td>
<td>2.9</td>
</tr>
<tr>
<td>Bulk</td>
<td>950</td>
<td>1.6×10^3</td>
<td>220</td>
<td>35</td>
</tr>
</tbody>
</table>

**4.3 CMOS Inverter Characteristics**

In this section, the digital performance of various devices is assessed using ATLAS 3D mixed mode simulation [ATLAS10]. The basic CMOS inverter circuit is described as a series combination of P-MOS (as load) and N-MOS (as driver) transistors as shown in figure 4.05. \(C_L\) is the external load capacitor and output of the inverter circuit is taken across the drain and ground terminal of N-MOS transistor.
In case of CMOS inverter, output is (Voltage Transfer Characteristics VTCs) either “Zero” or “One” i.e. high or Low. In these states only one of the MOS transistor is in conducting state at a time. However, transition region also exists between “High” and “Low” level. During the transition region, both N-MOS and P-MOS are in conducting state. For fast digital performance, inverter circuit should exhibit a narrow transition region. In order to understand the physics behind the operation of real CMOS inverter circuit, output voltage w.r.t to input voltage is plotted in figure 4.06 (a) showing different regions of operation.

**Region A:** when the input voltage is less than the threshold voltage of the NMOS, the P-MOS is in linear region and N-MOS is in cutoff.

**Region B:** when the input voltage is in between the $V_{tn}$ and half of the supply voltage. In this region P-MOS is in non-saturated region and N-MOS is in saturation

**Region C:** when both the transistors are in saturation region.

**Region D:** when P-MOS is in saturation while NMOS is in its non-saturation region.

**Region E:** when P-MOS is in cut-off region and N-MOS is in linear mode.

$V_{in}$ and $V_{tp}$ specify the threshold voltage of N-MOS and P-MOS transistor. $V_{inv}$ is the point at which the output voltage is equal to the applied input voltage i.e. $V_{in}=V_{out}$. For better digital performance $V_{inv}$ should be at $V_{dd}/2$ [Weste06].
There is no static current or static power dissipation during region A and E, since only one of the transistor is in conducting state. Power dissipation occurs during the transition region i.e. in region B to D, when a pulse of charging and discharging current flowing through the circuit as shown in figure 4.06 (b). The static power dissipation in the CMOS circuit is given by $I_{dd}V_{dd}$. Ideally, the switching current is zero ($I_{dd}= 0$) in CMOS inverter but the various leakage current associated with the nanoscale device causes the switching current to be nonzero ($I_{dd}> 0$) and can be defined as the quiescent leakage current $I_{ddQ}$. Thus in real inverter circuit the static power dissipation is described by $I_{ddQ}V_{dd}$. 

Figure 4.06 (a) Voltage Transfer Characteristics and (b) switching current of CMOS inverter circuit showing various region of operations (Modified from [Leblebici03]).
The *Voltage Transfer Characteristics* and switching current of the CMOS inverter based on different devices as a function of input voltage are plotted in figure 4.07 (a) and (b) respectively. As can be seen from the figure, *VTC* of SON MOSFET based inverter is steeper than that of ISE and SOI devices and hence more preferable for fast digital applications. In ISESON MOSFET, *VTC* becomes much more steeper due to improved sub-threshold slope and higher device gain [Kumari11a]. The current drawn from the power supply during the high-to-low transition or vice versa in CMOS inverter, reaches its peak value with $V_{in}=V_{inv}$. The sharpness in the peak of the switching current is a strong function of transition slope of *VTC* curve.

![Figure 4.07](image-url)
The sharper peak in case of ISESON MOSFET (in figure 4.07(b)) reflects narrow transition region of VTC curve. The transition region $\Delta V_{in}$ is given by the change in input voltage during which output makes a transition from 90% to 10% of final value ($V_{out_{max}}$) i.e. $V_{in}$ at $V_{out_{max}}$ (90%)-$V_{in}$ at $V_{out_{max}}$ (10%). The observed transition region is 0.14 V for ISESON MOSFET while it is 0.18 V for SON, 0.3 V for ISE, 0.32 V for SOI and 0.82 V for bulk MOSFET.

The switching current of bulk MOSFET is constant thereby showing linear VTC curve which is due to high sub-threshold slope ($S$) and off-state current ($I_{off}$). Although, the maximum supply (switching) current is higher in ISESON MOSFET as compared to other devices but it remains zero when only one of the MOS transistor is in conducting state i.e. either P-MOS or N-MOS which is mainly responsible for the static power dissipation as discussed above.

4.3.1 Channel Length Variation

In this section, the impact of channel length scaling on the performance CMOS inverter (Voltage Transfer Characteristics and supply current), based on ISESON MOSFET has been investigated for two different cases. 

Case I: device is optimized at different channel length i.e. threshold voltage ($V_{th}$) of the device remains same with channel length scaling (figure 4.08 (a) and (b)), and

Case II: device is not optimized at different channel lengths i.e. threshold voltage of the device decreases with decreasing channel length (figure 4.08 (c) and (d)).

The reduction in channel length for both optimized and non-optimized cases results in the degradation in transition region of VTC curve as shown in figure 4.08 (a) and (c) respectively. This is mainly because of enhancement in sub-threshold slope of the device with channel length scaling. In case of optimized device, as channel length decreases, peak value of switching current also decreases as shown in figure 4.07 (b). However it increases in case of non-optimized device (figure 4.08 (d)). At higher channel lengths, switching current falls very sharply leading to steeper VTC curve because of the lower sub-threshold slope of the device.

As the device dimensions are scaled, threshold voltage of the device decreases and switching speed (given by $g_{m}/C_{gg}$) increases. Since the supply voltage ($V_{dd}$) remains
constant leading to enhancement in the power dissipation. Thus, there is a trade-off between switching speed and power dissipation in CMOS inverter circuit.

![Graphs showing VTC curves and switching current for ISESON MOSFET with different channel lengths.](image)

**Figure 4.08** Impact of channel length variation on (a) VTC curve and (b) switching current for ISESON MOSFET optimized at the different channel lengths, and Impact of channel length variation on (c) VTC curve (d) switching current for non-optimized ISESON MOSFET for $T=300$ K and $V_{dd}=1$ V [Kumari13a].

### 4.3.2 Supply Voltage Scaling

This sub-section addresses the impact of voltage scaling on CMOS inverter characteristics by investigating the switching current and inverter gain. As can be seen through figure 4.09 (a)-(c) i.e. with decrease in applied drain bias (or supply voltage) ($V_{dd}$), maximum value of switching current decreases and the peak of switching current also gets broadened.
Figure 4.09 Effect of supply voltage ($V_{dd}$) on the switching current of different devices for (a) $V_{dd}=0.8$ V, (b) $V_{dd}=0.6$ V, and (c) $V_{dd}=0.5$ V; Effect of supply voltage ($V_{dd}$) on the inverter gain of different devices for (d) $V_{dd}=0.8$ V, (e) $V_{dd}=0.6$ V, and (f) $V_{dd}=0.5$ V; $T=300$ K and $L=32$ nm [Kumari13a].
It can also be observed from figure 4.09 (a)-(c) that, the reduction in switching current with $V_{dd}$ scaling is lower in ISESON MOSFET in comparison to SON and ISE MOSFET. The lower dependency of supply current on $V_{dd}$ implies the invariability of ISESON MOSFET against supply voltage variation. The wider peak of switching current reflects large transition zone in the VTC and this is maximum in case of ISE MOSFET followed by SON and ISESON MOSFET.

The impact of the supply voltage scaling on the inverter gain has also been investigated in this sub-section. Dynamic power dissipation deteriorates with increase in supply voltage (as it is directly proportional to square of supply voltage) and also affects the inverter gain. The inverter gain is calculated by taking the slope of the VTC curve and is given by [Rossello04] [Kaya07] [Kranti10]:

$$\text{Gain} = -\frac{\partial V_{out}}{\partial V_{in}}$$  \hspace{1cm} (4.01)

Figure 4.09 (d)-(f) illustrates that, ISESON MOSFET has highest inverter gain for supply voltage down to 0.5 V as compared to other devices due to the higher device gain ($g_m/g_d$). It can also be observed that the degradation in inverter gain with $V_{dd}$ scaling is 14% in ISESON MOSFET while it is 16% in SON and 20% in ISE based inverter circuit. This is mainly because of reduced charge sharing between source and drain region in ISESON MOSFET thereby showing immunity against supply voltage scaling as compared to other devices.

### 4.3.3 Temperature Variation

In this section, the impact of temperature variation on the performance of inverter circuit like VTCs and switching current has been investigated through exhaustive device simulation. Figure 4.10 (a)-(c) shows that, as the operating temperature increases, inverter performance deteriorates i.e. the width of transition region of VTC increases. This is mainly attributed to enhancement in leakage current and sub-threshold slope of the device with increase in operating temperature. In addition, ISESON MOSFET exhibits narrow transition region ($\Delta V_m$) even at higher operating temperatures thereby showing faster switching speed and higher noise margin as compared to other devices (Noise margin is discussed in next section).
Figure 4.10 Effect of temperature variation on Voltage Transfer Characteristics VTCs and switching current of different devices i.e. (a) ISESON MOSFET (b) SON MOSFET and (c) ISE MOSFET; L=32 nm and $V_{dd}=0.5$ V [Kumari13a].
The degradation in inverter performance at higher temperature is also lower in ISESON MOSFET in comparison to ISE and SON MOSFET. Figure 4.10 (a)-(c) also demonstrates the impact of temperature variation on supply current of inverter circuit. The change in maximum value of switching current with operating temperature is also lower in ISESON MOSFET as compared to SON and ISE MOSFET thereby showing lesser dependence of power dissipation on operating temperature. The immunity of ISESON MOSFET against temperature variation is mainly attributed to the presence of insulating layers that can suppress the leakage current of the device [Shih03] [Ghosh11]. This is because the degradation in device performance with increase in operating temperature is lower in ISESON MOSFET as compared to other devices [Kumari12b].

### 4.4 Noise Margin

For high performance circuit operation, noise margin should be as high as possible [Hause93] [Buddaraju08] so that the output signal will not be corrupted by the noise voltage present at the input level. The Voltage Transfer Characteristics discussed in the previous section is used to calculate noise margin of the CMOS inverter. The most commonly used specifications to describe the noise margin are: 1) low noise margin \( (NM_L) \) and 2) high noise margin \( (NM_H) \). Figure 4.11 shows the Voltage Transfer Characteristics in butterfly form to calculate the noise margin of the inverter circuit.

**Figure 4.11** Voltage transfer characteristics of CMOS inverter circuit in butterfly form showing noise margin.
$NM_L$ is defined as the difference in maximum of low input voltage ($V_{IL}$) recognized by the input terminal and the maximum low output voltage ($V_{OL}$) at the output terminal [Weste06].

\[ NM_L = V_{IL} - V_{OL} \quad (4.02) \]

Similarly $NM_H$ is defined as the difference in minimum high output voltage ($V_{OH}$) at the output terminal and the minimum high input voltage ($V_{IH}$) recognized by the input terminal [Weste06].

\[ NM_H = V_{OH} - V_{IH} \quad (4.03) \]

Input between $V_{IL}$ and $V_{IH}$ is defined as the indeterminate region (i.e. no logic level exist between these two voltage level). To avoid this region, $V_{IH}$ should be as close as possible to $V_{IL}$. This implies that the output of the inverter circuit should change abruptly from high to low or vice versa i.e. the transition zone should be very narrow with high inverter gain.

![Image of graph showing noise margin for different channel lengths and supply voltages](image-url)

**Figure 4.12** Comparative study of noise margin ($NM_L$) for different channel lengths and supply voltages [Kumari13a].

Figure 4.12 represents the noise margin of various devices at different channel lengths and supply voltages. It can be seen that, noise margin of ISESON MOSFET is higher than that of the ISE and SON MOSFET due to improved high-to-low transition region of the VTC as shown previously. As the channel length decreases, noise margin of the
device decreases. Also, the change in noise margin with channel length scaling is lower in ISESON MOSFET as compared to other devices. This is because the enhancement in sub-threshold slope and leakage current with channel length scaling is more pronounced in ISE and SON MOSFET as compared to ISESON MOSFET. It can also be observed that the reduction in noise margin with $V_{dd}$ scaling is lower in ISESON MOSFET as compared to ISE and SON MOSFET. The immunity against supply voltage variation in ISESON MOSFET with respect to other devices is mainly attributed to the lower carrier injection into channel region from the source side with increase in $V_{dd}$. This is due to reduced lateral coupling between S/D regions and back channel coupling between drain and channel regions that results in reduction of $DIBL$ and leakage current.

It is also important to study impact of parameter variation on the inverter performance such as noise margin. Thus the variation in noise margin due to the fluctuation in supply voltage (i.e. $\pm 5\%$ of $V_{dd}$) is also investigated. As can be seen from the figure 4.12, the percentage change in noise margin with supply voltage ($\pm 5\%$) is significantly lower in ISESON MOSFET ($7\%$) as compared to ISE ($34\%$) and SON MOSFET ($25\%$). This is because the enhancement in drain side depletion width with increase in drain bias is higher in ISE and SON MOSFET as compared to ISESON MOSFET. Thus, ISESON MOSFET shows better tolerance towards supply voltage variation as compared to SON and ISE MOSFET.

![Figure 4.13](image_url)

**Figure 4.13** Noise margin ($NM_H$) of the devices at different operating temperatures; $V_{dd}=0.5$ V [Kumari13a].
Figure 4.13 illustrates the impact of temperature variation on the high level noise margin ($N_{M_H}$) of different devices. As can be seen from the figure, the percentage degradation in noise margin with operating temperature is negligible in ISESON MOSFET (3%) and SON MOSFET (18%) as compared to ISE MOSFET (53%). This is because, the impact of temperature variation in on-state resistance $R_{on}$ is lesser in ISESON MOSFET as compared to SON and ISE MOSFETs as shown in Table 4.03. Table 4.03 shows that, on-state resistance $R_{on}$ is lower in SON followed by ISESON and ISE MOSFETs. The higher ($R_{on}$) in ISESON MOSFET is due to the lower drive current in ISESON MOSFET. Also, as the operating temperature increases $R_{on}$ increases. But, the enhancement in $R_{on}$ with increasing temperature is lesser in ISESON MOSFET followed by SON and ISE MOSFETs. Thus, ISESON MOSFET shows higher immunity towards temperature variation as compared to SON and ISE MOSFET and can be operated at high temperature without much degradation in device performance.

Table 4.03 Value of $R_{on}$ at two different temperatures; $V_{ds}$=0.5 V and $V_{gs}$=1.0 V [Kumari13a].

<table>
<thead>
<tr>
<th></th>
<th>T=300 K</th>
<th>T=400 K</th>
<th>% change</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISESON</td>
<td>1.8 KΩ</td>
<td>2.11 KΩ</td>
<td>14.6</td>
</tr>
<tr>
<td>SON</td>
<td>1.7 KΩ</td>
<td>2.06 KΩ</td>
<td>17.99</td>
</tr>
<tr>
<td>ISE</td>
<td>3.0 KΩ</td>
<td>4.28 KΩ</td>
<td>29.99</td>
</tr>
</tbody>
</table>

### 4.5 Immunity Against Process Variation

The variation in the position of the Dielectric Pocket (DP) is a serious issue while fabricating a un-conventional device as it also affects the performance of the CMOS inverter in terms of speed and stability. Thus the impact of position of dielectric pockets on the performance of inverter circuit has been investigated in this section. Two cases are discussed in this section: case a) when dielectric pockets are present inside the S/D region (at the junction of S/D and channel region) and case b) when dielectric pockets are present at the interface of the S/D and channel region i.e. partially inside the channel or partially inside the S/D region as shown in figure 4.14 (a) and (b) respectively.
The impact of structural modifications on the device performance of ISESON MOSFET is also an important aspect to study which is described as case c) when dielectric pockets are present completely inside the channel region (in figure 4.14 (c)). As shown in figure 4.14 (d)-(f), the transition zone of the VTC curve or noise margin is almost same in all the three cases. The marginal improvement in noise margin in case c) as compared to case a) is attributed to the fact that when DP is present inside the channel region, effective channel thickness of the device decreases. This results in reduction in sub-threshold slope because of higher gate controllability over inversion charge carriers and thereby showing improvement in VTC.

![Diagram showing different cases of dielectric pocket placement in ISESON MOSFET channel](image)

**Figure 4.14** Half cross-section view of the ISESON MOSFET with (a) case a) when Dielectric Pocket DP is present inside the S/D region (b) case b) when DP is partially inside the channel and partially inside the S/D region and (c) case c) when DP is inside the channel region at the S/D and channel interface regions. Impact of process variation on the VTC curve (in butterfly shaped) of the ISESON MOSFET for (d) case a, (e) case b, (f) case c; T=300 K and V_{dd}=0.5V [Kumari13a].

- 161 - | Vandana Kumari
4.6 Transient Analysis

In the previous sections, CMOS inverter circuit is investigated to analyze the transfer characteristics to determine noise margin of the circuit. This analysis is described as static analysis which is time independent. In the next section, transient analysis of CMOS inverter circuit is demonstrated to calculate propagation delay of the circuit. To study the transient behavior of different devices, a pulse input is applied at the input terminal of the inverter. The parameters used to calculate propagation delay of the CMOS inverter is described in figure 4.15 i.e. rise time (low-to-high propagation delay) and fall time (high-to-low propagation delay). The rise time \(t_{PLH}\) is defined as the time interval for a waveform to rise from 10% to 90% of its steady state value. Fall time \(t_{PHL}\) is defined as the time interval for a waveform to fall from 90% to 10% of its steady state value. The total propagation delay is the average of rise time and fall time and is given as [Chung97]:

\[
\tau_p = \frac{t_{PHL} + t_{PLH}}{2}
\]  

(4.04)

Figure 4.15 Idealized transient response of an CMOS inverter circuit showing rise time and fall time to calculate propagation delay (Modified from [Shterengas10]).
Figure 4.16 shows the rise time and fall time of the transient output response of CMOS inverter using various devices i.e. ISESON, ISE and SON MOSFET. The overshoot in the output response, is mainly because of the gate-to-drain capacitances and have a negative impact on the performance of the device. The overshoot in the output response is maximum in ISE MOSFET followed by SON MOSFET and ISESON MOSFET.

The switching characteristic of CMOS inverter is described in terms of the estimation of rise time \((t_{PLH})\) and fall time \((t_{PHL})\) values as discussed above. The calculated propagation delay of ISESON MOSFET is 8.55ps which is 54% lower than the SON MOSFET, and 81.3% from ISE MOSFET. The higher propagation delay of ISE MOSFET based inverter circuit is due to (a) smaller trans-conductance \((g_m)\) and drive current and (b) lower output resistance as compared to SON MOSFET and ISESON MOSFET [Kumari12b]. Because of increased internal nodal capacitances (i.e. gate to drain capacitance and gate to source capacitance) and higher sub-threshold slope of ISE MOSFET, the output of ISE based circuit does not go to completely off state. Thus, ISESON MOSFET can be used for fast switching applications as compared to ISE MOSFET and SON MOSFET.
4.7 Implementation of Logic Gates

The performance of the logic gates such as NOR and NAND gate have been investigated in this section using ISESON, ISE and SON MOSFET. The conventional circuit diagram of the NAND and NOR gate implemented using CMOS inverter circuit has been used to illustrate the capabilities of ISESON MOSFET for reconfigurable logic systems.

The output of NOR gate is high only when both the input voltage are low otherwise the output remains low. However the output of the NAND gate is high, when at least one of the input voltage is low.

Figure 4.17 and 4.18 illustrates the timing diagram of NOR and NAND logic gate respectively.

Figure 4.17 The simulated comparison of the timing diagram for NOR gate logic; $T=300$ K and $V_{dd}=0.5V$ [Kumari13a].
It is evident from the results that, low-to-high and high-to-low propagation time of ISE MOSFET based NOR and NAND gate is highly deteriorated followed by SON and ISESON MOSFET based logic gates. This implies that ISESON MOSFET has fast switching speed compared to both SON and ISE based circuits. This is mainly attributed to (a) high device gain \((g_m/g_d)\) (b) lower leakage current and (c) improved sub-threshold slope \((S)\) resulting in a reduction of charging and discharging time when connected to the load capacitor \((C_L)\).

The poor performance of ISE MOSFET based logic gates is due to the higher parasitic capacitance as compared to SON and ISESON MOSFET that can increase the charging and the discharging time of the device through load capacitor \((C_L)\).

**Figure 4.18** The simulated comparison of the timing diagram for NAND gate logic; \(T=300 \, K\) and \(V_{dd}=0.5 \, V\) [Kumari13a].
4.8 Three-stage Ring Oscillator

In this section, performance of three stage ring oscillator based on different devices has been analyzed. Oscillators are generally used for translating the information signal and channel selection in radio frequencies and light-wave communication systems. Oscillators are also used to provide a timing reference i.e., a clock signal, to synchronize the operations in digital electronic systems. The output of an ideal oscillator is a periodic signal. However, because of the presence of undesirable perturbation and noise in electronic systems, the output may be corrupted. Thus the output of the real oscillator is not perfectly periodic. Ring oscillator also known as delayed oscillator is a combination of cascaded inverter circuits, connected in a close loop chain i.e., the output of first inverter is the input of the second inverter and so on. Numerous useful features of the ring oscillators because of the chain of delay stages have created great interest in all electronics systems. The main attractive features of the ring oscillator are: (i) provides oscillations at low voltages, (ii) provides high frequency oscillations with low power dissipation, and (iii) also provides multiphase outputs. The multiphase output can further be logically combined to realize the clock signals used in a number of applications in communication systems [Mandal10]. The frequency of oscillations of ring oscillator is given as:

\[ f_c = \frac{1}{2n\tau} \]  

(4.05)

Where \( n \) is the number of inverter circuit (three in present analysis) and \( \tau \) is the delay between input and output cycle. Figure 4.19 shows the output response of 3-stage ring oscillator and it can be observed that, the ISE based ring oscillator provides maximum delay followed by SON and ISESON based oscillator and hence, reducing the frequency of oscillations. The calculated frequency of oscillations for ISESON MOSFET based ring oscillator is 5.99 GHz whereas it is 3.7 GHz for SON MOSFET. The improvement in ISESON MOSFET based output is due to lower parasitic capacitance and higher output resistance (\( R_{out} \)) as compared to other two devices i.e. ISE and SON MOSFET [Kumari12a].
The output of the ISE MOSFET does not go completely to its steady state value (i.e. 0.5 V) because of the increased parasitic capacitance leading to enhancement in RC time constant of the circuit. Hence it is not a suitable candidate for ring oscillator as compared to other devices i.e. SON and ISESON MOSFET.

4.9 Transmission Gate

In the previous sections, series combination of N-MOS and P-MOS transistor (i.e. CMOS inverter circuit) is used to investigate the digital performance of various devices. In this section, transmission gate as shown in figure 4.20 (a), is used to compare the performance of different devices. Transmission gate is demonstrated as the parallel combination of N-MOS and P-MOS transistor [Khan04] [Lopresti06] in which the output is same as the applied input with additional propagation delay because of internal nodal capacitances and applied external capacitor [Weste06]. High input voltage ($V_{dd}$) at N-MOS transistor and low input voltage (0 V) at P-MOS allow both transistors to conduct simultaneously and transmit the signal from input to output. In reverse case, both the transistors are in off state. In transmission gate, if one of the MOS fails to conducts, the other transistor provides the necessary conducting path for switching. But, it also increases the propagation delay of the circuit [Pathak02] [Pearson08].
All simulations in subsequent sections are performed for 22 nm channel length. At 22 nm channel length, Quantum Mechanical Effects are also taken into consideration to study the device and circuit behavior accurately. In order to ascertain the accuracy of simulated results the models used in simulation are first calibrated with the experimental results of 30 nm channel length MOSFET [Harrison04] as shown in figure 4.20 (b). The simulation result shows good agreement with the experimental results.

The physical models adopted for the simulation of 22 nm channel length devices are same as the models discussed previously along with the Band Gap narrowing model because of higher channel doping and quantum model [ATLAS10]. For fair comparison amongst all devices, P-MOS and N-MOS combinations of all the devices are first optimized to have same threshold voltage i.e. $V_{th} = 0.25 \text{ V}$ at $V_{ds} = 0.5 \text{ V}$.

### 4.9.1 Impact of Load Capacitor on Transmission Gate

In this sub-section, the transient behavior of ISESON, SON and ISE MOSFET based transmission gate has been analysed and compared at different load capacitance ($C_L$). The propagation delay of the transmission gate is calculated in the same way as that of the inverter circuit described in the previous section.
As shown in figure 4.21 (a)-(c), ISESON MOSFET possesses lower propagation delay as compared to SON and ISE MOSFET i.e. 27% lower from SON and 35% from ISE MOSFET. As the load capacitor ($C_L$) increases from 1 fF to 20 fF, propagation delay of the device also increases. But the enhancement in propagation delay with increase in load capacitor is lower in ISESON MOSFET (51%) followed by ISE (54%) MOSFET and SON MOSFET (67%) thereby showing better immunity against load capacitance variation. The lower propagation delay is mainly attributed to lower sub-threshold slope ($S$), higher device gain ($g_m/g_d$), higher $R_{out}$ and lower internal parasitic capacitances i.e. $C_{gs}$ and $C_{gd}$ in ISESON MOSFET as compared to other devices.

Figure 4.21 Output response of transmission gate with different load capacitance ($C_L$) for (a) ISESON MOSFET, (b) SON MOSFET and (c) ISE MOSFET; $L=22$ nm, $t_{si}=8$ nm, $t_{box}=8$ nm, $N_{ch}=1 \times 10^{23} \text{ m}^{-3}$, $N_{sub}=2 \times 10^{24} \text{ m}^{-3}$, $T_o=10$ nm, $X_e=2$ nm and $V_{ds}=0.5$ V [Kumari13b].
In the previous sections, superiority of ISESON MOSFET based various digital circuits like logic gates and ring oscillator implemented using CMOS inverter circuit have been discussed through exhaustive mixed mode simulation. In mixed mode simulation, the computation time required to study the behavior of the digital circuit depends on number of MOS transistors used to realize that circuit. As the number of MOS transistors increases, computational time to study the performance of the circuit also increases. In the next section, only NMOS is used to implement logic gate i.e. XOR gate and sequential circuits such as R-S Flip Flop and D Flip Flop [Ko00] [Heo01] in which the number of MOS transistors used to realize the logic circuit increases.

4.10 Implementation of XOR Gate

Figure 4.22 shows the simulated timing diagram of the input and output of the XOR gate for different devices.

Figure 4.22 Timing diagram of XOR gate for L=22 nm, t_ox=8 nm, t_box=8 nm, N_{ch}=1×10^{17} cm^{-3}, N_{sub}=2×10^{19} cm^{-3}, T_{st}=10 nm, X_e=2 nm and V_{ds}=0.5 V [Kumari13b].
The low-to-high or high-to-low delay is higher in case of ISE MOSFET based XOR gate followed by SON and ISESON MOSFETs. This is because of internal node capacitances i.e. $C_{gs}$ and $C_{gd}$ due to which ISE MOSFET based circuit takes longer time to charge and discharge through external loading capacitor. The calculated propagation delay for ISESON MOSFET is 9 ps which is 14% lower than the SON (12 ps) and 74% lower than that of ISE (38 ps) MOSFET.

### 4.11 Sequential Logic Circuit

This sub-section illustrates the behavior of sequential logic circuit based on different devices. The sequential circuits discussed in this section are R-S (Reset and Set) and D (Delay) Flip-Flop whose truth table is shown in Table 4.04.

<table>
<thead>
<tr>
<th></th>
<th>R-S Flip Flop</th>
<th>D Flip Flop</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>S</td>
<td>V\text{out}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Not defined</td>
</tr>
</tbody>
</table>

The basic R-S and D Flip-Flop circuits [Ko00] [Heo01] [Khan04] are used for investigating the flip flop response. The input/output timing diagram of the R-S and D flip flop is plotted in figure 4.23 and 4.24 respectively. Results show that, propagation delay is lower in ISESON MOSFET based sequential circuits followed by SON and ISE MOSFET. The calculated propagation delay in ISESON based R-S flip flop is 18 ps while it is 29 ps in SON and 36 ps in ISE which is 37% lower from SON and 50% from ISE MOSFET.

This improvement is mainly due to the reduction in parasitic capacitance in ISESON MOSFET due to the presence of side pillars and also due to the ultra thin buried oxide layer. Because of ultra thin buried oxide in ISESON and SON MOSFETs the impact of p-n junction which is formed between the bottom of the highly doped S/D and the substrate region is reduced resulting in lower propagation delay in comparison to ISE MOSFET.
Figure 4.23 Timing diagram of R-S flip-flop: $L=22 \text{ nm}, t_{si}=8 \text{ nm}, t_{box}=8 \text{ nm}, N_{ch}=1\times10^{21} \text{ m}^{-3}, N_{sub}=2\times10^{24} \text{ m}^{-3}, T_{st}=10 \text{ nm}, X_e=2 \text{ nm}$ and $V_{ds}=0.5 \text{ V}$ [Kumari13b].

Figure 4.24 Timing diagram of D flip-flop: $L=22 \text{ nm}, t_{si}=8 \text{ nm}, t_{box}=8 \text{ nm}, N_{ch}=1\times10^{21} \text{ m}^{-3}, N_{sub}=2\times10^{24} \text{ m}^{-3}, T_{st}=10 \text{ nm}, X_e=2 \text{ nm}$ and $V_{ds}=0.5 \text{ V}$ [Kumari13b].
It is also observed that, the peak overshoot voltage is minimum in ISESON MOSFET based R-S Flip Flop as compared to other devices due to lower gate to drain capacitance also known as Miller capacitance $C_{gd}$. The overall overshoot voltage depends on the $C_{gd}$ and drive current $I_{on}$. Although, the $I_{on}$ of ISESON MOSFET is lower than SON MOSFET but the overshoot voltage is still lower in ISESON MOSFET due to the lower $C_{gd}$ at comparable $I_{on}$ current.

The parasitic capacitances (i.e. gate to source capacitance $C_{gs}$ and gate to drain capacitance $C_{gd}$) and the power dissipation (i.e. static $P_{sat}$ and dynamic $P_{dyn}$) of the logic circuit is shown in Table 4.05. As seen from the Table, $C_{gd}$ is higher for SON MOSFET followed by ISE and ISESON MOSFET thus poses serious limitation for switching applications. The lower parasitic capacitance in ISESON MOSFET is due to the presence of side pillars at S/D junctions that prevents the dopant diffusion from S/D to channel region and thus preventing the bulk punch-through effect. In addition, the buried oxide layer underneath the channel suppresses the electrostatic coupling between S/D and the bulk region. It can also be observed that the total gate capacitance ($C_{gs}=C_{gd}+C_{gs}$) is also lower in case of ISESON MOSFET.

The dynamic power dissipation is directly proportional to effective capacitance and supply voltage [Burghartz13] given as:

$$P_{dyn} = \alpha f C_{eff} V_{dd}^2$$  \hspace{1cm} (4.06)
where \( \alpha \) is the switching factor, \( C_{\text{eff}} \) is the effective output capacitance of the switching gate or circuit, \( V_{dd} \) is the applied supply voltage and \( f \) is the maximum operation frequency.

Thus power dissipation is mainly depends on the charging/discharging time of the load capacitor and on-state current \( (I_{on}) \) \cite{Weste06} of the device. The lower parasitic capacitance of ISESON MOSFET results in the lower power dissipation of ISESON MOSFET based circuits followed by SON and ISE MOSFETs. Since the on-state current of ISESON MOSFET is higher than the ISE MOSFET but the reduction in \( C_{gg} \) of ISESON MOSFET is dominated by the enhancement in drive current thereby causing lower power dissipation. In SON MOSFET, \( I_{on} \) and parasitic capacitance both are higher as compared to ISESON, and ISE MOSFET thereby showing higher power dissipation as compared to ISE and ISESON MOSFET.

It can be also observed that, Power Delay Product (PDP) is higher for ISE MOSFET followed by SON MOSFET and ISESON MOSFETs due to the lower delay and power dissipation of the device.

The static power dissipation \( (P_{\text{sat}}) \) which mainly depends on the leakage current \cite{Arora07} of the device is also lower in ISESON MOSFET in comparison to SON MOSFET and ISE MOSFETs.

### 4.12 Immunity Against Interface Charges

Long term reliability is also a major source of concern for nanoscale MOSFET. In ideal conditions, it is assumed that no traps or interface states exist at the interface of silicon and silicon dioxide layer. However in real device, the Si/SiO\(_2\) interface and bulk silicon dioxide is far away from being electrically neutral. Some defects are present at the interface of the Si/SiO\(_2\), resulting in accumulation of positive/negative charges or fixed charges trapped within the oxide region \cite{Putra08}. These charges are either positive or negative and affect the device performance i.e. either enhances or degrades. These interface charges are induced because of various damages such as: 1) fabrication process induced damage 2) stress induced damage and 3) hot carrier induced damage \cite{Djeffal09}. 
Due to high electric field at the drain side, hot carrier effect becomes major source of interface charges at the Si/SiO$_2$ interface layer. These hot carriers are injected into the gate oxide region, thereby showing localized interface states and oxide charges near the drain side. The electrostatic properties of the device may also get altered due to the presence of these interface state density [Kang08] [Ioannidis11]. If the acceptor type trap charge is located at the interface of the Si/SiO$_2$ layer then it accept an electron from the channel region, and thus acts as negative fixed charge region. Reverse phenomenon is observed in case of positive fixed charges [Kumari13c]. In the present analysis, uniform distribution of fixed/interface charges is considered at the interface of the Si/SiO$_2$ layer.

The device reliability issues in terms of the interface charges which may be present at the interface of the SiO$_2$/Si layer is of paramount importance for device dimensions below sub-90 nm regime. The impact of these interface charges on device performance has been studied in this sub-section by analysing analog and digital performance metrics in terms of maximum trans-conductance ($g_{mmax}$), trans-conductance generation efficiency ($g_m/I_{ds}$), output resistance ($R_{out}$), early voltage ($V_{ea}$), Voltage Transfer Characteristics (VTCs), inverter delay, power dissipation ($P_d$) and Power Delay Product ($PDP$) of the CMOS inverter circuit at 22 nm channel length. Three different cases of interface charges are discussed in this section and these are:

- **Case I)** presence of positive fixed charges ($N_f=2 \times 10^{12} \text{cm}^{-2}$).
- **Case II)** ideal case i.e. no charges are present ($N_f=0$).
- **Case III)** Presence of negative fixed charges ($N_f=-2 \times 10^{12} \text{cm}^{-2}$).

As shown in Table 4.06, degradation in $I_{on}/I_{off}$ ratio with interface charges is lesser in ISESON (21.6%) MOSFET as compared to the ISE (33.3%) MOSFET and SON (58.5%) MOSFET. The change in other analog performance metrics because of interface charges such as $g_{mmax}$, $g_m/I_{ds}$, $R_{on}$, $V_{ea}$, and $R_{out}$ is also lower in ISESON MOSFET as compared to other devices. For improved analog performance these figure of metrics should be as high as possible (except on-state resistance $R_{on}$) and also the degradation caused by the interface charges should be minimum. The negative charge at the interface of Si/SiO$_2$ layer degrades the device performance but the change is marginal in ISESON MOSFET as compared to ISE MOSFET and SON MOSFET. This is because, the presence of insulating layers at the side walls and
underneath the channel region reduces the band bending caused by interface charges present at the drain side.

Table 4.06 Impact of Interface trap charges on the analog and digital performance of the different devices for $L=22\ \text{nm}$, $t_{ox}=8\ \text{nm}$, $t_{box}=8\ \text{nm}$, $N_{it}=1\times10^{23}\ \text{m}^{-3}$, $N_{sub}=2\times10^{24}\ \text{m}^{-3}$, $T_s=10\ \text{nm}$, $X_s=2\ \text{nm}$ and $V_{ds}=0.5\ \text{V}$ [Kumari13b].

<table>
<thead>
<tr>
<th></th>
<th>ISESON MOSFET</th>
<th>SON MOSFET</th>
<th>ISE MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Case I</td>
<td>Case II</td>
<td>Case III</td>
</tr>
<tr>
<td>$I_{on}\times10^{-7}\text{(A)}$</td>
<td>8.24</td>
<td>7.99</td>
<td>6.71</td>
</tr>
<tr>
<td>$I_{off}\times10^{-10}\text{(A)}$</td>
<td>2.19</td>
<td>1.63</td>
<td>1.04</td>
</tr>
<tr>
<td>$I_{on}/I_{off}\times10^6$</td>
<td>3.76</td>
<td>4.9</td>
<td>6.45</td>
</tr>
<tr>
<td>$g_{max}\ (mS)$</td>
<td>1.38</td>
<td>1.39</td>
<td>1.41</td>
</tr>
<tr>
<td>$R_{on} \ (K\Omega)$</td>
<td>4.20</td>
<td>4.24</td>
<td>4.19</td>
</tr>
<tr>
<td>$R_{off} \ (K\Omega)$</td>
<td>1.2</td>
<td>1.3</td>
<td>1.4</td>
</tr>
<tr>
<td>$V_{dd} \ (V)$</td>
<td>3.34</td>
<td>3.26</td>
<td>3.10</td>
</tr>
<tr>
<td>$g_{m}/I_{ds} \ (V^{-1})$</td>
<td>26.46</td>
<td>27.35</td>
<td>28.25</td>
</tr>
<tr>
<td>$NM$</td>
<td>0.219</td>
<td>0.214</td>
<td>0.207</td>
</tr>
<tr>
<td>$P_{dyf} \ (\mu W)$</td>
<td>14.9</td>
<td>13.9</td>
<td>8.76</td>
</tr>
<tr>
<td>$Delay \ (ps)$</td>
<td>1.68</td>
<td>1.89</td>
<td>2.86</td>
</tr>
<tr>
<td>$PDP \ (fJ)$</td>
<td>25.03</td>
<td>26.27</td>
<td>25.05</td>
</tr>
</tbody>
</table>

The impact of interface charges on the digital performance of different devices is also given in Table 4.06. From the results, it can be observed that the influence of interface charges on the noise margin ($NM$) is also marginal in ISESON MOSFET. Thus, higher $I_{on}/I_{off}$ ratio and higher noise margin ($NM$) along with the better immunity against interface charges of ISESON MOSFET proves its efficacy as a better candidate for fast switching applications as compared to other devices. The propagation delay and dynamic power dissipation ($P_{dyf}$) which depends mainly on on-state current ($I_{on}$) and $C_{gg}$ (also on other parameters) is also lower in ISESON MOSFET as compared to the other devices i.e. ISE and SON MOSFET.

The presence of positive (negative) interface charges increases (decreases) the delay of the inverter circuit however this will also reduces (increase) the power dissipation because of the lower (higher) leakage current of the device. Thus the overall power
delay product ($PDP$) of the device remains approximately same for both positive and negative interface charges and is marginally lower than the device having no interface charges. The power delay product of SON and ISE MOSFET is significantly higher as compared to ISESON MOSFET due to the higher power dissipation and delay of the circuit. Thus ISESON MOSFET is less susceptible to the degradation caused by the interface charges as compared to other devices.

### 4.13 Summary

The static and dynamic performance of CMOS inverter for different devices has been investigated in this chapter using ATLAS 3D device simulator. The dependency of $VTC$ and noise margin of the inverter circuit, on the various parameters like supply voltage and operating temperature which plays a vital role in designing small sized VLSI circuits was also investigated. Results reflect that ISESON MOSFET shows better tolerance towards parametric variation as compared to other devices. It was also observed that ISESON MOSFET has potential to boost the speed of the device due to smaller propagation delay and is also more reliable as compared to other devices. The advantage of ISESON MOSFET in terms of the performance of logic circuits such as NAND, NOR and ring oscillator has also been studied. The improved performance of ISESON based inverter is due to the smaller sub-threshold slope ($S$), lower leakage current ($I_{off}$), and smaller *Drain Induced Barrier Lowering* effect of the device. The immunity of the ISESON MOSFET against process variation is also investigated.

Flip-Flop circuit using ISESON MOSFET also shows lower propagation delay as compared to SON and ISE based circuits due to the lower parasitic capacitance optimized at the same channel length. However there is a trade-off between $PDP$ and power dissipation of the ISE and SON MOSFET due to the higher $I_{on}$ in case of SON MOSFET as compared to ISE.

Thus, it can be concluded that ISESON MOSFET is a better candidate for low-voltage-low-power digital application as compared to other devices. The vertical isolation provided by the buried layer in ISESON MOSFET protects the thin active silicon layer from radiation-induced photocurrents and also show latch-up immunity.
On the other hand, the lateral isolation also makes inter-device separation in SON free of complicated schemes like trench or well formation. After investigating the impact of insulating layers on the performance of single gate architecture, the next chapter explores the potential of insulating layers/dielectric pockets to enhance the performance of double gate MOSFET.
4.14 References


Chapter 4 Performance Investigation of ISESON MOSFET for Low Voltage Digital ...


