CHAPTER 5

SUMMARY OF APPLICATIONS
5.1 Introduction

The dynamics of submicron CMOS design has made delay estimation and power usage the two important concerns. As the design of power sensitive high speed products accelerate, so does the need for the design software that can help designers estimate and reduce the power consumed by an integrated circuit (IC) early in the design cycle.

Like most trends, integrated circuits have grown so big and so fast that the power dissipated during the operation cannot be ignored. Design teams contend with the impact on system power planning, on the packaging and cooling infrastructure, and on the power — and — ground network, which must pipe current to the actual silicon devices.

Market trends compound the issue. Fast growth markets like medical products are among the most likely to have power concerns. There is a shift from application specific integrated circuits to application specific standard parts. An ASIC is locked into a dedicated system — if the chip exceeds its power budget, the designer can often negotiate an allowance from the system architect.

However, the same over power chip, designed as an ASSP for multiple customers, may well lose business — those customers with power concerns may leave, reducing the overall market for the chip. A similar dynamic applies to intellectual property (IP) cores intended for reverse in multiple 80c ICs.

Lower voltage silicon no longer provides the relief for power problems it once did. Power usage continues to increase despite silicon technology improvements. The growing use of the same silicon technology means it is less
effective for the market problem. As a result, design teams look increasingly to design and design tools as a way to manage power. Function and performance are determined through design, so why not power? Like function and performance, the largest impact on IC power is found early in the design process, at the architectural and register transfer levels.

Most designers today handle power the way they handled timing issues — imprecise estimates early in the design, followed by detailed verification just before tape-out. This approach works as for simple ICs. Since most of the power in complex ICs is determined in the architecture, by the time the detailed verification finds the problem, it's too late to do anything, except to add fans, heat pipes or exotic packaging.

The solution lies at the beginning of the design flow and not at the end. Designers need to identify and fix power problems early. Designers should partition the circuit design into smaller manageable pieces, reducing the time to design, verify and implement the design. Partitioning also helps designers to achieve circuit performance improvements by applying design planning techniques and analyzing the results of their planning early in the design process. Analytical techniques detailed in the previous chapters will help circuit designers to estimate signal delay and short circuit power dissipation. The macromodels will help circuit designers to get a first hand estimate to meet timing and power specification — early in the design process when changes are inexpensive and don't impact the project schedule. The macromodels being
process and physics based help designers to chose the best circuit architecture for a particular CMOS technology.
5.2 Device Speed

The function of a device in a logic gate is to respond to input signals by initiating an electrical pulse on a wire. Some time is required between the receipt of the input and the transmission of an output, during which charges and potentials in the device readjust to the new set of terminal conditions. A device on a logic chip must control the current that charges a load capacitance. A delay of the form charge / current is increased before the signal at a following device switches it. The performance of a logic gate on a chip takes account of this through a delay equation of the form,

\[ t_D = Z + X C_w + y f_0 \]  

(5.1)

where \( C_w \) is the wire capacitance driven by the gate and \( X \) is a constant that is essentially the signal voltage divided by the current supplied by the gate; the term represents the trade-off between speed and power. \( f_0 \) is the fan out and \( y \) includes the input capacitances of the receiving gates as a factor. \( Z \) is a constant that represents delays within the devices of the switching gate, and may also depend weakly on the fan-in to the gate.

In this thesis, a simple analytical, process and layout based model of the delay equation is derived in Chapter 3 for various capacitive loads. A natural extension of this model would be to develop a delay model for series connected
MOSFETS. Section 5.3 derives a delay model for series connected MOSFETs using the Klaassen's MOSFET model, a precursor of the PREDICTMOS model.
5.3 Delay Through Series Connected MOSFETS

5.3.1 Introduction

A series connected MOSFET structure (SCMS) has been analysed using a small geometry, physical MOSFET model – Klaassen’s model [5.3.1]. The result shows the relation of physical parameters on delay of submicron CMOS gates. The results are compared with that obtained by using the RC based model [5.3.4]. An analytical expression derived from a short channel MOS model (Klaassen’s model) gives an insight into the physical parameters affecting the propagation delay. Analytical expressions can also be solved much faster than circuit simulators with as much accuracy. Sakurai and Newton have used an empirical model to obtain delay expressions for SCMS (series connected MOSFET structure) [5.3.2]. However the model used i.e \( n^{th} \) Power Law model is empirical and not as easily scalable as Klaassen’s model. Merino, Bota and Samities have tried to derive some data and information using controlled experiments [5.3.3].

Klaassen’s model: The following current equations from Klaassen’s model are used

\[
I_{DLIN} = \frac{\beta \left[V_{GS} - V_{TN} - \frac{\alpha_i}{2} V_{DS} \right] V_{DS}}{1 + \frac{V_{DS}}{LE_C}} \quad \text{when } V_{DS} < V_{DSAT} \quad (5.2)
\]

where \( \beta \) is the transconductance parameters, \( V_{GS} \) is the gate source voltage, \( V_{TN} \) is the threshold voltage, \( V_{DS} \) is the drain – source voltage, \( \alpha_i \) is the square root

145
approximation parameter, \( E_C \) is the critical electric field, \( L \) is the effective length of the MOST and \( I_{DLIN} \) is the current in the linear region.

and,

\[
I_{DSAT} = \beta L [V_{GS} - V_T - \alpha V_{DSAT}] E_P \left( \frac{E_P}{E_C} \right) \quad \text{when } V_{DS} \geq V_{DSAT}
\]  

(5.3)

where \( I_{DSAT} \) is the current in the saturation region of operation of the MOST and \( E_P \) is a geometry and bias independent parameter characterizing the electric field in the region where the gradual channel approximation is no longer valid.
5.3.2 Delay Expression of Series Connected MOSFET Structure:

The circuit whose delay is to be calculated is shown in Fig. 5.1.

![Circuit Diagram](image)

**Fig. 5.1:** MOSTs are connected in series discharge a capacitive load.

The delay of simple gates connected in series may be approximated by macromodelled by constructing an 'equivalent inverter'. The effective $\beta$ of the two transistors is given by,

$$\beta = \frac{1}{\frac{1}{\beta_1} + \frac{1}{\beta_2}}$$  \hspace{1cm} (5.4)

The fall time of the equivalent inverter for a step input is the time required to discharge a load capacitance $C_L$ from 90% to 10% of its steady state value.

Fig 5.2 shows a CMOS inverter with a capacitive load $C_L$ that represents the capacitance of the input of the next gates, output of this gate and routing. The fall time can be considered to be divided into two periods:

a. $t_{sat}$ = period during which the capacitor voltage, $V_{out}$, drops from 0.9 $V_{DD}$ to $V_{DSAT}$. 

147
b. \( t_{\text{in}} \) = period during which the capacitor voltage, \( V_{\text{out}} \), drops from \( V_{\text{DSAT}} \) to 0.1 \( V_{\text{DD}} \).

The behaviour of the circuit is described by the differential equation.

\[
\frac{dV_{\text{out}}}{dt} - t_{\text{sat}} \frac{V_{\text{out}}}{V_{\text{DSAT}}} = I_D
\]

where \( V_{\text{out}} \) is the output voltage, \( C_L \) is the capacitive load, \( t \) is the time and \( I_D \) is the drain current.

The period during which the capacitor voltage discharges from 0.9\( V_{\text{DD}} \) to \( V_{\text{DSAT}} \) is given by,

\[
t_{\text{sat}} = C_L \int_{V_{\text{DSAT}}}^{V_{\text{DD}}} \frac{1}{I_{\text{DSAT}}} dV_{\text{out}}
\]

Solving equation (5.6) we have,
\[ t_{\text{sat}} = \frac{C_L}{I_{DSAT}} (V_{DD} - V_{DSAT}) \]  
(5.7)

where \( I_{DSAT} \) is given in equation (5.3) and,

\[ V_{DSAT} = L_{\text{eff}} E_C \left[ \sqrt{1 + \frac{2(V_{GS} - V_T)}{\alpha L_{\text{eff}} E_C} - 1} \right] \]

The period during which the capacitor voltage discharges from \( V_{DSAT} \) to 0.1\( V_{DD} \) is given by,

\[ t_{\text{lin}} = C_L \int_{0.1V_{DD}}^{V_{DSAT}} \frac{1}{I_{\text{DLIN}}} dV_{\text{out}} \]  
(5.8)

solving equation (5.8) we get,

\[ t_{\text{lin}} = \frac{C_L}{\beta u_{\text{sat}}} \left[ \ln |V_{\text{DSATN}}| \alpha - 2u_{\text{sat}} \ln |\alpha V_{\text{DSATN}} - 2u| - \alpha \ln |\alpha V_{\text{DSATN}} - 2u| \right] \]

(5.9)

where,

\[ a = L_{\text{eff}} E_C; \]
\[ u = V_{DD} - V_{TN}; \]

rewriting equation (5.9) as,

\[ t_{\text{lin}} = \frac{C_L}{\beta u_{\text{sat}}} \left[ \frac{- (\alpha a - 2g) \log_e |\alpha 0.1V_{DD} - 2u| - \frac{(2u + aa)}{\beta u a}}{\beta u a} \right] \]

(5.10)
5.3.3 Results

The fall time, calculated by adding $t_{\text{sat}}$ and $t_{\text{lin}}$ from (5.7) and (5.10), is compared with a SCMS using SPICE model 3. Analytical equations give results much faster than SPICE 3 and also provide physical insight into the process parameters. The results are shown in Table 5.1.

Table 5.1

Fall Times of Our Model Compared to SPICE 3 for varying $C_L$

<table>
<thead>
<tr>
<th>Capacitive Load $C_L$</th>
<th>Fall Time (Our Model) (ns)</th>
<th>Fall Time (SPICE 3) (ns)</th>
<th>Error %</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 fF</td>
<td>0.12 ns</td>
<td>0.16 ns</td>
<td>25</td>
</tr>
<tr>
<td>100 fF</td>
<td>0.24 ns</td>
<td>0.25 ns</td>
<td>5.4</td>
</tr>
<tr>
<td>250 fF</td>
<td>0.6 ns</td>
<td>0.53 ns</td>
<td>-13</td>
</tr>
<tr>
<td>0.5 pF</td>
<td>1.6 ns</td>
<td>0.99 ns</td>
<td>-22</td>
</tr>
</tbody>
</table>

The Table 5.2 compares the signal propagation delay obtained by using (5.7) as against the RC model. In the delay equation, $V_{\text{DSAT}}$ in (5.7) is replaced by $V_{\text{DD}}/2$.

Table 5.2

Comparison of Signal Propagation Delay of Our Model with other Models

<table>
<thead>
<tr>
<th>$C_L$</th>
<th>$T_d$ (RC Model)</th>
<th>$T_d$ (Spice 3)</th>
<th>Error %</th>
<th>Error % (RC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 fF</td>
<td>0.12</td>
<td>0.13</td>
<td>7</td>
<td>39</td>
</tr>
<tr>
<td>150 fF</td>
<td>0.18</td>
<td>0.17</td>
<td>-6</td>
<td>30</td>
</tr>
<tr>
<td>200 fF</td>
<td>0.24</td>
<td>0.21</td>
<td>-14</td>
<td>23</td>
</tr>
</tbody>
</table>

The table shows that as the $C_L$ increases, the delay value using (5.7) is more than that given by SPICE 3. The input capacitance of such a SCMS is 68 fF and the delay has been measured for upto 3 times the input capacitance.

For larger capacitances the equivalent inverter of the SCMS operates in the linear part of the circuit and therefore (5.10) is more valid for delay prediction.
Secondly the linear region piece dominates the discharge time (i.e. it is 34% larger than the saturation piece).

Hence the delay equation for large capacitive loads can be written as,

\[ T_d = \frac{C_L(W_1 + W_2)}{C_{OX}W_1W_2v_sN(V_{DD} - V_{TN})} \left[ \log_{e} |V_{DD}0.9(\alpha - 2(V_{DD} - V_{TN})\log_{e}\alpha(0.9V_{DD} - 2(V_{DD} - V_{TN}))| - \alpha \log_{e}(\alpha(0.9V_{DD} - 2(V_{DD} - V_{TN})) - \alpha \log_{e}\left| \frac{V_{DD}}{2} \right| + 2\log_{e} \left( \frac{\alpha V_{DD}}{2} - 2(V_{DD} - V_{TN}) \right) \right] \]

(5.11)

where \( T_d \) is the propagation delay, \( v_s \) is the saturation velocity and \( N \) is the number of inverters. The equation (5.11) assumes that all inverters in the SCMS are of the same length.

Physical Interpretation: From (5.11) we can infer the following:

i. When \( L \) increases, the equivalent transistor resistance increases. In order to minimize delay, the \( L \) parameter must be the minimum gate length of the chosen technology.

ii. As the width increases, the delay reduces proportionately. However the capacitance increases and therefore the width of the transistor has a complex relationship with the propagation delay.

Is there an optimum width design which gives the minimum propagation delay?

The propagation delay model expressed as (5.11) is used for plotting curves shown in Figure 5.3 and Figure 5.4.
Figure 5.3 shows that as the width of the transistors in series is increased the propagation delay reduces.

The relationship of the width of the topmost transistor with the delay, keeping the widths of all other MOST's in the circuit constant, is convex showing that the width of the topmost transistor can be optimized for minimum delay.

**Fig. 5.3 : Progressive increase in Width of SCMS Vs Propagation Delay**

**Fig. 5.4: Optimization of Topmost MOST for Minimum Propagation Delay**
5.3.4 Summary

A propagation delay model of short channel series connected MOSFETs is derived. The expression has a physical basis, is scalable and convenient for designers to understand the parameters affecting delay in series connected MOSFETs. The parameters for transistor sizing and design of MOSFETs in series to minimize delay are demonstrated.
5.3 References


5.4 Comparative Evaluation of the Schmitt Trigger Architecture

5.4.1 Introduction

The section evaluates three Schmitt Trigger architecture's under three headings:-

5.4.1 Ease of designing

5.4.1 Propagation delay

5.4.1 Short circuit power dissipation

The Schmitt Trigger of D. Kim, Kih and W Kim (KST) is shown to be the architecture with minimum delay and short circuit power dissipation compared to the Conventional Schmitt Trigger (CST) and the Schmitt Trigger designed by M. Steyaert and W. Sansen (SSST).

<table>
<thead>
<tr>
<th>NOTATIONS</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \mu_{SNC} )</td>
<td>Surface mobility of NMOST</td>
</tr>
<tr>
<td>W</td>
<td>Width of the MOST</td>
</tr>
<tr>
<td>L</td>
<td>Effective Length of MOST</td>
</tr>
<tr>
<td>( V_s )</td>
<td>Velocity Saturation</td>
</tr>
<tr>
<td>( V_{THN} )</td>
<td>Threshold voltage of NMOST</td>
</tr>
<tr>
<td>( V_{THP} )</td>
<td>Threshold voltage of PMOST</td>
</tr>
<tr>
<td>( V_{DSATN} )</td>
<td>Saturation voltage of NMOST</td>
</tr>
<tr>
<td>( V_{DSATP} )</td>
<td>Saturation voltage of PMOST</td>
</tr>
<tr>
<td>( C_{OX} )</td>
<td>Gate Oxide Capacitance per unit area</td>
</tr>
<tr>
<td>( V_{SPH} )</td>
<td>Upper Switching Voltage</td>
</tr>
<tr>
<td>( V_{SPL} )</td>
<td>Lower Switching Voltage</td>
</tr>
<tr>
<td>( V_{SB} )</td>
<td>Source – Bulk Voltage</td>
</tr>
<tr>
<td>( V_{DS} )</td>
<td>Drain – Source Voltage</td>
</tr>
<tr>
<td>( ECP )</td>
<td>Critical Electric Field of PMOST</td>
</tr>
<tr>
<td>( ECN )</td>
<td>Critical Electric Field of NMOST</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>Parameter of Square Root Approximation</td>
</tr>
</tbody>
</table>

The Schmitt Trigger is a circuit that converts a varying voltage into a stable logical signal. A Schmitt Trigger architecture which gives a guaranteed
hysteresis under large process variation, has a DC transfer characteristic which is insensitive to noise and other disturbances and which can be designed so as to accurately determine the switching points is an ideal Schmitt Trigger.

A comparison of three Schmitt Trigger architectures is done in the present communication to determine which architecture comes closest to the ideal Schmitt Trigger.

The CST is perhaps the most common Schmitt Trigger architecture whose design methodology has been well discussed in many textbooks [5.4.1], [5.4.2]. M. Steyaert and W. Sansen suggested a better architecture with better prediction of the switching points and a better immunity to process variations [5.4.3]. D. Kim, J.Kih and Wochan Kim introduced an alternative approach to Schmitt Trigger design involving the ratioless circuit design concept wherein the process and supply voltage variations do not affect the hysteresis feature [5.4.4].

5.4.2 Design Methodology of the Three Schmitt Trigger’s

The architecture of the conventional Schmitt trigger is shown in Fig 5.5 below. Let $V_{in}$ be at 0V, hence the $V_{out}$ is high at $V_{DD}$. Therefore the MOST M3 is ON and the voltage at $V_x$ is $V_{DD} - V_{THN}$. MOST’S M4 and M5 are ON and MOST’S M1 and M2 are OFF. Due to the body effect the voltage of the MOST M2 will now be increased to $(V_{THN2} + V_x)$. $V_{SPH}$ is the switching voltage at which the output is pulled down to zero. As the input voltage rises and reaches $V_{SPH} = V_{THN}$, the transistor M1 is switched ON. The voltage at $V_x$ is pulled down. At this point, the
current through MOST M1 and MOST M3 are equal and by using the PREDICTMOS model can be written as:

\[
\frac{\mu_{\text{IN}} W C_{\text{OX}}}{L + \frac{\mu_{\text{IN}}}{V_s} V_x} \left[ \left( V_{\text{SPH}} - V_{\text{THN1}} - \frac{a_i}{2} V_{\text{DSATN1}} \right) V_{\text{DSATN1}} + \left( V_{\text{SPH}} - V_{\text{THN1}} - a_i V_{\text{DSATN1}} \right) V_{x} - V_{\text{DSATN1}} \right]
\]

\[
= -\frac{\mu_{\text{IN}} W C_{\text{OX}}}{L + \frac{\mu_{\text{IN}}}{V_s} (V_{\text{DD}} - V_x)} \left[ \left( V_{\text{DD}} - V_x - V_{\text{THN3}} - \frac{a_i}{2} V_{\text{DSATN3}} \right) V_{\text{DSATN3}} + \left( V_{\text{DD}} - V_x - V_{\text{THN3}} - a_i V_{\text{DSATN3}} \right) V_{\text{DD}} - V_x - V_{\text{DSATN3}} \right]
\]

(5.12)

It is known that,

\[ V_{\text{SPH}} = V_{\text{THN2}} + V_x; \]

or,

\[ V_x = V_{\text{SPH}} - V_{\text{THN2}}; \]

and,

\[ V_x = V_{\text{DD}} - V_{\text{THN3}}; \]
we use an approximation, wherein

$$V_{THN1} = V_{THN3} = V_{THN}$$  \hspace{1cm} (5.13)

else (5.12) is unsolvable. This ratio of widths of the transistors M1 and M3 for a particular $V_{SPH}$ is given by,

$$\frac{W_i}{W_j} = \mu_{SN3} \left[ \frac{L + \mu_{SN1}}{V_{DSATN3}} (V_{DD} - V_{THN1}) \right] \left[ (V_{DD} - V_{SPH} - \frac{a}{2} V_{DSATN3}) V_{DSATN3} + 
(V_{DD} - V_{SPH} - a_i V_{DSATN3} + V_{TIN3} - V_{DSATN3}) \right]$$

$$\frac{W_i}{W_j} = \mu_{SN1} \left[ \frac{L + \mu_{SN3}}{V_{DSATN1}} (V_{DD} - V_{SPH} - V_{THN1}) \right] \left[ (V_{SPH} - V_{THN1} - \frac{a}{2} V_{DSATN1}) V_{DSATN1} + 
(V_{SPH} - V_{THN1} - a_i V_{DSATN1} + V_{DD} - V_{THN1} - V_{DSATN1}) \right]$$  \hspace{1cm} (5.14)

The approximation made above results in an error because we would be neglecting the effect of $V_{SB}$ and $V_{DS}$ on the threshold voltage. The above derivation utilizes the current equation of the small geometry MOSFET model PREDICTMOS. The ratio of the widths of the MOST5 and MOST6 for a particular $V_{SPL}$ is also obtained in a similar manner as above. The currents through MOST5 and MOST6 are the same and so by using the PREDICTMOS model we have,

$$\frac{\mu_{SP5} W_{C} C_{O}}{L_x + \mu_{SP5} V_{DSATP5} (V_x - V_{DD})} \left[ (V_{SP5} - V_{DD} - V_{THP5} - \frac{p}{2} V_{DSATP5} V_{DSATP5} + \frac{q}{2} V_{DSATP5} V_{DSATP5} (V_x - V_{DD} - V_{DSATP5}) = 
(V_{SP5} - V_{THP5} - \frac{q}{2} V_{DSATP5} V_{DSATP5} (V_x - V_{THP5} - \frac{q}{2} V_{DSATP5} V_{DSATP5} (V_x - V_{DSATP5})) \right]$$

$$\frac{\mu_{SP6} W_{C} C_{O}}{L_x + \mu_{SP6} V_{DSATP6} (V_x - V_{THP6})} \left[ (V_{SP6} - V_{THP6} - \frac{q}{2} V_{DSATP6} V_{DSATP6} (V_x - V_{THP6} - \frac{q}{2} V_{DSATP6} V_{DSATP6} (V_x - V_{DSATP6})) \right]$$  \hspace{1cm} (5.15)

where $V_{SPL}$ is the input voltage at which the output voltage goes high. It can be seen that

$$V_x = -V_{THP}$$

and,
From (5.15),

\[
W_{PS} = \frac{\mu_{SPL}\left(L_p + \frac{\mu_{SPL}}{\mu_{SPL}} (V_{TP} - V_{SPL})\right)}{W_{PS}} \left[ -\frac{V_{SPL}}{2} - \frac{V_{DSATP6}}{2} \right] + \\
\left[ -\frac{V_{SPL}}{2} - \frac{V_{DSATP6}}{2} \right] V_{THP} - V_{SPL} - V_{DSATP6}
\]

(5.16)

5.4.3 Design Methodology of KST:

The switching voltage of the inverter is determined by obtaining the ratio of the transconductances of the 2 MOSFET's forming the CMOS inverter. The ratio of
the widths of the transistors forming the CMOS inverter for a particular switching voltage $V_{sp}$, using the PREDICTMOS model is given by,

$$W_N = \frac{-\left[ E_{cp} \left( -\alpha_p (V_{DSATP})^2 - 2(V_{SP})^2 + 2V_{DD} V_{SPH} \right) \mu_p E_{CP} \left( L_N E_{CN} + V_{SP} \right) \right]}{\left[ (L_p E_{CP} + V_{SP}) \mu_p E_{SN} E_{CN} \left( \alpha_N (V_{DSATN})^2 + 2(V_{SP})^2 - 2V_{TN} V_{SP} - 2\alpha_N V_{DSATN} V_{SP} \right) \right]}$$

(5.17)

MOSFETs M5 and M6 are designed using the ratio less circuit design concept. The MOST's M1, M2, M3 and M4 are designed by rationed logic using equation (5.17). Hence, the sizes of MOST's M5 and M6 do not affect the switching voltages. Also these gates can be laid out in a very small area and the outputs can swing from $V_{DD}$ to ground.

5.4.4 Design Methodology of SSST

This SSST requires the least number of transistors. The $V_{SPH}$ of the Schmitt Trigger is the switching point of the inverter formed by transistors M1 and M2. The VSPL calculation includes the MOST M3 as an additional current drain which is responsible for the hysteresis. The ratio of the widths of MOST's M2 & M1 & M5 & M4 to obtain the upper trip point ($V_{SPH}$) are,

$$W_N = \frac{-\left[ E_{cp} \left( -\alpha_p (V_{DSATP})^2 - 2(V_{SP})^2 + 2V_{DD} V_{SPH} + 2V_{THP} V_{SPH} + 2\alpha_p V_{DSATP} V_{SPH} \right) \mu_p (L_N E_{CN} + V_{SP}) \right]}{(L_p E_{CP} + V_{SP} - V_{DD}) \mu_p E_{SN} E_{CN} \left( \alpha_N (V_{DSATN})^2 + 2(V_{SP})^2 - 2V_{THN} V_{SPH} - 2\alpha_N V_{DSATN} V_{SPH} \right)}$$

(5.18)

Once the ratio is determined the sizes of MOST's M1, M2, M4 and M5 can be determined. The architecture of the Schmitt Trigger is shown in Fig. 5.7,
The size of the M3 inorder to lower the switching point to $V_{SPL}$ is determined as given below:

A. The current passing through MOST M1 is sunk by MOST's M2 and M3.

B. The current through MOST M1 is equal to the current through M2 and M3 together.

C. From (5.18) the current through MOST's M1 and M2 can be determined at $V_{SPL}$.

Therefore the width of the transistor M3 is determined as follows:

$$\frac{\mu_{SM}W_3C_{ox}}{L + \mu_{SS}/V_S} \left[ \left( V_{DD} - V_{THN} - \frac{a_i}{2} V_{DSATN} \right) V_{DSATN} + (V_{DD} - V_{THN} - a_i V_{DSATN}) (V_{DS} - V_{DSATN}) \right]$$

$$= I_{DSATPM1} - I_{DSATNM2} = I_{DS(diff)}$$

(5.19)

By putting $V_{DS} = 0$. 

161
\[ W_s = \frac{I_{DS(diff)} (L + \mu S / \nu_s) V_{DS}}{\mu S C_{ox} \left( \frac{V_{DD} - V_{THN} - \frac{\alpha}{2} V_{DSATN}}{V_{DSATN}} \right) V_{DSATN} + \left( \frac{V_{DD} - V_{THN} - \alpha V_{DSATN}}{V_{DSATN}} \right) V_{DSATN} } \] (5.20)

\[ I_{DSATPM1} = \frac{\mu_{SN2} W_{N2} C_{OX}}{L_{N2}} \left[ \left( \frac{V_{SPH} - V_{DP} - V_{TP1} - \frac{\alpha}{2} V_{DSATP}}{V_{SPH}} \right) V_{DSATP} + \left( \frac{V_{SPH} - V_{DP} - V_{TP1} - \alpha V_{DSATP}}{V_{SPH}} \right) V_{DSATP} \right] \]

where,
\[ V_{TP1} = V_{THP} - 2.5 \eta (V_{DD}) \]

\[ I_{DSATPM2} = \frac{\mu_{SN2} W_{N2} C_{OX}}{L_{N2}} \left[ \left( \frac{V_{SPH} - V_{THN} - \frac{\alpha}{2} V_{DSATN}}{V_{SPH}} \right) V_{DSATN} + \left( \frac{V_{SPH} - V_{THN} - \alpha V_{DSATN}}{V_{SPH}} \right) V_{DSATN} \right] \]

**5.4.5 OBSERVATION:**

I. CST: The CST was designed using the design equations detailed above.

The accuracy of predicting the switching point was observed using the SPICE model 3, as depicted in Table 5.3.

Table 5.3

<table>
<thead>
<tr>
<th>Width of M3</th>
<th>$V_{SPH}$</th>
<th>$V_{SPH}$ (SPICE 3)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 µ</td>
<td>2.75 V</td>
<td>3 V</td>
<td>5 %</td>
</tr>
<tr>
<td>16 µ</td>
<td>3.89 V</td>
<td>4 V</td>
<td>3 %</td>
</tr>
</tbody>
</table>

Width of M1=3µ and M2=15µ.

<table>
<thead>
<tr>
<th>Width of MOST 5</th>
<th>Width of MOST 6</th>
<th>$V_{SPH}$</th>
<th>$V_{SPH}$ (SPICE 3)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9 µ</td>
<td>14 V</td>
<td>1</td>
<td>0.68</td>
<td>32 %</td>
</tr>
<tr>
<td>10 µ</td>
<td>156 V</td>
<td>1</td>
<td>0.73</td>
<td>27 %</td>
</tr>
<tr>
<td>20 µ</td>
<td>311 µ</td>
<td>1</td>
<td>0.75</td>
<td>25 %</td>
</tr>
<tr>
<td>0.9 µ</td>
<td>1 µ</td>
<td>2</td>
<td>1.24</td>
<td>36 %</td>
</tr>
<tr>
<td>10 µ</td>
<td>11 µ</td>
<td>2</td>
<td>1.9</td>
<td>5 %</td>
</tr>
<tr>
<td>20 µ</td>
<td>22 µ</td>
<td>2</td>
<td>1.97</td>
<td>1.5 %</td>
</tr>
</tbody>
</table>
Convergence problems were faced and were solved by setting, OPTIONS: ITL 1=300 and ITL 6=100.

II. KST: The Schmitt Trigger was designed and the accuracy of predicting the switching point was observed using SPICE 3, as shown in Table 5.4.

<table>
<thead>
<tr>
<th>WN</th>
<th>WP</th>
<th>VSP</th>
<th>Vint (SPICE 3)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 μ</td>
<td>764 V</td>
<td>4 V</td>
<td>3.87 V</td>
<td>3.25 %</td>
</tr>
<tr>
<td>3 μ</td>
<td>11 V</td>
<td>3 V</td>
<td>2.54 V</td>
<td>15.33 %</td>
</tr>
<tr>
<td>3 μ</td>
<td>1 μ</td>
<td>2 V</td>
<td>1.40 V</td>
<td>30 %</td>
</tr>
</tbody>
</table>

A lot of convergence problems were faced and were solved by setting.

OPTIONS: ITL1 = 300 and ITL6 = 100

The SPICE model was modified to exclude capacitances, DIBL and other secondary effects. In the above table, the Vint is the voltage at the node between the inverters formed by MOST's M1, M2, M3 and M4 and the MOST's M5 and M6. The results are shown in Table 5.5.

<table>
<thead>
<tr>
<th>WN</th>
<th>WP</th>
<th>VSP</th>
<th>Vint (SPICE 3)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 μ</td>
<td>764 V</td>
<td>4 V</td>
<td>3.87 V</td>
<td>3.25 %</td>
</tr>
<tr>
<td>3 μ</td>
<td>11 V</td>
<td>3 V</td>
<td>3.3 V</td>
<td>10%</td>
</tr>
<tr>
<td>3 μ</td>
<td>1 μ</td>
<td>2 V</td>
<td>1.88 V</td>
<td>6 %</td>
</tr>
</tbody>
</table>

III. SSST: Was designed and the accuracy of predicting the switching point was observed using the SPICE model 3, as shown in Table 5.6.
Table 5.6

Predicting the Accuracy of the Switching Point for SSST

<table>
<thead>
<tr>
<th>$W_N$</th>
<th>$W_P$</th>
<th>Width of MOST 5</th>
<th>$V_{SPH}$</th>
<th>$V_{SPL}$</th>
<th>$V_{SPH}$ (SPICE 3)</th>
<th>$V_{SPL}$ (SPICE 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3µm</td>
<td>3932µm</td>
<td>1425µm</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>3µm</td>
<td>3932µm</td>
<td>1425µm</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>0.9µm</td>
<td>1180µm</td>
<td>428µm</td>
<td>4</td>
<td>-</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>0.9µm</td>
<td>1180µm</td>
<td>428µm</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>2.04</td>
</tr>
</tbody>
</table>

Table 5.7 shows the propagation delay of the three Schmitt Triggers for the same capacitive load $C_L=0.5pF$. The delay was calculated for a specific $V_{SPL}$ and $V_{SPH}$ fixed. The $V_{SPH}$ was fixed at 4V and $V_{SPL}$ at 3V. The power supply was $V_{DD} = 5V$. Kim’s circuit has the minimum propagation delay compared to the other two architectures.

Table 5.7

The Propagation Delay of the Three Schmitt Triggers

<table>
<thead>
<tr>
<th></th>
<th>CST</th>
<th>KST</th>
<th>SSST</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_D=(R_{N1}+R_{N2})C_L$</td>
<td>$T_D=R_N C_L$</td>
<td>$T_D=R_N C_L$</td>
<td></td>
</tr>
<tr>
<td>$T_D=1.44$ ns</td>
<td>$T_D=1.2$ ns</td>
<td>$T_D=4$ ns</td>
<td></td>
</tr>
</tbody>
</table>

5.4.6 Discussion

The table 5.8 shows the comparison of the three Schmitt Trigger architectures.
Table 5.8
Comparison of the Three Schmitt Trigger Architectures

<table>
<thead>
<tr>
<th>CST</th>
<th>KST</th>
<th>SSST</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The switching points cannot be accurately determined as the body effect cannot be incorporated suitably.</td>
<td>Design is simple and the switching points can be accurately determined.</td>
</tr>
<tr>
<td>2</td>
<td>Moderate propagation delay.</td>
<td>Minimum propagation delay.</td>
</tr>
</tbody>
</table>

Thus the PREDICTMOS model has been used to design the Schmitt Trigger and an analytical method to compare Schmitt trigger architecture has been described.
5.4 References


5.5 A Physical Submicron MOSFET model Incorporating the Source/Drain Series Resistances and its Application to CMOS Inverter Delay Analysis

5.5.1 Introduction

The PREDICTMOS model – a small geometry, layout and process based MOSFET model is modified to include the parasitic source and drain series resistances. The modified model, which also includes short channel effects like velocity saturation, DIBL, channel length modulation and mobility degradation, becomes the basis to derive a CMOS inverter delay model. The delay model is benchmarked against a robust numerical MOSFET model SPICE 3. The model can predict the delay to within a few percent of the simulated results, while offering a significant gain in CPU time.

The scaling of a MOS transistor has been the major driving force of the growth of the microelectronic industry. As the scaling progresses into the submicron region, the effects of the contact resistances originating from the resistance of the source / drain diffusion islands and from contact imperfections limit the current drive capability of FETs. A MOSFET model incorporating the source / drain series resistance in addition to short channel effect like velocity saturation, DIBL, channel length modulation and mobility degradation, is very useful to a circuit designer. We have borrowed a physics based small geometry MOSFET model ~ PREDICTMOS and modified it to include the source / drain
parasitic resistances[5.5.1]. The modified model is then used to derive a propagation delay model of a submicron CMOS inverter.

Many researchers have developed propagation delay models for submicron CMOS inverters [5.5.2, 5.5.3, 5.5.4, 5.5.5, 5.5.6]. The novelty of this communication is that for the first time we have an analytical, physics based propagation delay model incorporating the effects of source / drain series resistance in addition to other short channel effects.

5.5.2 Derivation of the Current Expression & Propagation Delay Model Incorporating the Source / Drain Series Resistance

The PREDICTMOS model has been the basis on which we have derived the current expression and the propagation delay model. This model has been selected from a number of MOSFET models because

a. The model is physics based and hence the designer can correlate the circuit behavior with parameters obtained from the process and layout data.

b. The model current expression is simple mathematically.

c. The incorporation of channel length modulation into the current expression is efficient and simple.

d. It has a few parameters which can be easily extracted from the process and layout data [5.5.7]. The model parameters can also be extracted from the SPICE 3 and BSIM 3 models [5.5.8].

e. The model being physical is potentially scalable.
The PREDICTMOS model divides the channel into two regions,

A. The region where the Gradual Channel Approximation is valid and

B. A high field region where the GCA breaks down and the gate no
   longer controls the channel.

The current expression of the PREDICTMOS model is:

\[
I_D = \frac{\mu_w W C_{OX}}{L + \frac{\mu_w}{V_s V_D} \left[ (V_{GS} - V_T - \frac{a}{2} V_{DSX}) V_{DSX} \right] \left[ (V_{0S} - V_T - a V_{DSX} V_{DSX}) \right] \left( V_D - V_{DSX} \right)}
\]

where

\[
V_{DSX} = V_D \quad \text{when } V_D < V_{DSAT}
\]
\[
= V_{DSAT} \quad \text{else}
\]

In order to incorporate the drain / source series resistance the following
expression have to be incorporated in (5.21):

\[
V_{gs} = V_{GS} - R_S I_D
\]

\[
V_{ds} = V_{DS} - (R_S + R_D) I_D
\]

Solving the expression (5.21) for \( I_D \), both in the linear and saturation region we
have

\[
I_D = \frac{-y + \sqrt{y^2 - 4X2}}{2X} \quad \text{for } V_d > V_{dsat}
\]

and
The saturation voltage of the MOSFET considering the effect of the parasitic series resistance is:

\[
V_{dsat} = V_{DSAT} - RI_D
\]  
(5.26)

The \(V_{dsat}\) expression including the series resistance is:

\[
V_{dsat} = \frac{-N + \sqrt{N^2 - 4MP}}{2M}
\]  
(5.27)

where,

\[
M = E_p\alpha_t + E_p\alpha_bLECR_S - \alpha_tEC;
\]

\[
N = 2E_C(V_{GS} - V_T) + 2E_p\alpha_tLECEC;
\]

\[
P = 2E_pLEC(V_T - V_{GS});
\]
Using (5.24), (5.25) and (5.27) the I-V characteristics of a MOSFET can be plotted and compared to simulated curves using SPICE 3 model. We can also gauge independently the effects that a change in the source / drain resistance has on the I-V characteristics. It can also be shown that the \( I_d \) and \( V_{dsat} \) expressions revert back to their original expressions when \( R_S = R_D = 0 \).

We use (5.25) to derive the propagation delay model of a CMOS inverter for a step input. The fall time of a CMOS inverter driving a capacitive load \( C_L \), for a step input can be estimated by using the differential equation:

\[
C_L \frac{dV_{ds}}{dt} = -I_d
\]  

(5.28)

Since the NMOS transistor operates in the linear region for a longer period of time, during which the \( V_{ds} \) falls from \( V_{DD} \) to 0, we can substitute (5.25) in (5.28) and solve the differential equation. The time taken for the output voltage to fall from \( V_{DD} \) to half the supply voltage is given by,

\[
t_d = \frac{C_L}{t_s} \left[ \frac{(sv - ut)\log|SV_{DD} + t| - ut\log|2|}{sV_{DD} + 2t} \right]
\]  

(5.29)

where,

\[
s = \beta_i \alpha_i;
\]

\[
t = 2\beta_i (V_T - V_{DD});
\]

\[
u = 2\beta_i R_S + 2b - 2\beta_i \alpha_i R;
\]

\[
v = 2\beta_i R (V_{DD} - V_T) + 2L;
\]
The expression (5.29) is thus a physics based, small geometry MOSFET based propagation delay model incorporating the effect of the parasitic source / drain series resistance. $t_d$ is the signal propagation delay.

5.5.3 Results

The accuracy of expressions (5.24) and (5.25) are shown in Fig. 5.8 where the I-V characteristics are compared to that of the SPICE 3 model. All the current values for various bias conditions are within 5% of the SPICE values. An increase in the source resistance decreases the current in both the linear and saturation regions of the MOSFET operation as shown in Fig. 5.9. A change in the drain resistance affects only the current in the linear region of the MOSFET as shown in Fig. 5.10.

The propagation delay model incorporating the series drain / source resistance is compared with simulated values using SPICE 3 for 0.5\mu CMOS MOSIS technology. The propagation delay of a submicron CMOS inverter for a step input and the minimum channel length of 0.5\mu is compared. Table 5.9 shows the propagation delay obtained with expression (5.29) against the delay obtained with the SPICE 3 model for different channel widths and capacitive loads.
Table 5.9

Comparison of Propagation Delay of a 0.5μ CMOS inverter for varying source / drain series resistance and capacitive loads

<table>
<thead>
<tr>
<th>C_L (fF)</th>
<th>R_S (Ω)</th>
<th>R_D (Ω)</th>
<th>Our Model (S)</th>
<th>SPICE3 (S)</th>
<th>Error %</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>16.7</td>
<td>16.7</td>
<td>4.07e-11</td>
<td>4.55e-11</td>
<td>10.5</td>
</tr>
<tr>
<td>45</td>
<td>33.4</td>
<td>33.4</td>
<td>4.16 e-11</td>
<td>4.66 e-11</td>
<td>10.7</td>
</tr>
<tr>
<td>45</td>
<td>50</td>
<td>50</td>
<td>4.25 e-11</td>
<td>4.8 e-11</td>
<td>11.4</td>
</tr>
<tr>
<td>45</td>
<td>66.7</td>
<td>66.7</td>
<td>4.33 e-11</td>
<td>4.9 e-11</td>
<td>11.6</td>
</tr>
<tr>
<td>45</td>
<td>83.4</td>
<td>83.4</td>
<td>4.42 e-11</td>
<td>5 e-11</td>
<td>11.6</td>
</tr>
<tr>
<td>45</td>
<td>100</td>
<td>100</td>
<td>4.51 e-11</td>
<td>5.1 e-11</td>
<td>11.5</td>
</tr>
<tr>
<td>90</td>
<td>16.7</td>
<td>16.7</td>
<td>8.15 e-11</td>
<td>8.31 e-11</td>
<td>1.9</td>
</tr>
<tr>
<td>90</td>
<td>33.4</td>
<td>33.4</td>
<td>8.32 e-11</td>
<td>8.51 e-11</td>
<td>2.2</td>
</tr>
<tr>
<td>90</td>
<td>50</td>
<td>50</td>
<td>8.5 e-11</td>
<td>8.6 e-11</td>
<td>1.1</td>
</tr>
<tr>
<td>90</td>
<td>66.7</td>
<td>66.7</td>
<td>8.67 e-11</td>
<td>8.88 e-11</td>
<td>2.3</td>
</tr>
<tr>
<td>90</td>
<td>83.4</td>
<td>83.4</td>
<td>8.85 e-11</td>
<td>9 e-11</td>
<td>1.6</td>
</tr>
<tr>
<td>90</td>
<td>100</td>
<td>100</td>
<td>9 e-11</td>
<td>9.15 e-11</td>
<td>1.6</td>
</tr>
</tbody>
</table>

The capacitive load considered is equal to three fanouts, which is the typical loading considered by most circuit designers. The error between the analytical and simulated values is found to reduce with an increase in capacitive load because:
a. In the analytical derivation we assume that the NMOST always operates in the linear region while in the actual simulation the NMOST operates initially in saturation and later in the linear mode.

b. The contribution of the PMOST is neglected in the analytical solution.

5.5.4 Discussion and Conclusion

A current expression for a short channel MOSFET incorporating the following short channel effects is derived:

i. Channel length modulation.
ii. DIBL.
iii. Mobility degradation due to high electric field.
iv. Velocity saturation.
v. Parasitic drain / source series resistance.

The novelty lies in the fact that the current expression is entirely layout and process based and therefore potentially scalable. These advantages are extended to the propagation delay model derived from the current equation. The credibility of the model is established by benchmarking it against a robust numerical model – SPICE 3.

The delay model is simplistic since it does not include the contribution of the input voltage ramp on delay, however it helps the circuit designer to predict the intrinsic delay due to physical devices (MOS transistor in this case). Secondly, the analytical delay model is several orders of magnitude faster than simulation thus consuming less CPU time.
5.5 References


[5.5.7]. A. Kloes and A. Kostka, "A New Analytical Method of Solving the 2D Poisson's Equation in MOS Device Applied to Threshold Voltage and

5.6 Conclusion

In this concluding chapter of the thesis, I have shown the application of the delay and short circuit power dissipation macromodels in VLSI circuit design. The models help VLSI designers to predict the effect of process or layout parameters on the circuit behavior. The accuracy of these models is not as high as numerical models but then the numerical models are neither scalable nor predictive. The aim of the research has been to establish compact physical MOSFET models as another helpful tool in the hands of the VLSI designer and we feel that we have done justice.

Long term reliability of MOS VLSI circuits is becoming an important issue as the densities of VLSI chips increase with shrinking design rules. The assessment and improvement of reliability on the circuit level should be based on both the failure mechanism observed in integrated circuits. While some of the physical degradation mechanism, such as electro-migration and electrostatic discharge, manifest themselves by abrupt and catastrophic changes in the device characteristics and the circuit operation, other mechanisms, such as hot carrier effects, cause non catastrophic failures which develop gradually over time and change the circuit performance. The PREDICTMOS model being physics based can form the basis of a macromodel used to predict non catastrophic failures e.g hot carrier stress. The macromodel would be useful to evaluate circuit performance over time.