CHAPTER 8

CONCLUSION

The main focus of our thesis is on the memory architecture of parallel computer. In parallel computer architecture where lots of operations are performed simultaneously, so it become necessary that memory operation must be ordered. All processor having its own local memory like distributed memory architecture that is accessible only to that processor, requires very less memory ordering. But system like Distributed Shared Memory system where processors have common memory with single address space, allows all processor to access entire memory. As DSM system allows multiple processors to access memory location simultaneously, so it requires an abstract model for memory operations that allow using memory location correctly and maintaining memory consistency. The memory consistency plays important role in DSM system because it specifies order of memory operation.

The thesis has addressed several important issues for distributed shared memory system. But it mainly concentrates on designing of distributed shared memory framework for memory consistency maintenance. The framework is designed with the help of memory consistency model and memory coherence. So appropriate memory consistency model and memory coherency is required for the proper
design of the framework. The thesis defines & verifies various memory consistency models on unified framework for finding the appropriate memory consistency. The main issues taken so far are

1. Designing and defining of the memory consistency model on unified framework
2. Verification of memory consistency model.
3. Selection of perfect memory consistency model
4. Designing framework for DSM system with the help of memory consistency model and memory coherency.
5. Data Replication
6. Parallelism improvement in DSM framework.
7. Overheads analysis of the framework
8. Paging Implementation

For issue 1 and 2 we have designed a structural memory model for Uniform & Hybrid memory consistency model on unified framework. The entire consistency models for uniform as well as hybrid memory model are defined and verified on the basis of designed structural memory model. A relation between consistency models is also developed to understand the memory consistencies perfectly. After analyzing all the memory consistency it is found that processor consistency is best suitable memory consistency for our framework. For issue 4 we have designed a DSM framework with processor consistency and write-update coherence protocol. The data replication in the proposed framework is done by multiple read and multiple write (MRMW) algorithm. Parallelism improvement in DSM framework is shown through the degree of parallelism. The thesis analyzed different overheads such as page fault service overhead, coherence maintenance overhead and network
communication overheads. On the basis of these different overheads the paging is implemented in the framework. The concept of variable page size is taken for proper implementation of paging technique. The page size is tested with different parameter such as number of writes, number of shared nodes and the different overheads and observed that the page size is increased as the number of writes is increased.

8.1 Summary

The thesis has described a new mechanism for designing DSM framework. Chapter 2 lays down the foundation for this by analyzing the works done in the field of DSM system. The chapter discusses various topics like shared memory abstraction, memory consistency model, memory coherence and some implementation of DSM system. The structural memory model of Uniform memory model and hybrid memory model is described in chapter 3 and chapter 4 respectively. The verification of memory consistencies has also been done in these chapters. This is the result of chapter 3 and 4 that we were able to find the perfect memory consistency model for our DSM framework. The maintenance of memory consistency has been done in chapter 5. For this a DSM framework with processor consistency and write-update coherence protocol is designed. The degree of parallelism and performance of framework is discussed in chap 6. The chapter also proposes some algorithm for the message communication between processors. The false sharing, granularity, thrashing has been discussed in chapter 7. The chapter also discusses how the page size for the DSM framework is calculated. It analyzes the implementation of variable page size with
respect to different parameter like writes, processor and overheads. The framework gives the complete idea about synchronizing the memory operations, updating the message among shared processor, communication between processors etc.

8.2 Observation and Limitation

The main contribution of the thesis is verification of memory consistency model, parallelism improvement and paging implementation for Distributed Shared Memory system. A structural memory model for uniform and hybrid memory model is designed for defining and verifying different memory consistency. The verification of memory consistency is done on the basis of execution history of memory operation. The execution history of processor consistency shows that the writes in processor consistency is observed in each processor, but the order of reads from each processor is not restricted as long as they do not involve other processor. So processor consistency allows reads following write, to bypass the write. Write-update coherence protocol supports multiple producers and multiple consumers i.e. many processor can have multiple write access simultaneously. The DSM framework proposed in the thesis is designed with the concepts of processor consistency and write-update coherence protocol. That’s why the proposed DSM framework gives relaxation on memory order and supports multiple writes. As a result in the framework high data replication is done. The framework provides high degree of parallelism. The performance load of the framework is increased as numbers of writes or numbers of shared processor are increased. But it
has observed that the framework reduces performance load if numbers of reads are increased.

All communication between processors for updating the writes starts from the owner processor of the write operation. The updating process to other process is going on until the owner processor is acknowledged about the updates. For the proper communication a copy-list chain and page map table is made. Network communication overhead is also elaborated so that the perfect page size can be calculated. As the network communication overhead changes as per change of number of writes and number of shared processor, so the page size of the proposed DSM framework also changes. The variable page concept taken for the framework helps in performance load of the DSM system.

Anything can not be perfect it have always some limitation, the proposed DSM framework has also some limitation. The first one is that it concentrates mainly on synchronization of read/write operations not on process synchronization. In proposed framework process synchronization is done on communication level only. The second on is that paging implementation in the framework is an extension of traditional Virtual Memory systems. It is designed in a way that it will be transparent with respect to the memory system. The memory system of the framework is hidden from users of the system. So sometime it become difficult to choose the right size for the page because the pages not only depends on the system overheads but also depend on applications.

8.3 Future Work
One limitation of the work presented in this thesis is the relatively small number of applications used in the calculation of page size. The page size defined in the framework is based on system overheads. So extending these results with taking applications for framework would help improving our understanding. As the proposed framework concentrates on synchronization of memory operation only, so the framework can be extended with considering process synchronization also. An important direction of future research is to design and evaluate the performance of concurrency control mechanisms. On concurrency control mechanism the framework focuses on communication level only. It checks only that updating of processors completed successfully or not. The performance and speed of the framework can be increased with taking best suitable network topology for proper communication between processor.