CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

Semiconductor technology provides a powerful means for implementation of analog, digital and mixed signal circuits for high speed systems. The high speed systems, in turn depend on the clock generator circuits. A survey on the different types of phase locked loop architectures which can be used as a clock generator is carried out.

2.2 SURVEY ON CHARGE PUMP PHASE LOCKED LOOP ARCHITECTURES

The work by Jeong et al (1987) was focusing on the design of clock generation circuitry being used as a part of a high-performance microprocessor chip set. A self-calibrating tapped delay line is used to generate four non overlapping clock phases of a system clock. A charge-pump PLL calibrates the delay per stage of the delay line. This technique is used to obtain an accurate phase relationship between the off-chip reference clock and the internal clock signals. Experimental results have been shown with less than 2ns clock skew for clock frequencies from 1 to 18 MHz with 2µm n-well CMOS technology.

The design of Low jitter PLL for clock generator with a supply noise insensitive VCO was presented by Chang-Hyeon Lee et al (1998). In this work, in order to achieve a low-jitter PLL design, fully differential signal
and control paths of the VCO are maintained. The clock skew is less than 60ps with a peak to peak jitter of 100ps for a 200 MHz PLL clock frequency with a power dissipation of 16 mW.

The design of a fully integrated phase locked loop clock generator for a 1.0 GHz microprocessor using a 1.8V 0.25µm digital CMOS process was described by Boerstler and Jenkins (1998). The peak-to-peak jitter amounts to ±36ps with the high maximum lock frequency of 1560 MHz. Later, Boerstler (1999) proposed a design of a fully integrated, phase-locked loop clock generator/phase aligner for the POWER3 microprocessor using a 2.5V, 0.4µm digital CMOS6S process. Cycle to cycle jitter measurements with the microprocessor actively executing instructions were 10.0ps rms, 80ps peak to peak (P-P) measured from the clock tree. To consolidate, a demonstration of the viability of a low-jitter PLL design approach amenable to high-speed microprocessors was carried out in this work.

A 1.25 GHz monolithic CMOS PLL clock synthesis unit was fabricated in a 0.35µm CMOS process, occupying an active area of 1 mm^2 and consuming 100 mW power at 3.3V was proposed by Lizhong Sun and Tad Kwasniewski (1999) for data communications.

Ingino and von Kaenel (2001) suggested that jitter can be minimized by regulating the supply to the PLL’s noise-sensitive analog circuit blocks in order to filter out supply noise.

A fully integrated low-jitter CMOS phase-locked loop and clock buffer for low-power digital systems with a wide range of operating frequencies was described by Mansuri and Yang (2003). The operating frequency range of the PLL is 130 – 1600 MHz with peak to peak jitter of output clock of 28.89ps at 1 GHz.
Dual-slope phase frequency detector and charge pump architectures to achieve fast locking of phase locked loops are proposed and analyzed by Kuo-Hsing Cheng et al (2003). The output jitter obtained in this type of PLL is around 45ps at 80 MHz (divided by 8 VCO oscillation frequency 640 MHz).

The report by Burbidge et al (2004) gives an idea of charge pump PLL as a choice for embedded frequency synthesis applications.

A detailed study of these papers which are related to the charge pump-PLLs as clock generator gave an idea to implement a novel type of charge pump PLL for high speed microprocessor applications.

2.3 SURVEY ON ANALOG PHASE LOCKED LOOP ARCHITECTURES

A four-transistor four-quadrant analog multiplier using MOS transistors operating in the saturation region was discussed by Wang (1993). It is based on the square-law characteristic of a MOS transistor operating in the saturation region. The author has compared the MOS based multiplier with its BJT counterpart.

Razavi (1997) describes the design of a 2 GHz 1.6-mW phase locked loop (PLL) fabricated in an 18 GHz 0.6µm BiCMOS technology. It was suggested that the high-speed PLLs can be implemented as compact, low power circuits through the use of techniques such as crosscoupled delay elements, inductive peaking and minimum length ring oscillators.

A fully differential analog current steering technique is proposed by Lin Wu and Black (1998) to implement a Gbps serial communication PLL.
CMOS clock recovery circuit. It uses a fully differential current steering structure from phase detector to VCO with inherently good power supply rejection ratio. Another advantage of this circuit is its work at a reduced voltage swing; it can achieve very high speed and reduced power dissipation. Simulation results show that the jitter of this structure is about 60% that of traditional single ended approaches and it has the potential of working at even higher frequencies.

Payne et al (2001) has described the design and implementation of a current-mode PLL using a log-domain oscillator. The loop is fully tunable, with independent control of center frequency and loop bandwidth. The major benefit of these current-mode log-domain circuits is thought to be the potential for wide tuning range under low power supply voltages.

Lee (2002) analyzed the jitter in clock signals, linking noise in free-running oscillators to short-term and long-term time-domain behaviour of phase-locked loops. The jitter in clock signals was minimized to achieve accurate analog-to-digital conversion in mixed-signal circuits and establish reliable synchronization in data processing, networking and communication systems.

The analog PLLs have been focused in several books and papers like Razavi (2001), Best (2005), etc and it suggests that the use of differential voltage controlled oscillator is more advantageous than the single ended VCO.

With the help of this survey, implementation of the single ended and differential VCO based PLLs with a four quadrant multiplier as phase detector are carried out. It is also compared with the Gilbert cell multiplier based PLL with three stage ring oscillator VCO.
2.4 SURVEY ON ALL-DIGITAL PHASE LOCKED LOOP ARCHITECTURES

The most important use of PLL Circuit is the recovery of the clock from a given data and the regeneration of the clock stream (Terng-Yin Hsu et al 1999). The data coming into the recovering circuit is jittered due to intersymbol interference and other undesirable effects that happen in the real world such as power supply noise, component tolerance and any added noise at the Voltage Controlled Oscillator (VCO) input. This means that the received data edges (i.e., zero crossing, transitions, etc.) are not happening at a fixed time period but are varying around the ideal. The PLL, being a narrow-band system, will tend to average out these variations and produce a clock which is closer to the ideal. Therefore a low jitter performance is essential for any PLL.

In order to cover a wide range of applications with different frequency specifications and to allow the adaptation for different semiconductor technologies, the design of the ADPLL should be portable. This means it has to rely on standard cells only and must not contain library specific components that have to be redesigned when the technology changes. The design is adapted solely by readjusting the parameters that define its performance (Duo Sheng et al 2006). Thereby the redesign of the ADPLL components is avoided. A hardware description language based design of the ADPLL will be beneficial as it permits design debugging at a high level and enables system simulation in a digital simulator including the ADPLL. A novel DCO proposed achieves 1.06ps resolution and can extend the controllable range easily. Furthermore, the HDL offers an easy and fast facility to modify the parameters of a design.
The concepts, design and potential applications of all-digital phase locked loop in digital signal processors was discussed by Shayan and Le-Ngoc (1989).

Lundberg and Nuckolls (1994) suggested that analog PLLs are not well suited as clock generators for high speed, low power microprocessors. The authors described an all digital PLL with 50 cycle lock time and 1 cycle shutdown to zero power. The ADPLL achieved a skew-to-reference of less than 250ps and a peak-to-peak jitter under 125ps at 200 MHz. Later, Dunning et al (1995) implemented the ADPLL design with 6000 transistors using 0.5µm CMOS process with the operating frequency of upto 900 MHz at 3.3 V supply voltage.

The design and implementation of an all digital phase locked loop circuit with a small DCO and fast phase lock was proposed by Jen-Shiun Chiang and Kuang-Yuan Chen (1999). The core of the ADPLL is the switch-tuning digital control oscillator. The ADPLL has the characteristics of fast frequency locking, full digitization, easy design and implementation and good stability. The authors suggest that the design is suitable for use as the clock generator for high performance microprocessors.

A novel ADPLL with ultra fast locked time and high oscillation frequency is proposed by Kuo-Hsing Cheng and Yu-Jung Chen (2001). The phase lock process takes 20 reference cycles and the maximum frequency is about 820 MHz. The Simulation tools were Verilog-XL. The jitter of the new ADPLL is about 150ps at 730 MHz.

Ching-Che Chung and Chen-Yi Lee (2002) implemented an ADPLL with standard cells. It can operate from 40 MHz to 540 MHz. The peak to peak jitter is less than ±170ps. Later, Ching-Che Chung and Chen-Yi
Lee (2003) proposed an ADPLL that can also be implemented with standard cells and with good portability over different processes. The ADPLL was implemented in a 0.35μm 1P4M CMOS standard cell library. It can operate from 45 to 510 MHz. The peak to peak jitter of the output clock is less than 70ps and the rms jitter of the output clock is less than 22ps at 500 MHz. The ADPLL designed was suggested as a clock generator for SoC applications. A performance comparison with the other reports was also carried out.

Watanabe and Yamauchi (2003) proposed an all-digital phase-locked loop circuit in which the resolution in the phase detector and digitally controlled oscillator matches exactly the gate-delay. It can be used for frequency multiplication by 4 to 1022 with seven-cycle lock time and a high level of precision was achieved with a clock jitter standard deviation of 234ps. This digital PLL can withstand a broad range of operating environments, from 30ºC to 140ºC and is suitable for making a programmable clock generator on a chip.

A hardware implementation of an ADPLL-based clock generator has been presented by Stefo et al (2003). The proposed design can easily be fitted into different processes without the need to redesign any of its components. It uses a novel DCO that allows the generation of a clock signal with a high frequency resolution and a small jitter. It has been implemented in a V400BG432 VIRTEX FPGA and synthesized for two different standard cell libraries. The maximum lock-in time is 30 reference clock cycles.

A fully integrated digitally controlled phase-locked loop used as a clock multiplying circuit was designed and fabricated by Olsson and Nilsson (2004). The PLL has no off-chip components and it was made from standard cells found in most digital standard cell libraries. The design is, therefore,
portable between technologies as an IP block. The VHDL description of the PLL makes it easy to include in digital simulations and then to synthesize to any technology assuming a DCO is available. The peak to peak jitter incurred is 775ps.

2.5 SURVEY ON ALL–DIGITAL DELAY LOCKED LOOP ARCHITECTURES

Bum-Sik Kim and Lee-Sup Kim (1998) have proposed a basic counter type low power all digital delay-locked loop. This all digital DLL was useful for synchronization of high frequency VLSI system with low power consumption and small area. Two new design methods were presented. First, the operation was described by Verilog HDL and verified. Secondly, by the circuit level simulations and optimizations, low power consumption and high speed were achieved. A Low power 100 MHz all digital delay locked loop consists of a type IV phase detector, Up-down counters, 8-stage coarse delay and fine delay units. This design operates with a frequency greater than 100 MHz with a capture time of less than 5µs and maximum error of 200ps. First, the operation was described by Verilog HDL and verified. Second, by the circuit level simulations and optimizations, low power consumption and high speed were achieved.

Garlepp et al (1999) proposed a portable digital delay-locked loop (DLL) for high speed CMOS interface circuits that achieves an infinite phase range and 40ps worst case phase resolution at 400 MHz was developed in a 3.3V, 0.4µm standard CMOS process. The DLL uses dual delay lines with an end-of-cycle detector, phase blenders and duty-cycle correcting multiplexers. This more easily process-portable DLL achieves jitter performance comparable to a more complex analog DLL when placed into identical high-
speed interface circuits fabricated on the same test-chip die. At 400 MHz, the digital DLL provides < 250ps peak-to-peak long-term jitter at 3.3 V and operates down to 1.7 V, where it dissipates 60 mW. The DLL occupies 0.96 mm². The author had compared a typical analog and digital DLL at 3.3 V and 400 MHz and tabulated the observations indicating that the output clock jitter is 195ps and 245ps with a lock time of 2.0µs and 2.9µs respectively.

A1-Gb/s/pin 512-Mb DDRII SDRAM has been developed using a digital delay-locked loop (DLL) and a slew-rate-controlled output buffer by Tatsuya Matano et al (2003). The digital DLL has a frequency divider for DLL input, performs at an operating frequency of up to 500 MHz at 1.6 V and provides internal clocking with 50% duty-cycle correction. The DLL has a current-mirror-type interpolator which enables a resolution as high as 14 ps, needs no standby current and can operate at voltages as low as 0.8 V. The slew-rate impedance controlled output buffer circuit reduces the output skew from 107 to 10ps. This SDRAM was tested using a 0.13µm, 126.5mm² and 512Mb chip.

Hsiang-Hui Chang and Shen-Iuan Liu (2005) have developed wide-range and fast-locking all-digital cycle-controlled delay-locked loop using Successive-Approximation Register (SAR). Utilizing the cycle-controlled delay unit, the SAR type DLL reuses the delay units to enlarge the operating frequency range rather than cascade a huge number of delay units. Adopting the binary search scheme, the two-step Successive-Approximation Register (SAR) controller ensures the locking the input clock by the proposed DLL within 32 clock cycles regardless of input frequencies. The DLL operates in an open-loop fashion, once the lock occurs in order to achieve low jitter operation with small area and low power dissipation. Since the DLL was unable to track temperature or supply variations once it was in lock, it was best suited for a burst mode operation.
Cockburn and Keith Boyle (2006) have developed a basic counter type digital delay locked loop, synthesized from black box standard cells. Due to an aggressive design schedule and a limited number of designers, it was decided to synthesize the DLL from a VHDL model down to black box standard cells. This necessitated a robust, structural-level DLL design that would operate over a broad frequency range while tolerating a range of gate delays. The digital delay line was implemented as a cascade containing 256 inverter pairs. Altogether the DLL occupied 28200 sq.microns, which was only 0.405% of the 6.92 sq. mm core of the IC. The fabricated DLL was found to operate from 14 MHz up to the 166 MHz maximum frequency of the available tester.

Yang and Liu (2007) have proposed a wide-range all-digital delay-locked loop (ADDLL) to achieve low jitter, low power and process immunity. The variable successive approximation register-controlled algorithm was proposed to eliminate the harmonic-locking issue in wide-range operation. It can also achieve the fast-locking property and closed-loop operation.

2.6 SURVEY ON PHASE LOCKED LOOP ARCHITECTURES FOR ADC

Chen (1992) proposes an on-chip clock generator for clock de-skewing and perfect synchronization. The phase locked loop designed was used to synchronize the output of the color graphics display system’s three video Digital to Analog Converters (DACs) by putting an on-chip PLL in each DAC.

A high-speed, low-power clock generator for a microprocessor application was discussed by von Kaenel (1998). The circuit was
implemented in a CMOS 0.35µm process. The voltage-controlled-oscillator frequency range was between 350 MHz and 2.8 GHz, with a peak-to-peak cycle-to-cycle jitter lower than 16ps. While booting Unix on a system, the maximum phase misalignment is lower than ± 100ps.

Nilsson and Torkelson (1996) have shown a robust and easily implementable monolithic digital clock-generator for on-chip clocking of custom DSPs. It is a fully digital design suitable for both high-speed clocking and low-voltage applications. This clocking method is digital and it avoids analog methods like phase locked loops or delay line loops. Instead, the clock generator was based on a ring counter which stops a ring oscillator after the correct number of cycles. Both a 385 MHz clock and a 15 MHz custom DSP application using the on chip clocking strategy are described here. The prototypes have been fabricated in a 0.8µm standard CMOS process.

Chen Jia and BoanLiu (2003) propose a 250MHz clock for SoC systems. In order to reject the jitters, a voltage regulator is applied to reduce the power supply noise which is the dominant and common source of jitter. The design is simulated at different corners for 100 MHz. The VCO frequency is found to be 1 GHz. The jitter at 3.3 V supply was 4.372ps.

An adaptive-bandwidth PLL with an improved passive filter is described and analyzed by Song Ying et al (2007). The jitter performance of the proposed PLL was improved by applying matching technique and a voltage-to-voltage converter to the charge pump and VCO circuit respectively. The post simulation results demonstrate that the adaptive-bandwidth Charge Pump Phase Locked Loop (CPPLL) maintains optimal dynamic response and jitter performance in its operating range. Moreover, compared with the conventional CPPLL, the filter capacitance can be scaled down in the proposed PLL. The operating frequency range of the VCO is 100 MHz to 1 GHz with a jitter value greater than 1ps.